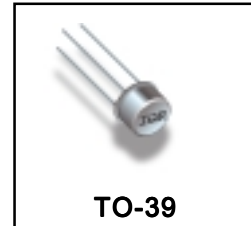


RADIATION HARDENED POWER MOSFET THRU-HOLE (TO-39)

IRHF7110 100V, N-CHANNEL RAD Hard™ HEXFET® TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	ID
IRHF7110	100K Rads (Si)	0.60Ω	3.5A
IRHF3110	300K Rads (Si)	0.60Ω	3.5A
IRHF4110	600K Rads (Si)	0.60Ω	3.5A
IRHF8110	1000K Rads (Si)	0.60Ω	3.5A



International Rectifier's RADHard HEXFET® technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low Rds(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Package
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
ID @ VGS = 12V, TC = 25°C	Continuous Drain Current	3.5	A
ID @ VGS = 12V, TC = 100°C	Continuous Drain Current	2.2	
IDM	Pulsed Drain Current ①	14	
PD @ TC = 25°C	Max. Power Dissipation	15	W
	Linear Derating Factor	0.12	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	68	mJ
IAR	Avalanche Current ①	—	A
EAR	Repetitive Avalanche Energy ①	—	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063 in.(1.6mm) from case for 10s)	
	Weight	0.98 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.10	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.60	Ω	V _{GS} = 12V, I _D = 2.2A ④
		—	—	0.69		V _{GS} = 12V, I _D = 3.5A
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 1.0mA
g _{fs}	Forward Transconductance	0.8	—	—	S (Ω)	V _{DS} > 15V, I _{DS} = 2.2A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100	nA	V _{GS} = -20V
Q _g	Total Gate Charge	—	—	11	nC	V _{GS} = 12V, I _D = 3.5A V _{DS} = 50V
Q _{gs}	Gate-to-Source Charge	—	—	3.0		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	3.3		
t _{d(on)}	Turn-On Delay Time	—	—	20	ns	V _{DD} = 50V, I _D = 3.5A V _{GS} = 12V, R _G = 7.5Ω
t _r	Rise Time	—	—	25		
t _{d(off)}	Turn-Off Delay Time	—	—	40		
t _f	Fall Time	—	—	40		
L _S + L _D	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C _{iss}	Input Capacitance	—	290	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{OSS}	Output Capacitance	—	100	—		
C _{rSS}	Reverse Transfer Capacitance	—	15	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	3.5	A	T _J = 25°C, I _S = 3.5A, V _{GS} = 0V ④
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	14		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _F = 3.5A, di/dt ≤ 100A/μs
t _{rr}	Reverse Recovery Time	—	—	180	nS	V _{DD} ≤ 50V ④
Q _{RR}	Reverse Recovery Charge	—	—	2.0	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	8.3	°C/W	Typical socket mount
R _{thJ-PCB}	Junction-to-Ambient	—	—	175		

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Parameter	Parameter	100-600K Rads(Si) ¹		1000K Rads (Si) ²		Units	Test Conditions
		Min	Max	Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	100	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.0	1.25	4.5		V _{GS} = V _{DS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V _{GS} = -20 V
I _{DSS}	Zero Gate Voltage Drain Current	—	25	—	25	μA	V _{DS} =80V, V _{GS} =0V
R _{DS(on)}	Static Drain-to-Source ④	—	0.60	—	0.80	Ω	V _{GS} = 12V, I _D = 2.2A
	On-State Resistance (TO-3)						
R _{DS(on)}	Static Drain-to-Source ④	—	0.60	—	0.80	Ω	V _{GS} = 12V, I _D = 2.2A
	On-State Resistance (TO-39)						
V _{SD}	Diode Forward Voltage ④	—	1.5	—	1.5	V	V _{GS} = 0V, I _S = 3.5A

1. Part numbers IRHF7110, IRHF3110, and IRHF4110

2. Part number IRHF8110

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET MeV/(mg/cm ²)	Energy (MeV)	Range (μm)	V _{DS} (V)				
				@V _{GS} =0V	@V _{GS} =-5V	@V _{GS} =-10V	@V _{GS} =-15V	@V _{GS} =-20V
Cu	28	285	43	100	100	100	80	60
Br	36.8	305	39	100	90	70	50	—

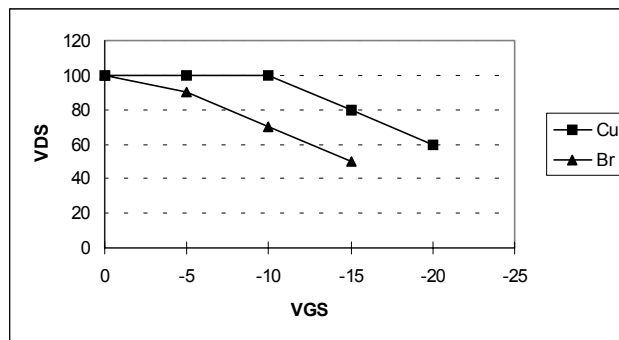


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

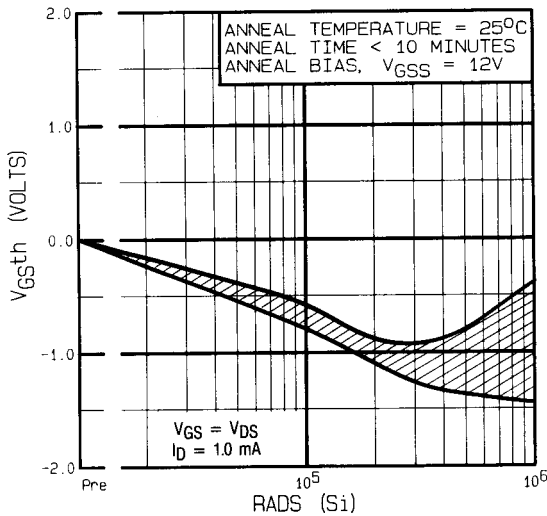


Fig 1. Typical Response of Gate Threshold Voltage Vs. Total Dose Exposure

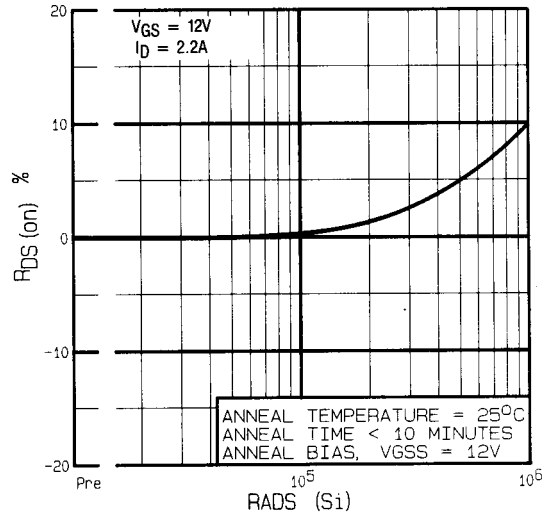


Fig 2. Typical Response of On-State Resistance Vs. Total Dose Exposure

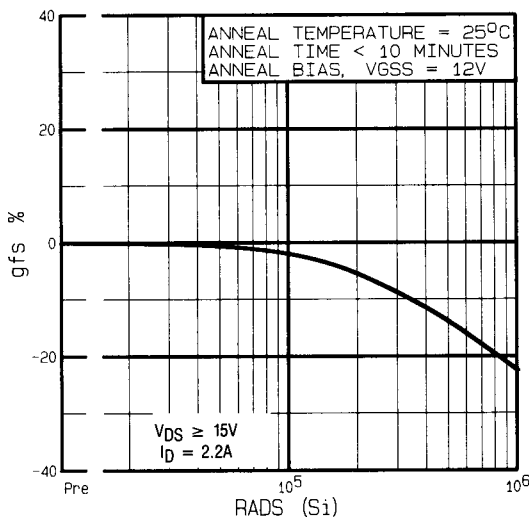


Fig 3. Typical Response of Transconductance Vs. Total Dose Exposure

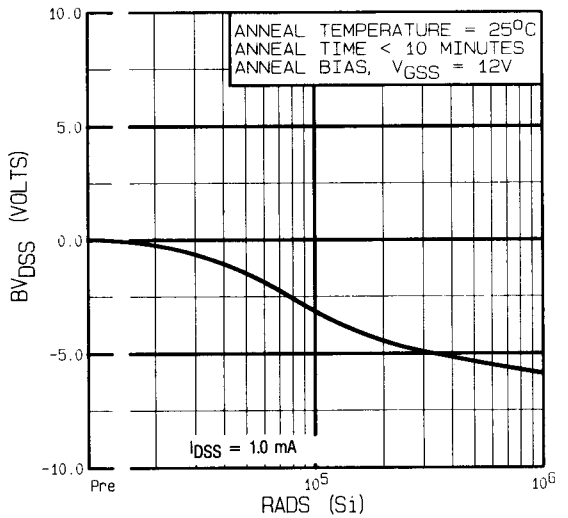


Fig 4. Typical Response of Drain to Source Breakdown Vs. Total Dose Exposure

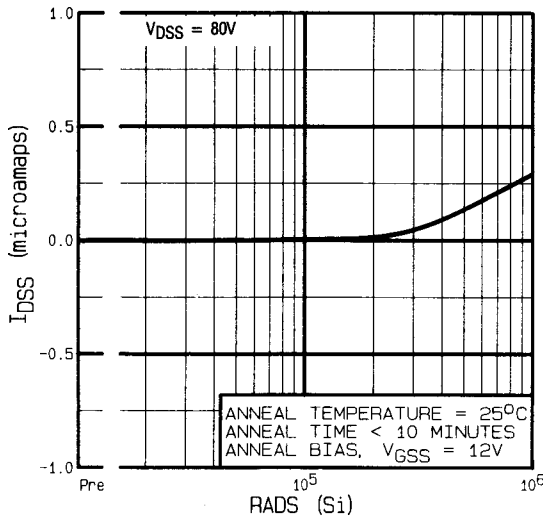


Fig 5. Typical Zero Gate Voltage Drain Current Vs. Total Dose Exposure

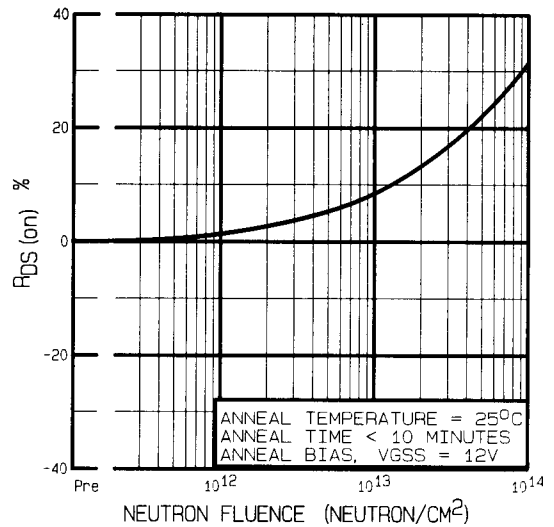


Fig 6. Typical On-State Resistance Vs. Neutron Fluence Level

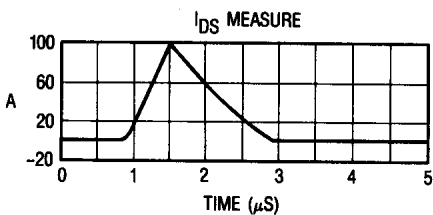
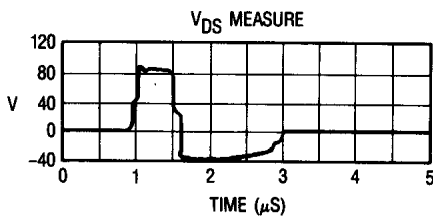


Fig 7. Typical Transient Response of Rad Hard HEXFET During 1×10^{12} Rad (Si)/Sec Exposure

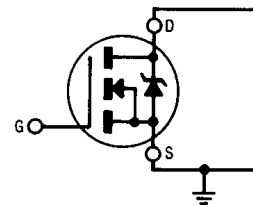


Fig 8a. Gate Stress of V_{GSS} Equals 12 Volts During Radiation

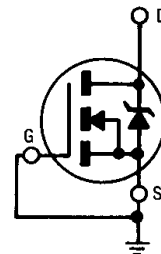


Fig 8b. V_{DSS} Stress Equals 80% of $B_{V_{DSS}}$ During Radiation

Note: Bias Conditions during radiation: $V_{GS} = 12\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$

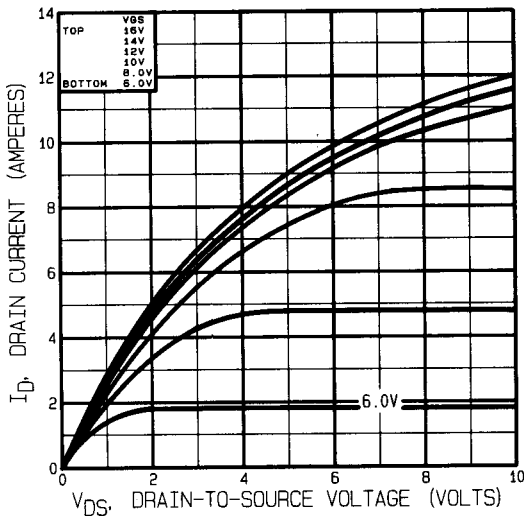


Fig 9. Typical Output Characteristics Pre-Irradiation

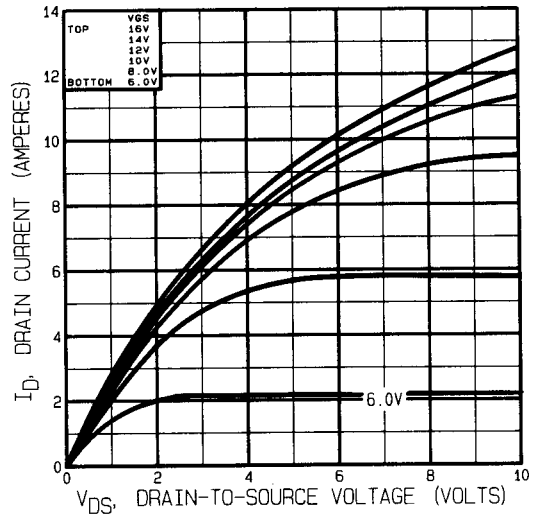


Fig 10. Typical Output Characteristics Post-Irradiation 100K Rads (Si)

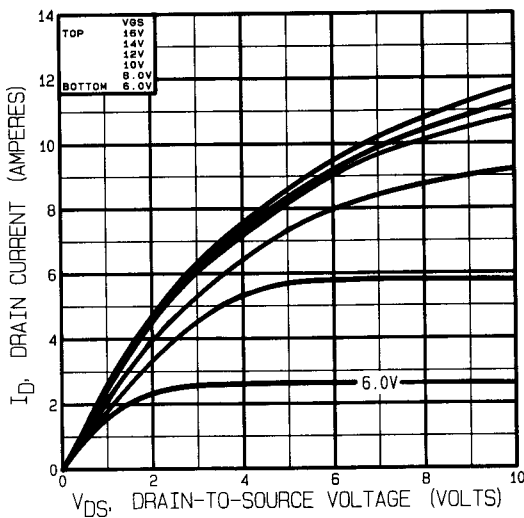


Fig 11. Typical Output Characteristics Post-Irradiation 300K Rads (Si)

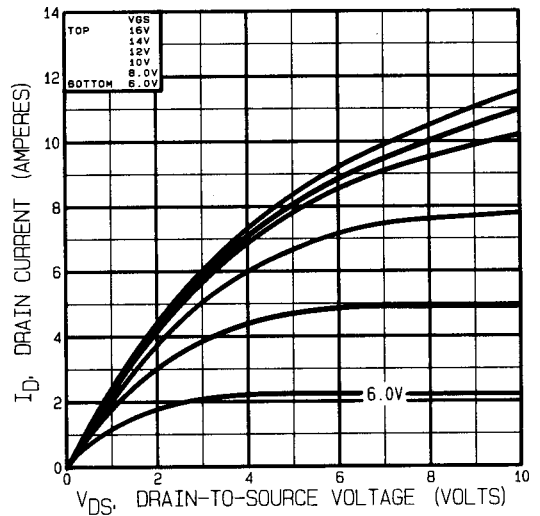


Fig 12. Typical Output Characteristics Post-Irradiation 1 Mega Rads (Si)

Note: Bias Conditions during radiation: $V_{GS} = 0$ Vdc, $V_{DS} = 80$ Vdc

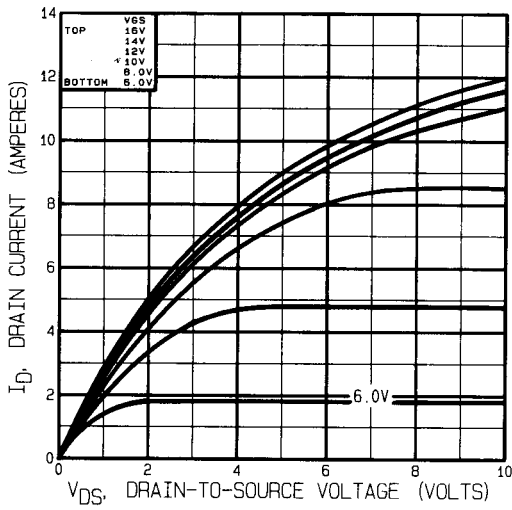


Fig 13. Typical Output Characteristics Pre-Irradiation

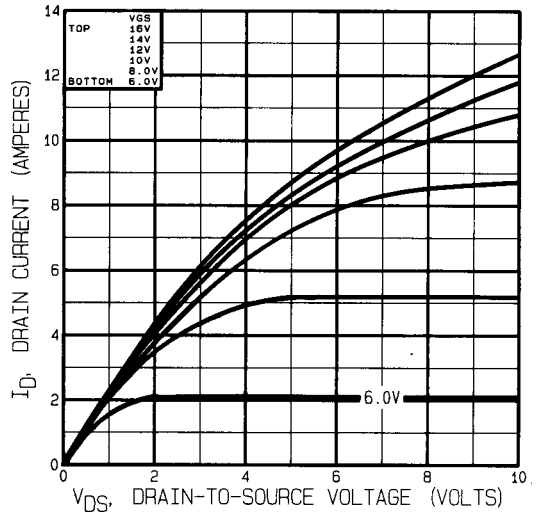


Fig 14. Typical Output Characteristics Post-Irradiation 100K Rads (Si)

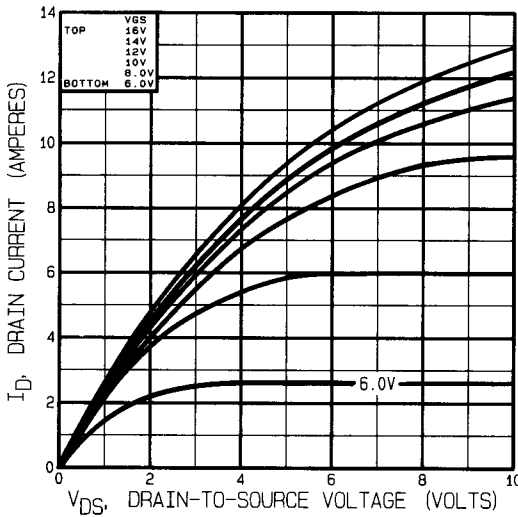


Fig 15. Typical Output Characteristics Post-Irradiation 300K Rads (Si)

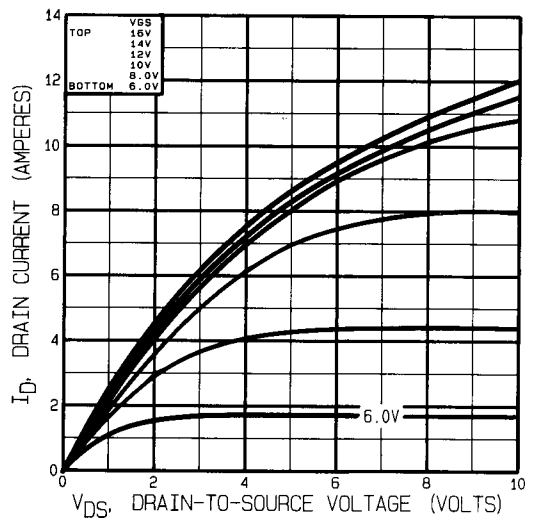


Fig 16. Typical Output Characteristics Post-Irradiation 1 Mega Rads (Si)

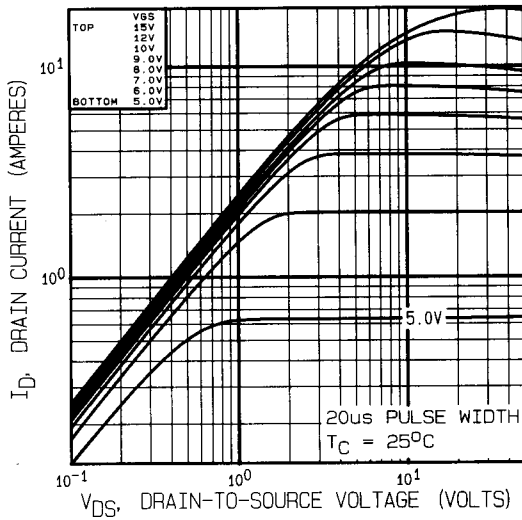


Fig 17. Typical Output Characteristics

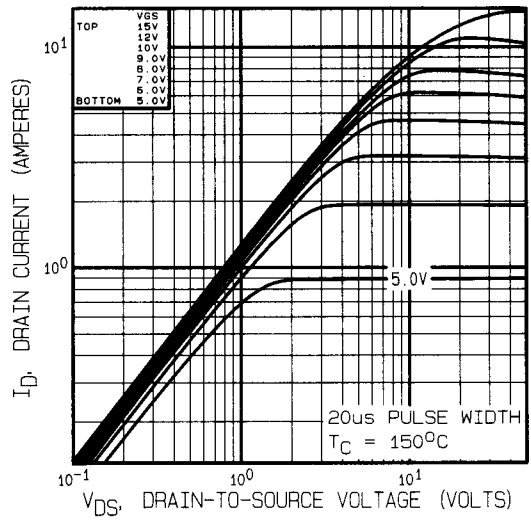


Fig 18. Typical Output Characteristics

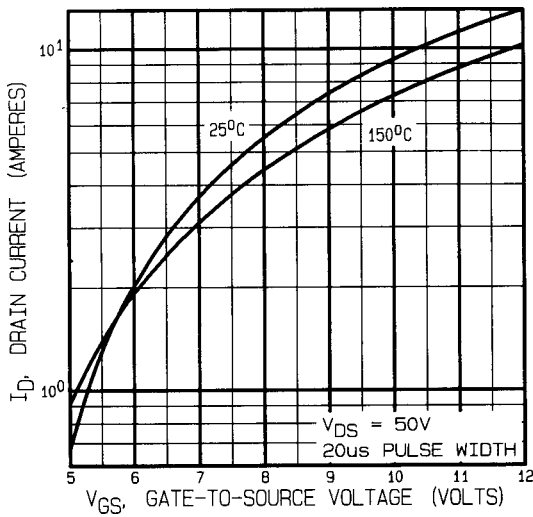


Fig 19. Typical Transfer Characteristics

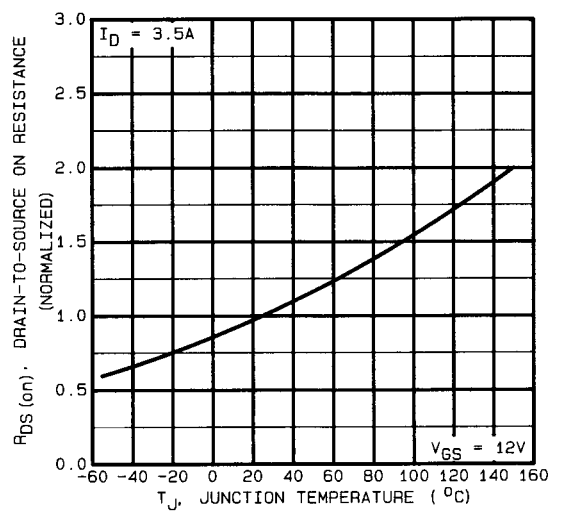


Fig 20. Normalized On-Resistance Vs. Temperature

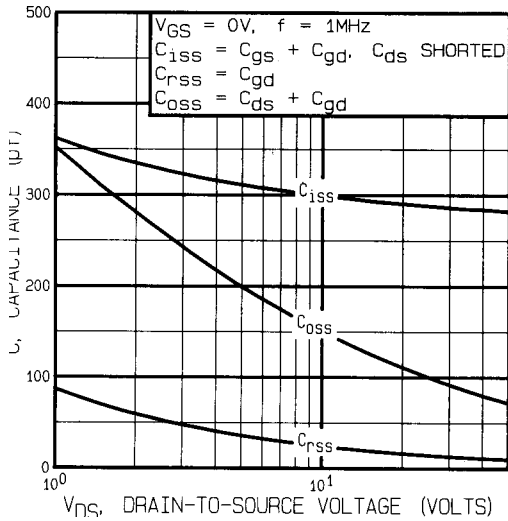


Fig 21. Typical Capacitance Vs. Drain-to-Source Voltage

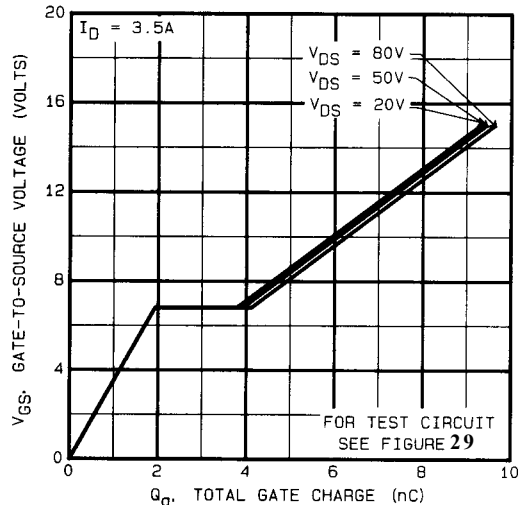


Fig 22. Typical Gate Charge Vs. Gate-to-Source Voltage

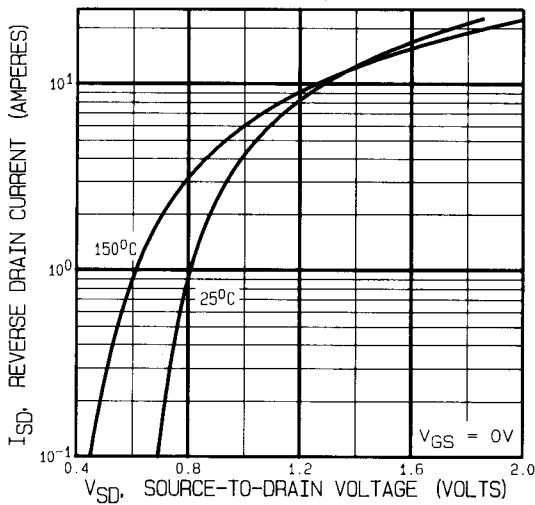


Fig 23. Typical Source-Drain Diode Forward Voltage

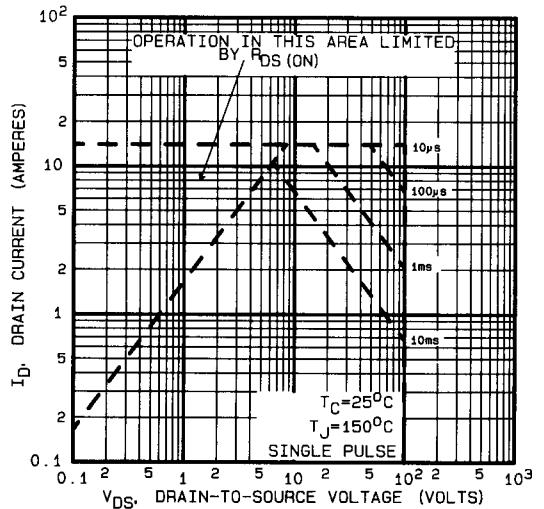


Fig 24. Maximum Safe Operating Area

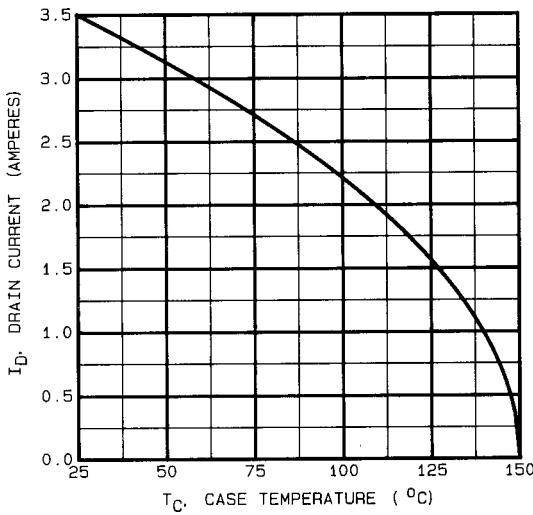


Fig 25. Maximum Drain Current Vs. Case Temperature

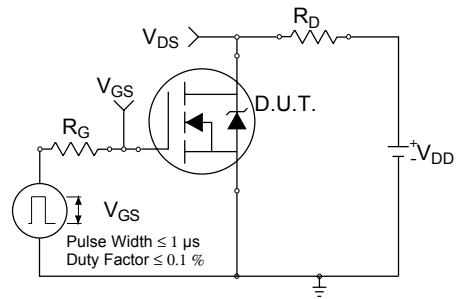


Fig 26a. Switching Time Test Circuit

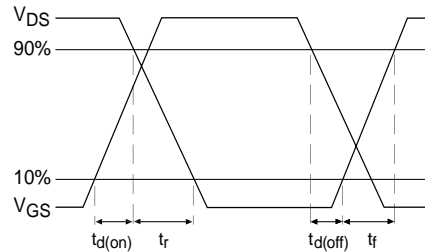


Fig 26b. Switching Time Waveforms

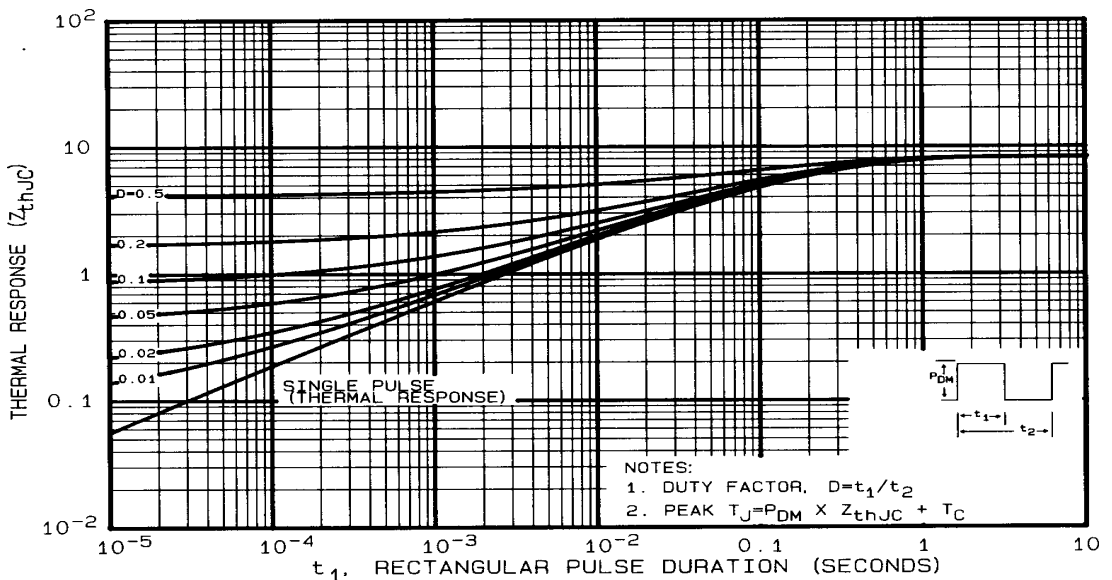


Fig 27. Maximum Effective Transient Thermal Impedance, Junction-to-Case

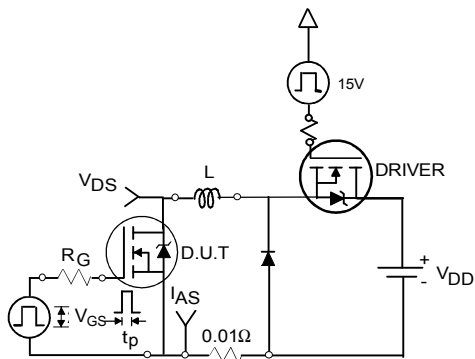


Fig 28a. Unclamped Inductive Test Circuit

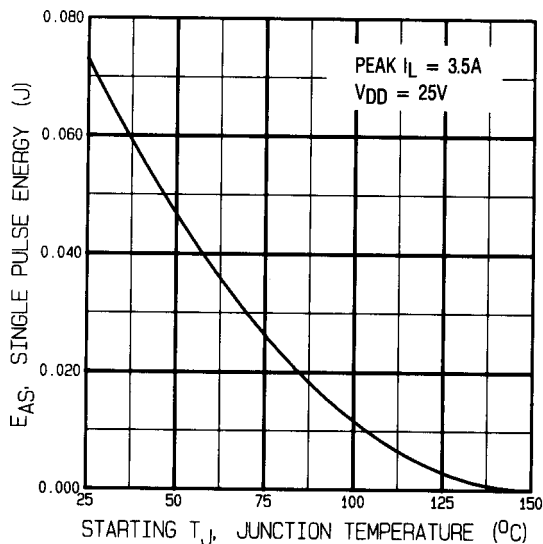


Fig 28c. Maximum Avalanche Energy Vs. Drain Current

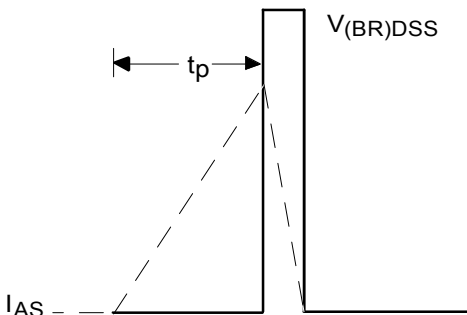


Fig 28b. Unclamped Inductive Waveforms

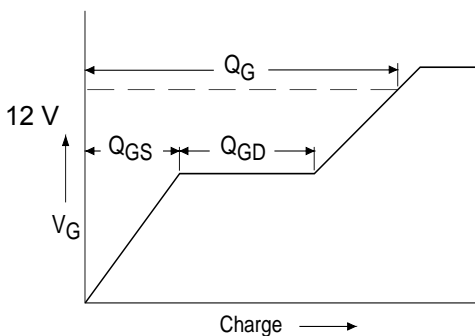


Fig 29a. Basic Gate Charge Waveform

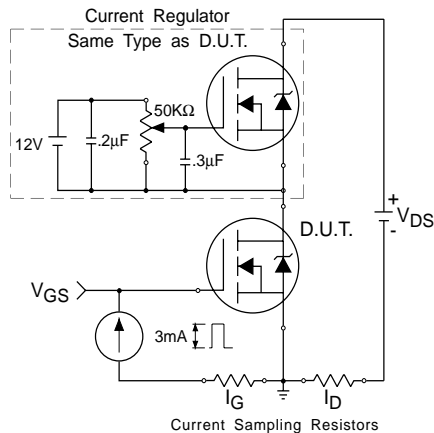
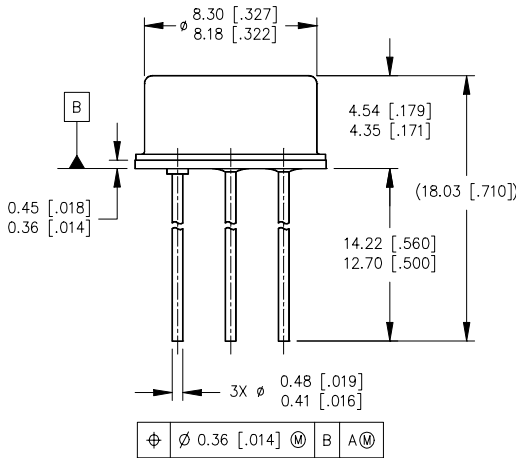


Fig 29b. Gate Charge Test Circuit

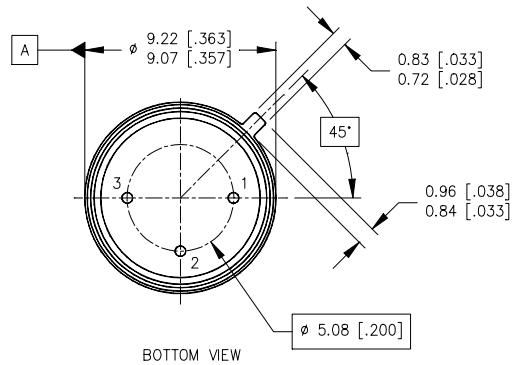
Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25V$, starting $T_J = 25^{\circ}C$, $L=11.1mH$
Peak $I_L = 3.5A$, $V_{GS} = 12V$
- ③ $I_{SD} \leq 3.5A$, $di/dt \leq 140A/\mu s$,
 $V_{DD} \leq 100V$, $T_J \leq 150^{\circ}C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
80 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — TO-205AF(Modified TO-39)



SIDE VIEW



BOTTOM VIEW

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME 14.5M-1994.
- 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3. CONTROLLING DIMENSION: INCH.
- 4. CONFORMS TO JEDEC OUTLINE TO-205AF (TO-39).

LEGEND

- 1- SOURCE
- 2- GATE
- 3- DRAIN



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

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