

HiPerFET™ Power MOSFETs Q-Class

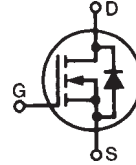
IXFH 30N60Q
IXFT 30N60Q

V_{DSS} = 600 V
I_{D25} = 30 A
R_{DS(on)} = 0.23 Ω

t_{rr} ≤ 250 ns

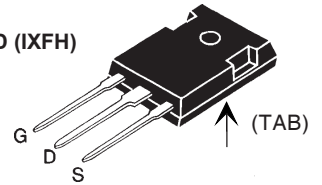
N-Channel Enhancement Mode
Avalanche Rated, High dv/dt, Low Q_g

Preliminary Data Sheet

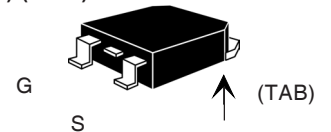


Symbol	Test Conditions	Maximum Ratings	
V _{DSS}	T _J = 25°C to 150°C	600	V
V _{DGR}	T _J = 25°C to 150°C; R _{GS} = 1 MΩ	600	V
V _{GS}	Continuous	±20	V
V _{GSM}	Transient	±30	V
I _{D25}	T _C = 25°C	30	A
I _{DM}	T _C = 25°C, pulse width limited by T _{JM}	120	A
I _{AR}	T _C = 25°C	30	A
E _{AR}	T _C = 25°C	45	mJ
E _{AS}	T _C = 25°C	1.5	J
dv/dt	I _S ≤ I _{DM} , di/dt ≤ 100 A/μs, V _{DD} ≤ V _{DSS} , T _J ≤ 150°C, R _G = 2 Ω	10	V/ns
P _D	T _C = 25°C	500	W
T _J		-55 ... +150	°C
T _{JM}		150	°C
T _{stg}		-55 ... +150	°C
T _L	1.6 mm (0.063 in) from case for 10 s	300	°C
M _d	Mounting torque	TO-247	1.13/10 Nm/lb.in.
Weight		TO-247	6 g
		TO-268	4 g

TO-247 AD (IXFH)



TO-268 (D3) (IXFT)



G = Gate
S = Source

D = Drain
TAB = Drain

Features

- Low gate charge
- International standard packages
- Epoxy meet UL 94 V-0, flammability classification
- Low R_{DS(on)} HD MOS™ process
- Rugged polysilicon gate cell structure
- Avalanche energy and current rated
- Fast intrinsic Rectifier

Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values (T _J = 25°C, unless otherwise specified)		
		min.	typ.	max.
V _{DSS}	V _{GS} = 0 V, I _D = 250 μA Temperature Coefficient	600	0.095	V %/K
V _{GS(th)}	V _{DS} = V _{GS} , I _D = 4 mA Temperature Coefficient	2.5	- 0.24	V %/K
I _{GSS}	V _{GS} = ±20 V _{DC} , V _{DS} = 0			±200 nA
I _{DSS}	V _{DS} = V _{DSS} , T _J = 25°C V _{GS} = 0 V, T _J = 125°C			25 μA 1 mA
R _{DS(on)}	V _{GS} = 10 V, I _D = 0.5 • I _{D25} Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			0.23 Ω

Fig. 1. Output Characteristics
@ 25 Deg. C

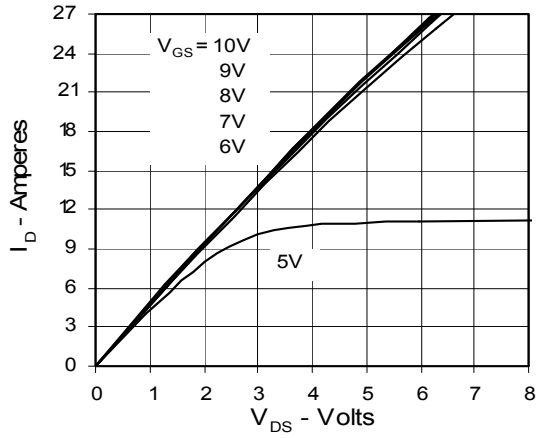


Fig. 2. Extended Output Characteristics
@ 25 deg. C

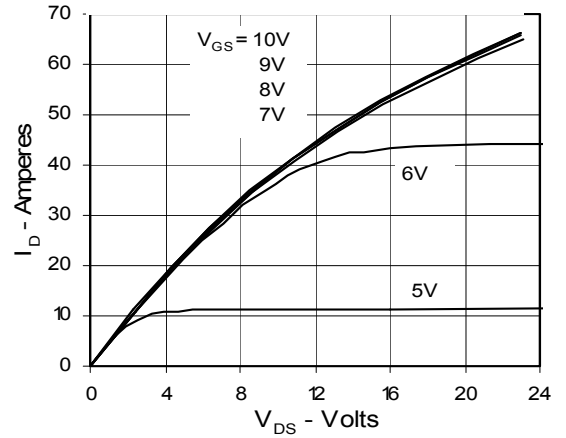


Fig. 3. Output Characteristics
@ 125 Deg. C

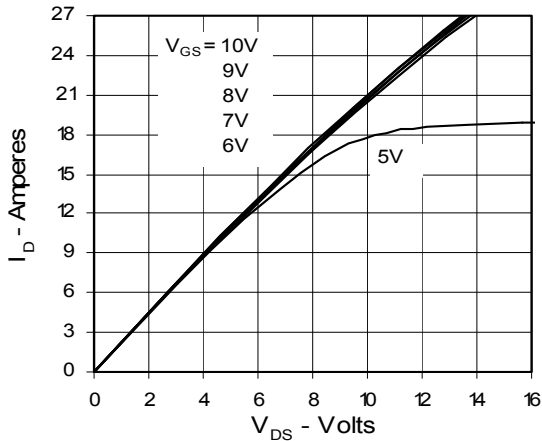


Fig. 4. $R_{DS(on)}$ Normalized to I_{D25} Value vs. Junction Temperature

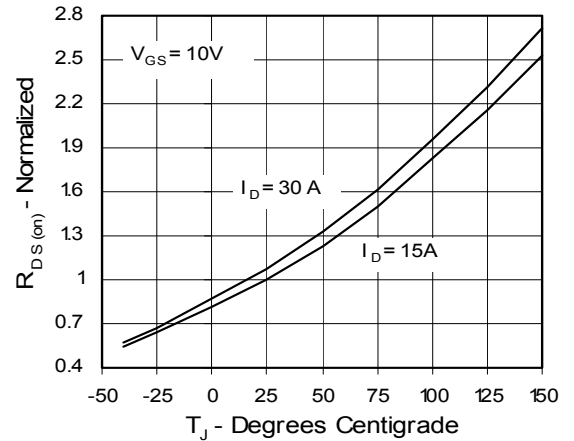


Fig. 5. $R_{DS(on)}$ Normalized to I_{D25} Value vs. I_D

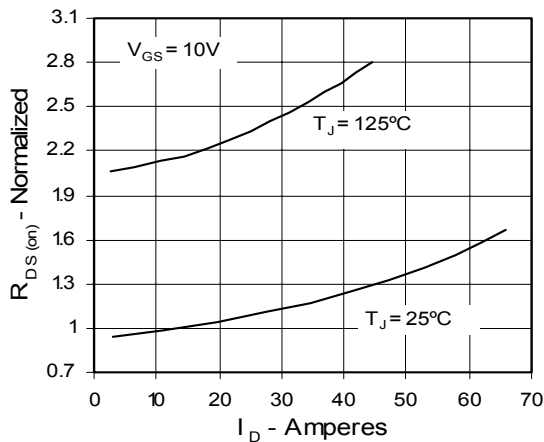


Fig. 6. Drain Current vs. Case Temperature

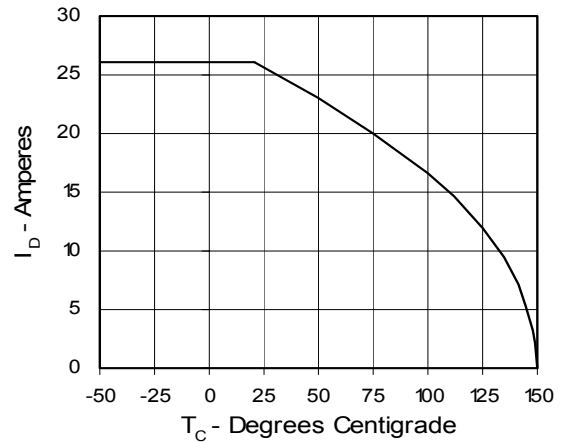


Fig. 7. Input Admittance

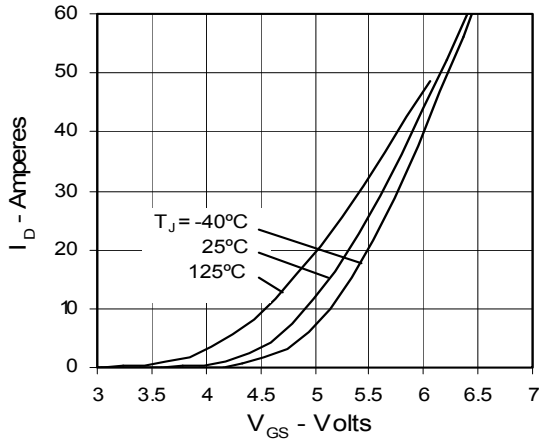


Fig. 8. Transconductance

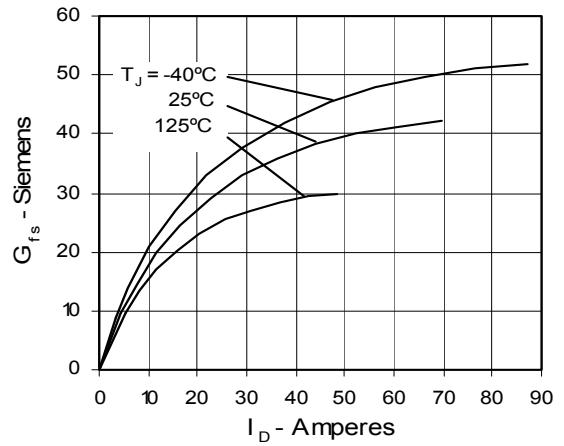


Fig. 9. Source Current vs. Source-To-Drain Voltage

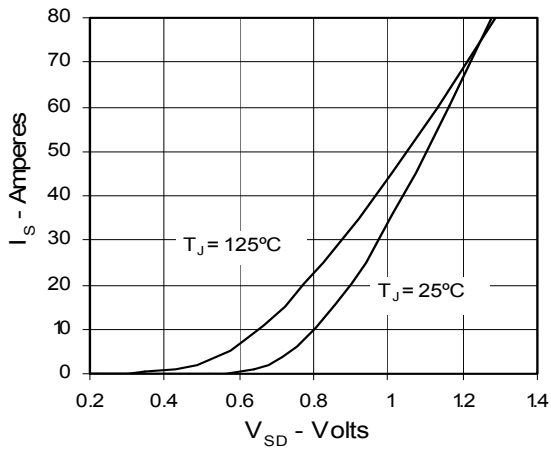


Fig. 10. Gate Charge

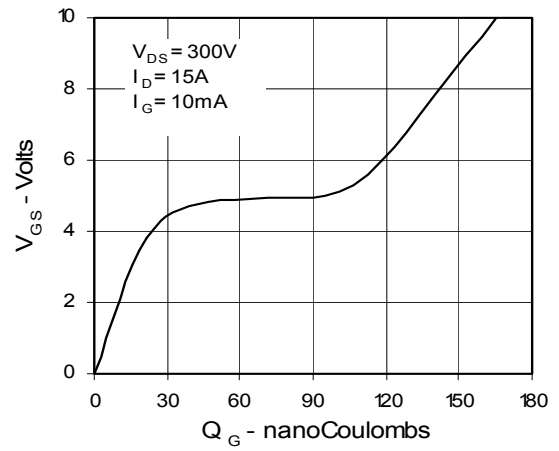


Fig. 11. Capacitance

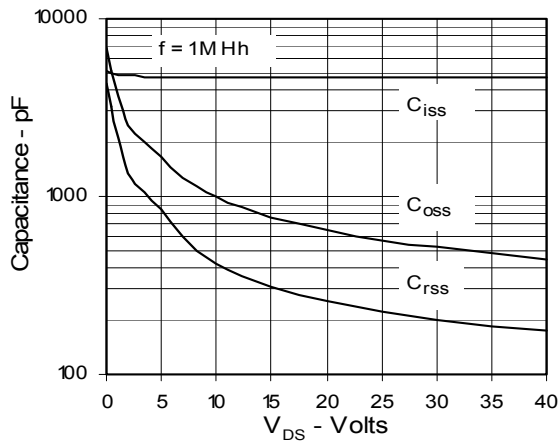
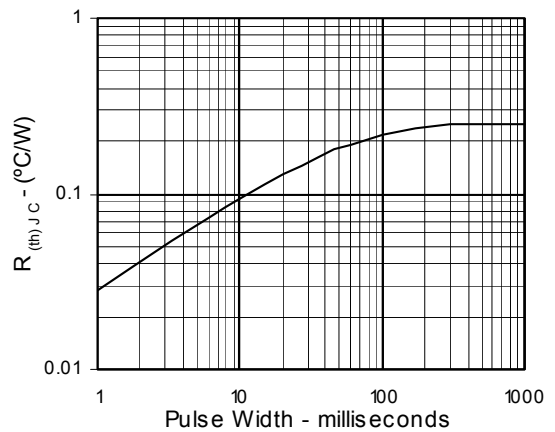


Fig. 12. Maximum Transient Thermal Resistance



IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 6,259,123B1 6,306,728B1
4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025 6,404,065B1 6,162,665 6,534,343



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