NEC

# MOS FIELD EFFECT TRANSISTOR
# 2SK3360

## SWITCHING
## N-CHANNEL POWER MOS FET
## INDUSTRIAL USE

### DESCRIPTION

The 2SK3360 is N-Channel MOS Field Effect Transistor designed for high current switching application.

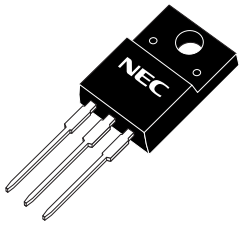
### ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| 2SK3360 | Isolated TO-220 |

### FEATURES

- Low on-state resistance
- ★ $R_{DS(on)1}$ = 30 mΩ MAX. ($V_{GS}$ = 10 V, $I_D$ = 18 A)
- ★ $R_{DS(on)2}$ = 40 mΩ MAX. ($V_{GS}$ = 4.5 V, $I_D$ = 18 A)
- ★ • Low $C_{iss}$: $C_{iss}$ = 3200 pF TYP.
- Built-in gate protection diode
- Isolated TO-220 package

(Isolated TO-220)




### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C)

| | | | | |
|---|---|---|---|---|
| | Drain to Source Voltage | $V_{DSS}$ | 100 | V |
| | Gate to Source Voltage | $V_{GSS(AC)}$ | ±20 | V |
| | Gate to Source Voltage | $V_{GSS(DC)}$ | +20, –10 | V |
| ★ | Drain Current (DC) | $I_{D(DC)}$ | ±35 | A |
| ★ | Drain Current (pulse) [Note1] | $I_{D(pulse)}$ | ±140 | A |
| | Total Power Dissipation ($T_C$ = 25°C) | $P_T$ | 35 | W |
| | Total Power Dissipation ($T_A$ = 25°C) | $P_T$ | 2.0 | W |
| | Channel Temperature | $T_{ch}$ | 150 | °C |
| | Storage Temperature | $T_{stg}$ | –55 to +150 | °C |
| ★ | Single Avalanche Current [Note2] | $I_{AS}$ | 35 | A |
| ★ | Single Avalanche Energy [Note2] | $E_{AS}$ | 122 | mJ |

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1 %

**2.** Starting $T_{ch}$ = 25 °C, $R_G$ = 25 Ω, $V_{GS}$ = 20 V→0 V

### THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| Channel to Case | $R_{th(ch-C)}$ | 3.57 | °C/W |
| Channel to Ambient | $R_{th(ch-A)}$ | 62.5 | °C/W |



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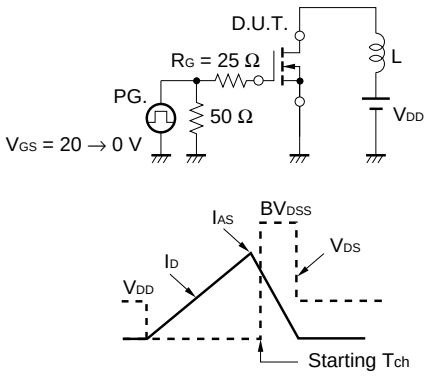
**The mark ★ shows major revised points.**

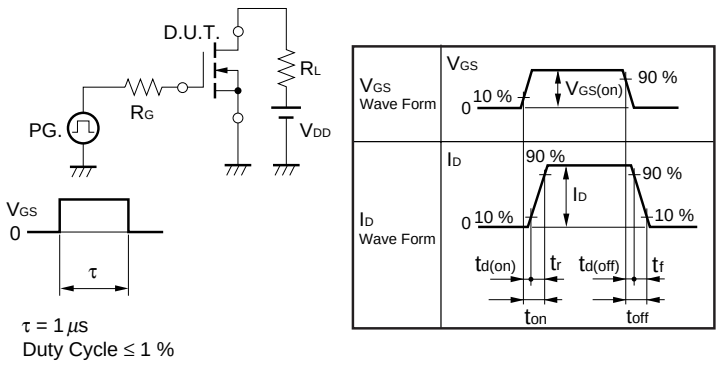
## ★ ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C)

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Drain to Source On-state Resistance | $R_{DS(on)1}$ | $V_{GS}$ = 10 V, $I_D$ = 18 A | | 20 | 30 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = 4.5 V, $I_D$ = 18 A | | 28 | 40 | mΩ |
| Gate to Source Cut-off Voltage | $V_{GS(off)}$ | $V_{DS}$ = 10 V, $I_D$ = 250 μA | 1.5 | 2.0 | 2.5 | V |
| Forward Transfer Admittance | $\|y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 18 A | 13 | 28 | | S |
| Drain Leakage Current | $I_{DSS}$ | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V | | | 10 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V | | 3200 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | | 640 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 360 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $I_D$ = 18 A | | 35 | | ns |
| Rise Time | $t_r$ | $V_{GS(on)}$ = 10 V | | 220 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $V_{DD}$ = 50 V | | 220 | | ns |
| Fall Time | $t_f$ | $R_G$ = 10 Ω | | 190 | | ns |
| Total Gate Charge | $Q_G$ | $I_D$ = 35 A | | 84 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{DD}$ = 80 V | | 11 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $V_{GS(on)}$ = 10 V | | 31 | | nC |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | $I_F$ = 35 A, $V_{GS}$ = 0 V | | 0.96 | | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 35 A, $V_{GS}$ = 0 V | | 150 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100 A/μs | | 800 | | nC |

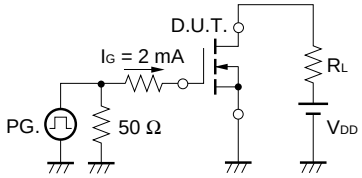
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**




**TEST CIRCUIT 2 SWITCHING TIME**

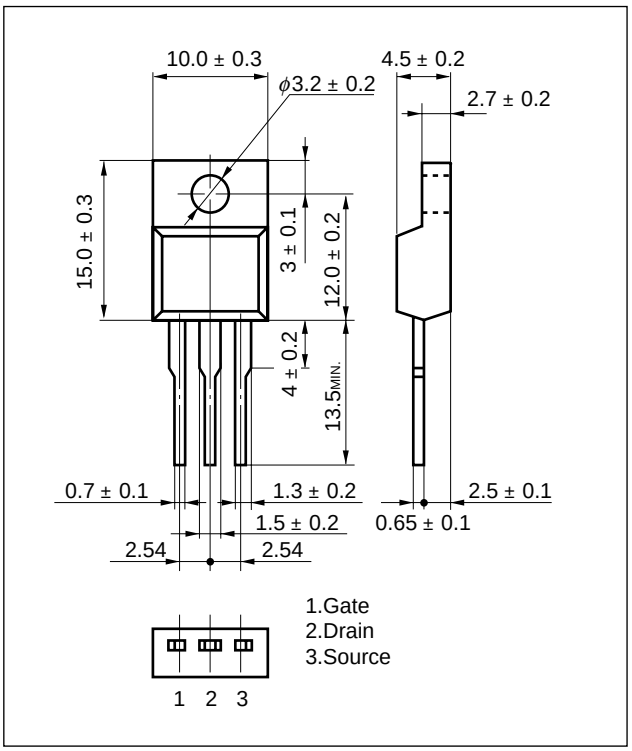



**TEST CIRCUIT 3 GATE CHARGE**

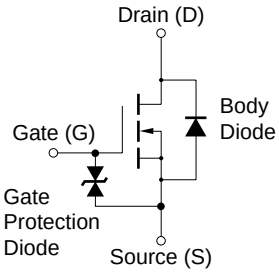


**PACKAGE DRAWING (Unit : mm)**

Isolated TO-220 (MP-45F)




**EQUIVALENT CIRCUIT**




**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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