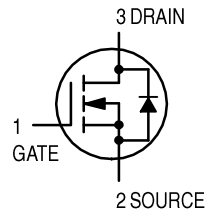


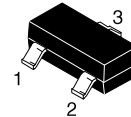


FET Transistor

N-Channel Enhancement



2N7002LT1



SOT-23

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	60	Vdc
Drain Current — Continuous $T_C = 25^\circ\text{C}$	I_D	± 115	mAdc
Continuous $T_C = 100^\circ\text{C}$	I_D	± 75	
Current — Pulsed(2)	I_{DM}	± 800	
Gate-Source Voltage			
— Continuous	V_{GS}	± 20	Vdc
— Non-repetitive ($t_p \leq 50 \mu\text{s}$)	V_{GSM}	± 40	Vpk

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board,(3) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate,(4) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

DEVICE MARKING

2N7002LT1 = 702

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 10 \mu\text{Adc}$)	$V_{(BR)DSS}$	60	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{GS} = 0, V_{DS} = 60 \text{ Vdc}$)	I_{DSS}	— —	— —	1.0 500	μAdc
Gate-Body Leakage Current, Forward ($V_{GS} = 20 \text{ Vdc}$)	I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GS} = -20 \text{ Vdc}$)	I_{GSSR}	—	—	-100	nAdc

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.
3. FR-5 = $1.0 \times 0.75 \times 0.062 \text{ in.}$
4. Alumina = $0.4 \times 0.3 \times 0.025 \text{ in.}$ 99.5% alumina.

2N7002LT1**ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS(2)					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{Adc}$)	$V_{GS(th)}$	1.0	—	2.5	Vdc
On-State Drain Current ($V_{DS} \geq 2.0\ V_{DS(on)}$, $V_{GS} = 10\ \text{Vdc}$)	$I_{D(on)}$	500	—	—	mA
Static Drain-Source On-State Voltage ($V_{GS} = 10\ \text{Vdc}$, $I_D = 500\ \text{mAdc}$) ($V_{GS} = 5.0\ \text{Vdc}$, $I_D = 50\ \text{mAdc}$)	$V_{DS(on)}$	— —	— —	3.75 0.375	Vdc
Static Drain-Source On-State Resistance ($V_{GS} = 10\ \text{V}$, $I_D = 500\ \text{mAdc}$) $T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$ ($V_{GS} = 5.0\ \text{Vdc}$, $I_D = 50\ \text{mAdc}$) $T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$	$r_{DS(on)}$	— — — —	— — — —	7.5 13.5 7.5 13.5	Ohms
Forward Transconductance ($V_{DS} \geq 2.0\ V_{DS(on)}$, $I_D = 200\ \text{mAdc}$)	g_{FS}	80	—	—	mmhos

DYNAMIC CHARACTERISTICS

Input Capacitance ($V_{DS} = 25\ \text{Vdc}$, $V_{GS} = 0$, $f = 1.0\ \text{MHz}$)	C_{iss}	—	—	50	pF
Output Capacitance ($V_{DS} = 25\ \text{Vdc}$, $V_{GS} = 0$, $f = 1.0\ \text{MHz}$)	C_{oss}	—	—	25	pF
Reverse Transfer Capacitance ($V_{DS} = 25\ \text{Vdc}$, $V_{GS} = 0$, $f = 1.0\ \text{MHz}$)	C_{rss}	—	—	5.0	pF

SWITCHING CHARACTERISTICS(2)

Turn-On Delay Time	($V_{DD} = 25\ \text{Vdc}$, $I_D \cong 500\ \text{mAdc}$, $R_G = 25\ \Omega$, $R_L = 50\ \Omega$, $V_{gen} = 10\ \text{V}$)	$t_{d(on)}$	—	—	20	ns
Turn-Off Delay Time		$t_{d(off)}$	—	—	40	ns

BODY-DRAIN DIODE RATINGS

Diode Forward On-Voltage ($I_S = 11.5\ \text{mAdc}$, $V_{GS} = 0\ \text{V}$)	V_{SD}	—	—	−1.5	Vdc
Source Current Continuous (Body Diode)	I_S	—	—	−115	mAdc
Source Current Pulsed	I_{SM}	—	—	−800	mAdc

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

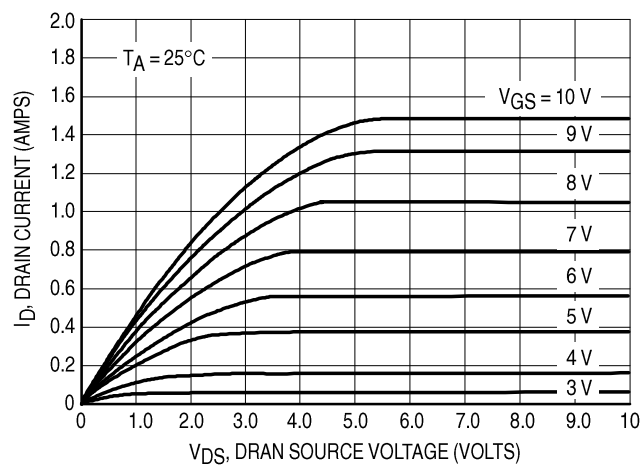


Figure 1. Ohmic Region

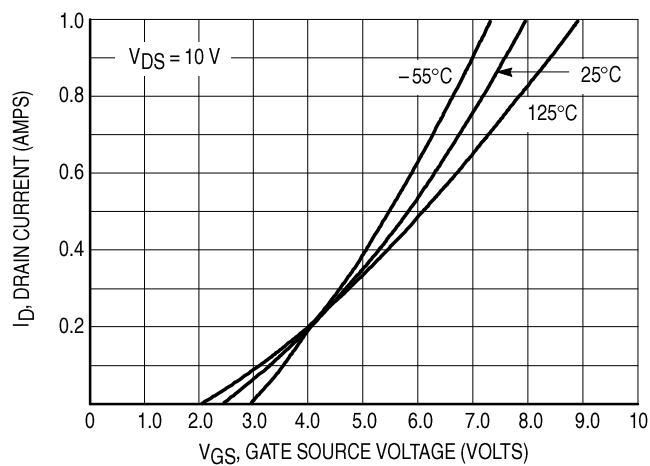


Figure 2. Transfer Characteristics

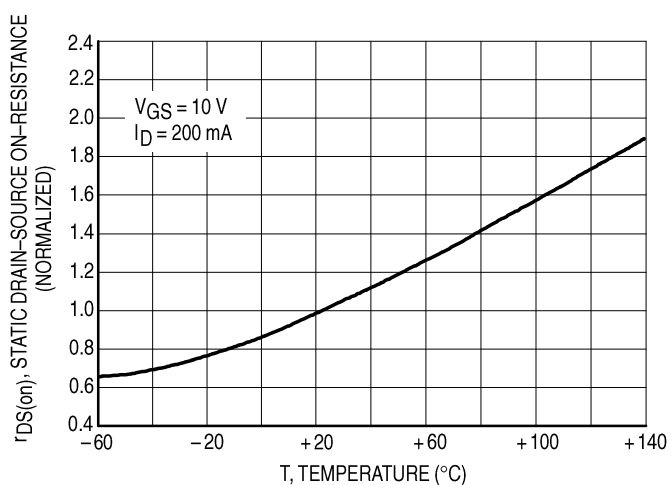


Figure 3. Temperature versus Static Drain-Source On-Resistance

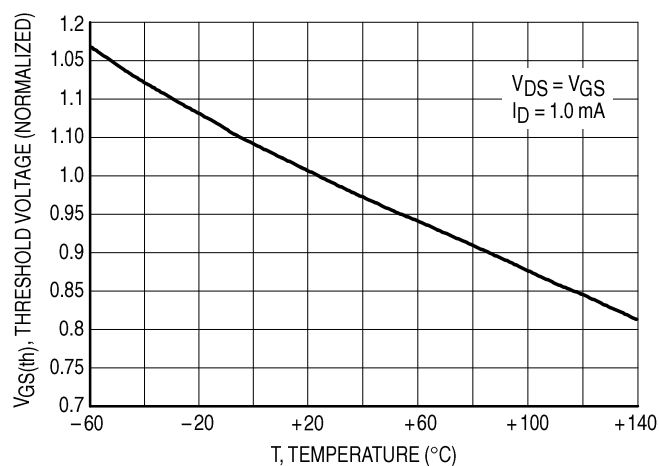
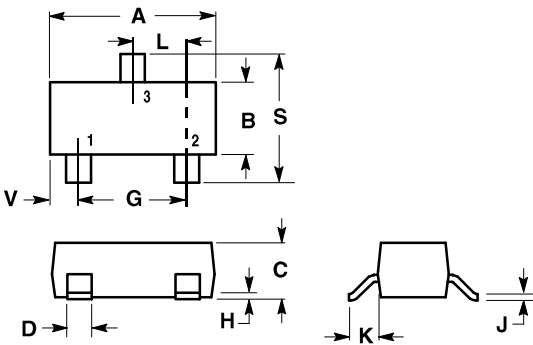


Figure 4. Temperature versus Gate Threshold Voltage

PACKAGE DIMENSIONS



SOT-23

- NOTES:
- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - 2. CONTROLLING DIMENSION: INCH.
 - 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

- STYLE 21:
- PIN 1. GATE
 - 2. SOURCE
 - 3. DRAIN

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