

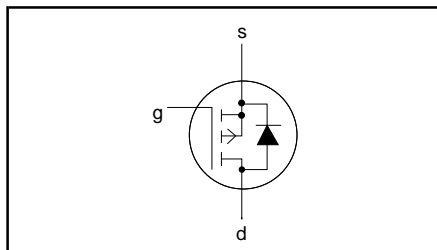
P-channel enhancement mode MOS transistor

BSH202

FEATURES

- Low threshold voltage
- Fast switching
- Logic level compatible
- Subminiature surface mount package

SYMBOL



QUICK REFERENCE DATA

$V_{DS} = -30\text{ V}$
$I_D = -0.52\text{ A}$
$R_{DS(ON)} \leq 0.9\ \Omega (V_{GS} = -10\text{ V})$

GENERAL DESCRIPTION

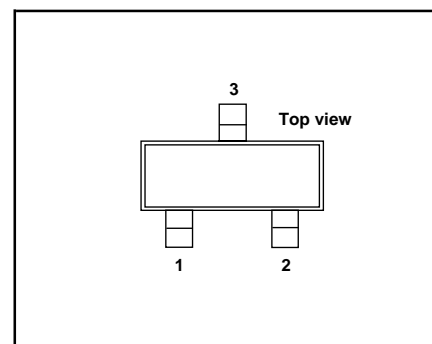
P-channel, enhancement mode, logic level, field-effect power transistor. This device has low threshold voltage and extremely fast switching making it ideal for battery powered applications and high speed digital interfacing.

The BSH202 is supplied in the SOT23 subminiature surface mounting package.

PINNING

PIN	DESCRIPTION
1	gate
2	source
3	drain

SOT23



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	-30	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	-30	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Drain current (DC)	$T_a = 25\text{ }^\circ\text{C}$	-	-0.52	A
		$T_a = 100\text{ }^\circ\text{C}$	-	-0.33	A
I_{DM}	Drain current (pulse peak value)	$T_a = 25\text{ }^\circ\text{C}$	-	-2.1	A
P_{tot}	Total power dissipation	$T_a = 25\text{ }^\circ\text{C}$	-	0.417	W
		$T_a = 100\text{ }^\circ\text{C}$	-	0.17	W
T_{stg}, T_j	Storage & operating temperature		-55	150	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-a}$	Thermal resistance junction to ambient	FR4 board, minimum footprint	300	-	K/W

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ELECTRICAL CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = -10\ \mu\text{A}$	-30	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = -1\ \text{mA}$	-1	-1.9	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	$T_j = 150^\circ\text{C}$ $V_{GS} = -10\ \text{V}; I_D = -280\ \text{mA}$ $V_{GS} = -4.5\ \text{V}; I_D = -140\ \text{mA}$	-0.4	-	-	V
g_{fs}	Forward transconductance	$V_{GS} = -10\ \text{V}; I_D = -280\ \text{mA}; T_j = 150^\circ\text{C}$	-	0.63	0.9	Ω
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0\ \text{V}$	-	0.89	1.35	Ω
I_{DSS}	Zero gate voltage drain current	$V_{DS} = -24\ \text{V}; I_D = -280\ \text{mA}; T_j = 150^\circ\text{C}$ $V_{DS} = -24\ \text{V}; V_{GS} = 0\ \text{V}; T_j = 150^\circ\text{C}$	-	0.95	1.35	Ω
$Q_{g(tot)}$	Total gate charge	$V_{DS} = -24\ \text{V}; I_D = -280\ \text{mA}$	0.2	0.7	-	S
Q_{gs}	Gate-source charge	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0\ \text{V}$	-	± 10	± 100	nA
Q_{gd}	Gate-drain (Miller) charge	$V_{DS} = -24\ \text{V}; V_{GS} = 0\ \text{V}; T_j = 150^\circ\text{C}$	-	-0.4	-10	μA
$t_{d\ on}$	Turn-on delay time	$I_D = -0.3\ \text{A}; V_{DD} = -15\ \text{V}; V_{GS} = -10\ \text{V}$	-	2.9	-	nC
t_r	Turn-on rise time		-	0.4	-	nC
$t_{d\ off}$	Turn-off delay time		-	0.5	-	nC
t_f	Turn-off fall time	$V_{DD} = -15\ \text{V}; I_D = -0.5\ \text{A}; V_{GS} = -10\ \text{V}; R_G = 6\ \Omega$	-	4.5	-	ns
C_{iss}	Input capacitance	Resistive load	-	45	-	ns
C_{oss}	Output capacitance		-	20	-	ns
C_{rss}	Feedback capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$	-	80	-	pF
			-	27	-	pF
			-	9	-	pF

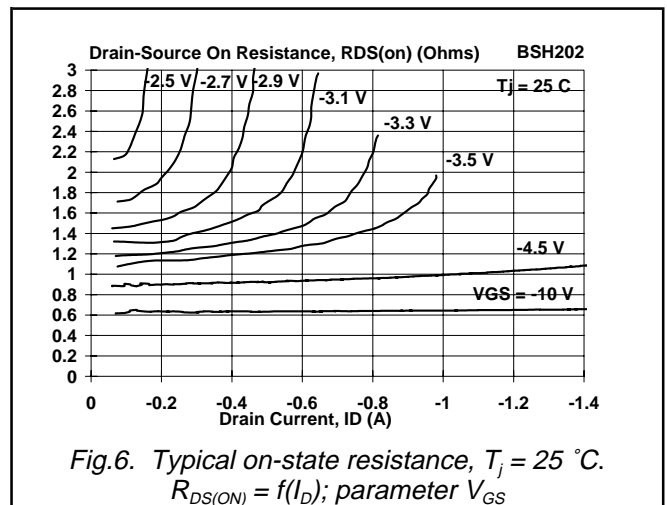
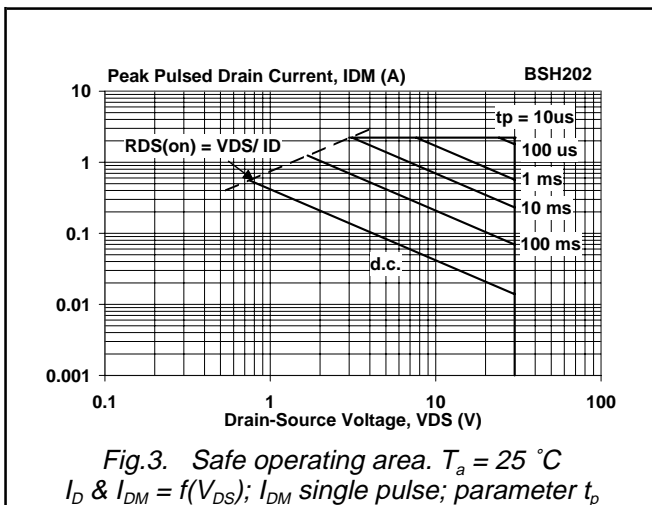
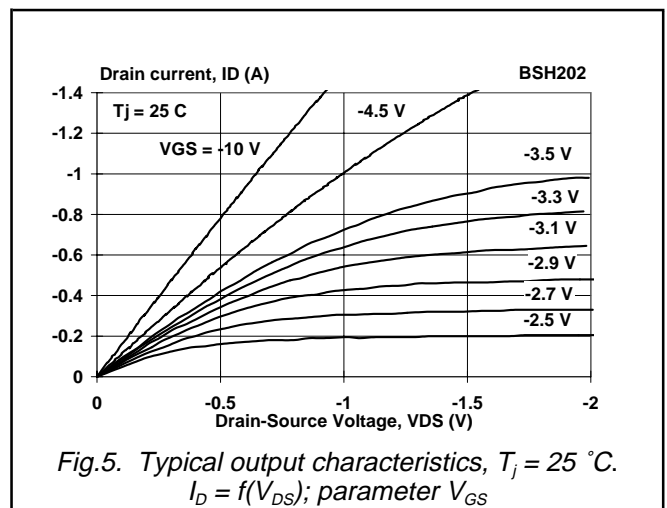
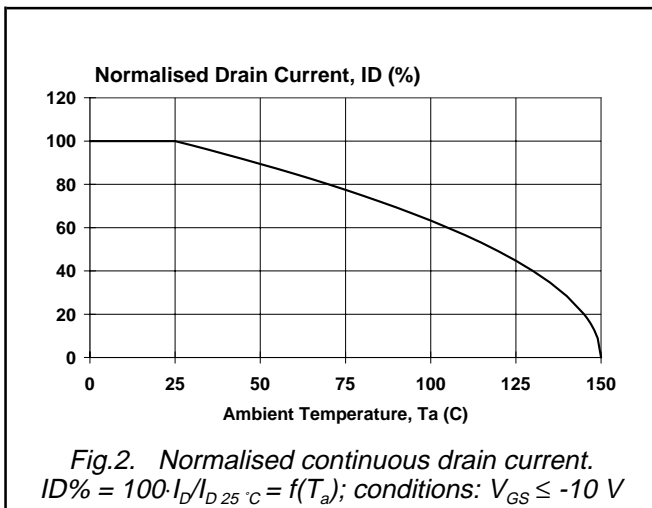
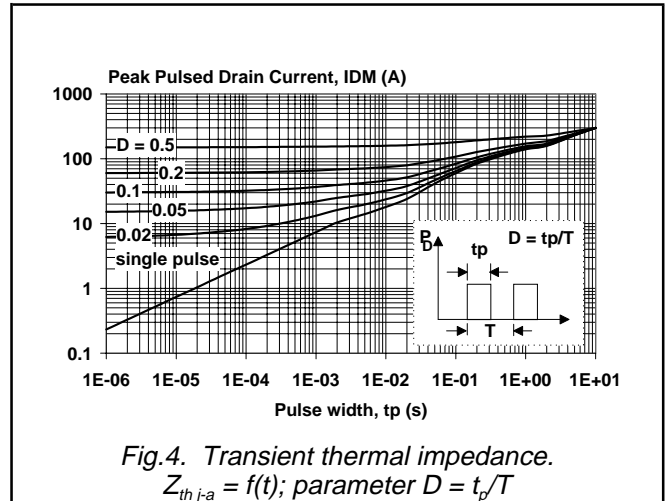
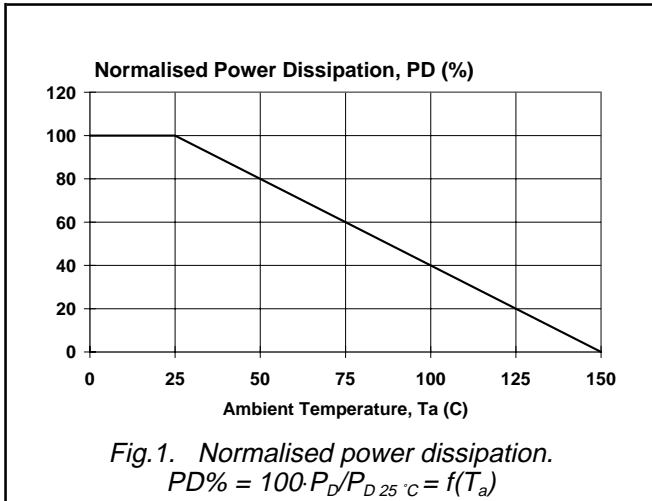
REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	$T_a = 25^\circ\text{C}$	-	-	-0.56	A
I_{DRM}	Pulsed reverse drain current		-	-	-2.2	A
V_{SD}	Diode forward voltage	$I_F = -0.5\ \text{A}; V_{GS} = 0\ \text{V}$	-	-0.87	-1.3	V
t_{rr}	Reverse recovery time	$I_F = -0.5\ \text{A}; -di_F/dt = 100\ \text{A}/\mu\text{s}; V_{GS} = 0\ \text{V}; V_R = -24\ \text{V}$	-	30	-	ns
Q_{rr}	Reverse recovery charge		-	28	-	nC

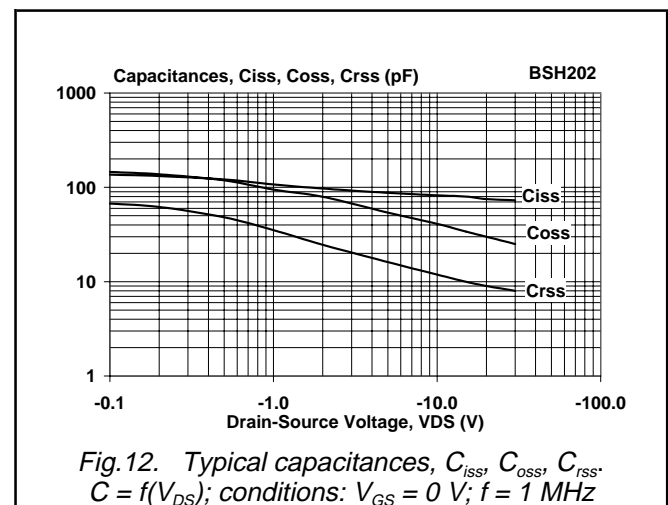
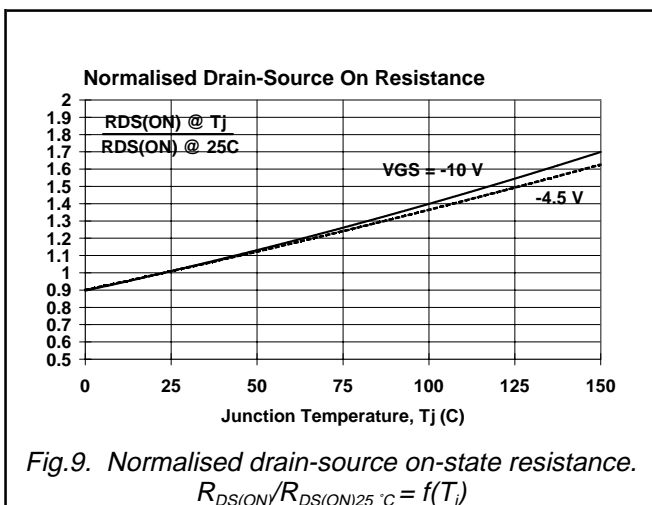
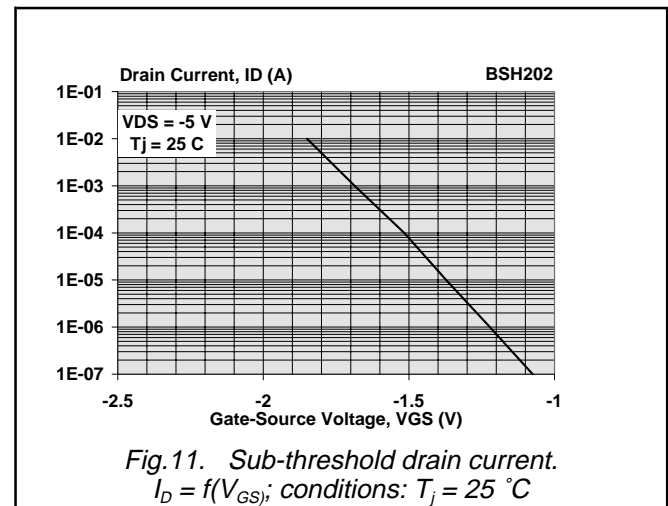
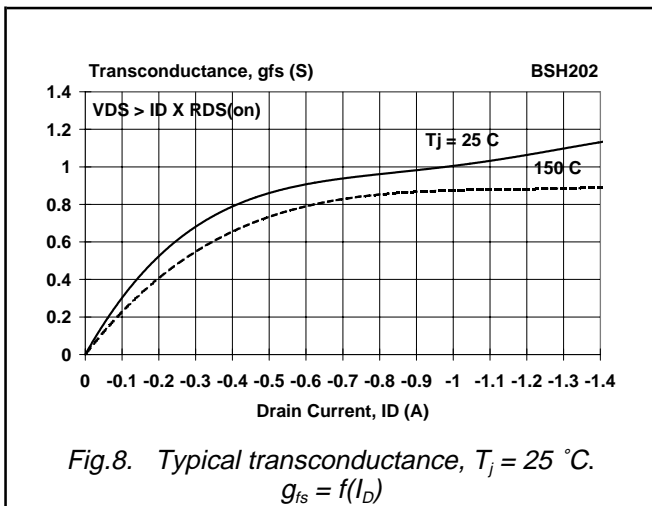
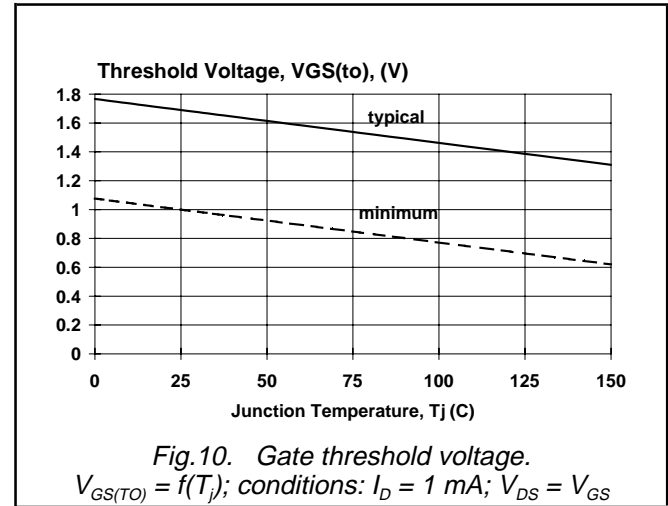
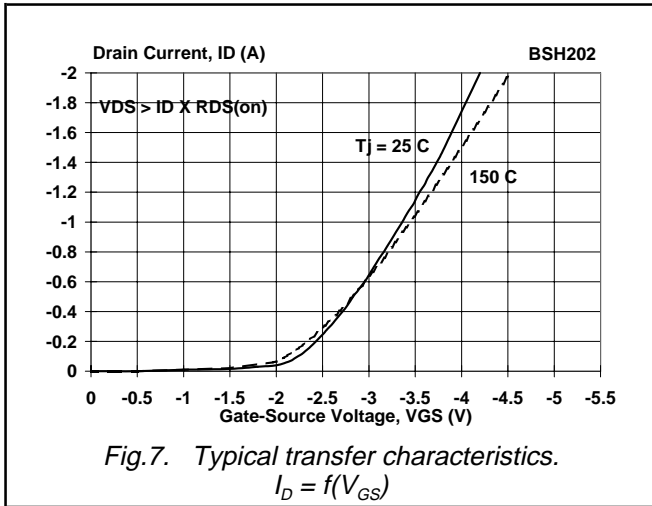
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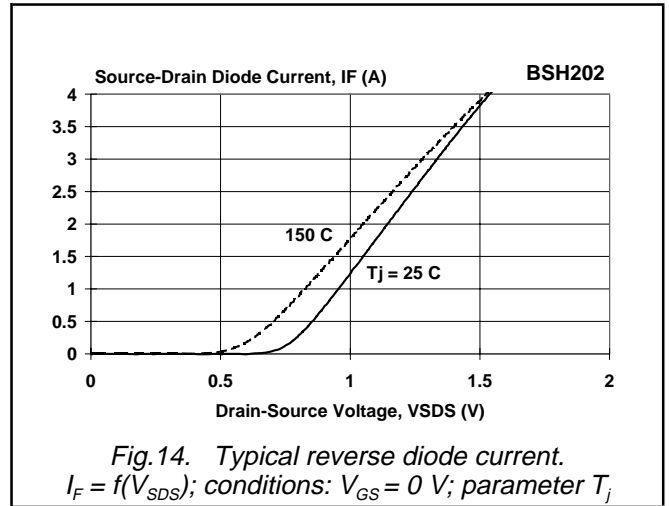
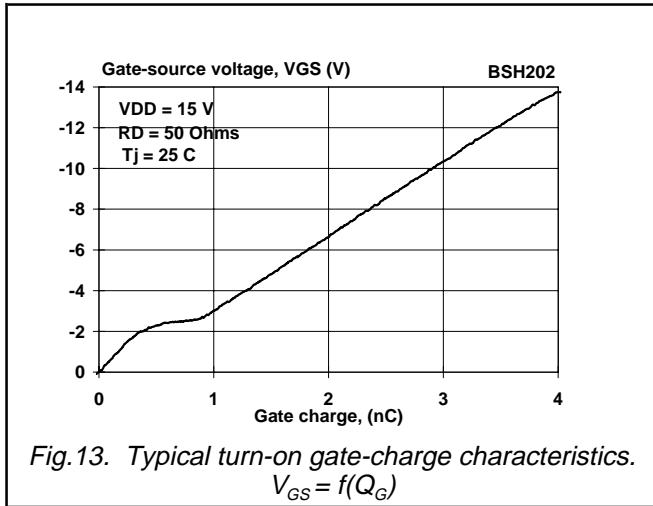
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P-channel enhancement mode
MOS transistor

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P-channel enhancement mode
MOS transistor

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MECHANICAL DATA

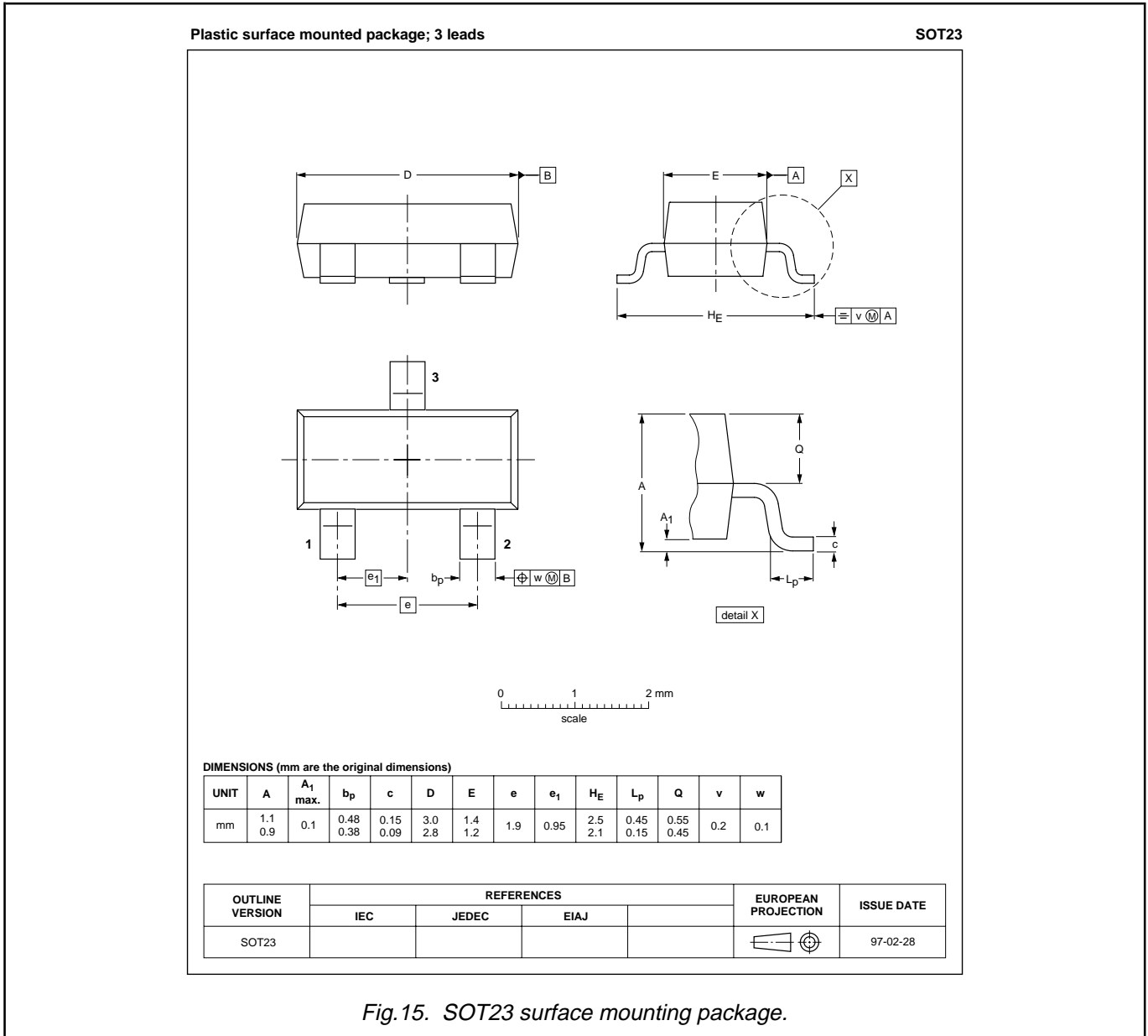


Fig.15. SOT23 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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