

To all our customers

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Renesas Technology Home Page: <http://www.renesas.com>

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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BB101C

Build in Biasing Circuit MOS FET IC UHF RF Amplifier

RENESAS

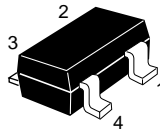
ADE-208-505A (Z)
2nd. Edition
Mar. 2001

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise characteristics;
(NF = 2.0 dB typ. at f = 900 MHz)
- Withstanding to ESD;
Build in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; CMPAK-4(SOT-343mod)

Outline

CMPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

- Notes:
1. Marking is "AU-".
 2. BB101C is individual type number of HITACHI BBFET.

Absolute Maximum Ratings (Ta = 25°C)

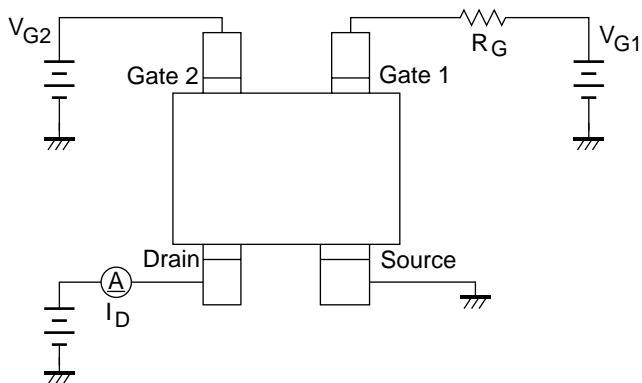
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 - 0	V
Gate2 to source voltage	V_{G2S}	±6	V
Drain current	I_D	25	mA
Channel power dissipation	Pch	100	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Electrical Characteristics (Ta = 25°C)

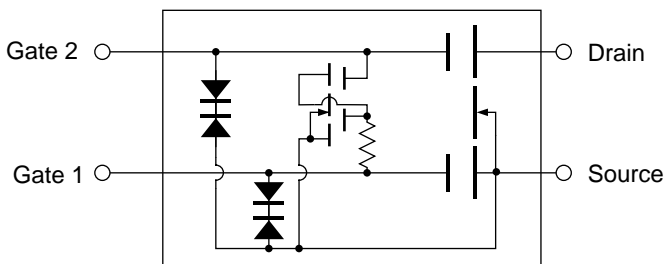
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200\mu A$ $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10\mu A$ $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	±6	—	—	V	$I_{G2} = +10\mu A$ $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5V$ $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	±100	nA	$V_{G2S} = \pm 5V$ $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.2	—	0.8	V	$V_{DS} = 5V, V_{G2S} = 4V$ $I_D = 100\mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.4	—	1.0	V	$V_{DS} = 5V, V_{G1S} = 5V$ $I_D = 100\mu A$
Drain current	$I_{D(op)}$	10	15	20	mA	$V_{DS} = 5V, V_{G1} = 5V$ $V_{G2S} = 4V$ $R_G = 220k\Omega$
Forward transfer admittance	$ y_{fs} $	16	22	—	mS	$V_{DS} = 5V, V_{G1} = 5V$ $V_{G2S} = 4V$ $R_G = 220k\Omega, f = 1kHz$
Input capacitance	C_{iss}	1.2	1.7	2.2	pF	$V_{DS} = 5V, V_{G1} = 5V$
Output capacitance	C_{oss}	0.7	1.1	1.5	pF	$V_{G2S} = 4V, R_G = 220k\Omega$
Reverse transfer capacitance	C_{rss}	—	0.012	0.03	pF	$f = 1MHz$
Power gain	PG	16	20	—	dB	$V_{DS} = 5V, V_{G1} = 5V$ $V_{G2S} = 4V$
Noise figure	NF	—	2.0	3.0	dB	$R_G = 220k\Omega$ $f = 900MHz$

Main Characteristics

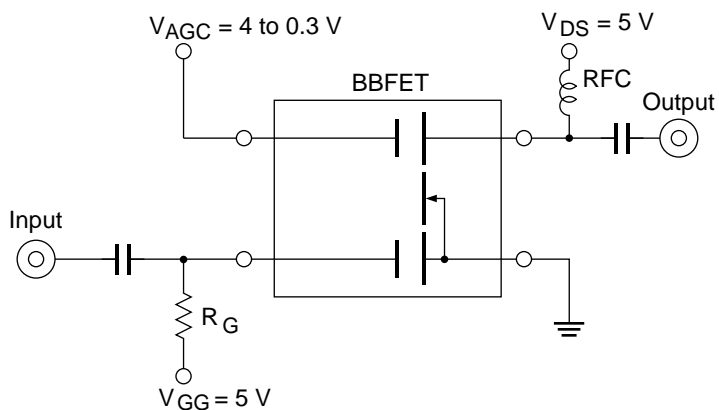
Test Circuit for Operating Items ($b_{(op)}$, $|y_{fs}|$, C_{iss} , C_{oss} , C_{rss} , NF , PG)



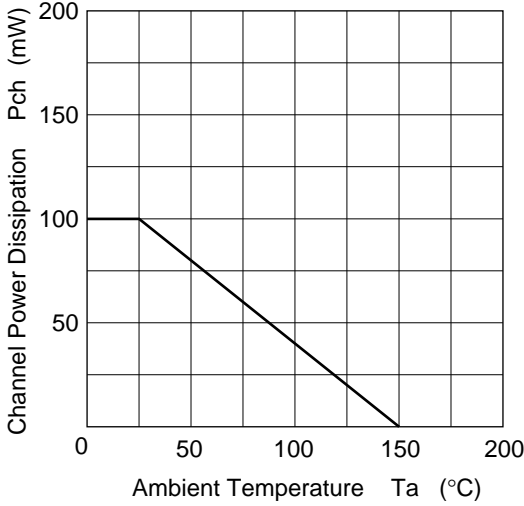
Equivalent Circuit



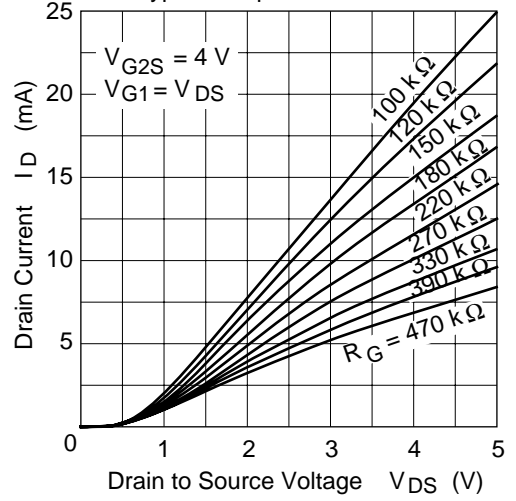
Application Circuit



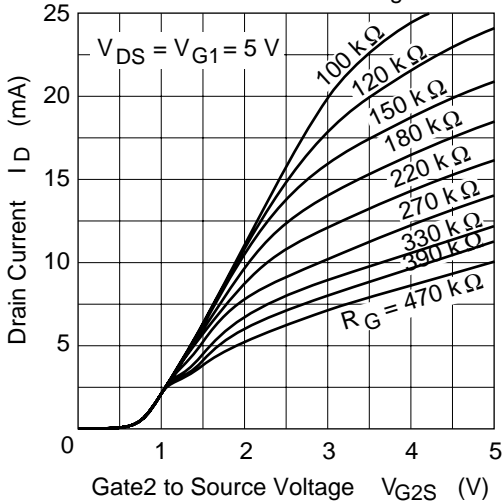
Maximum Channel Power Dissipation Curve



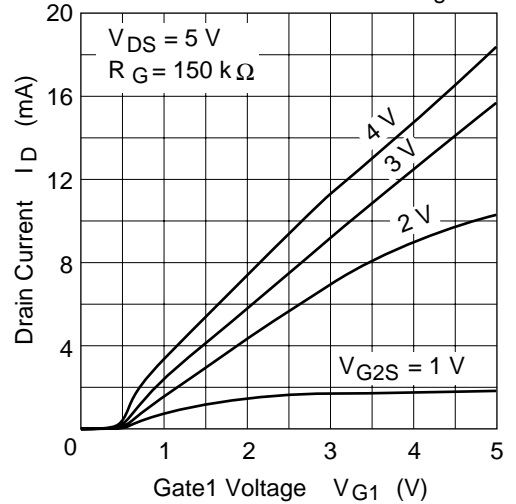
Typical Output Characteristics

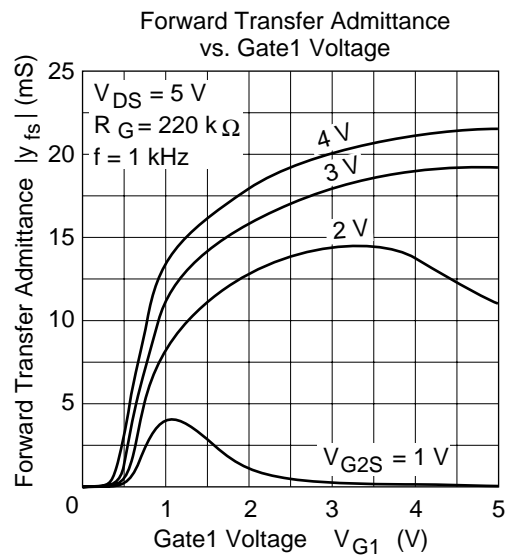
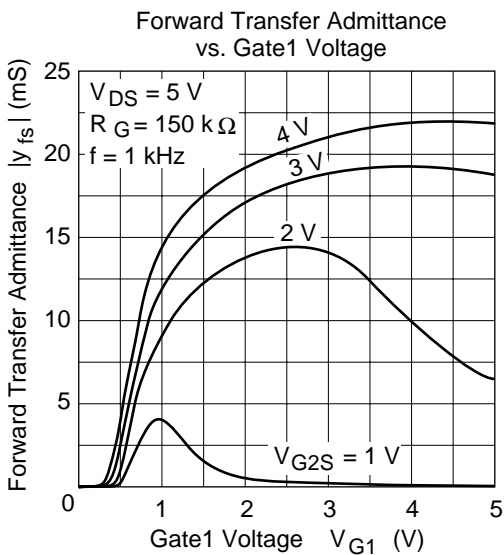
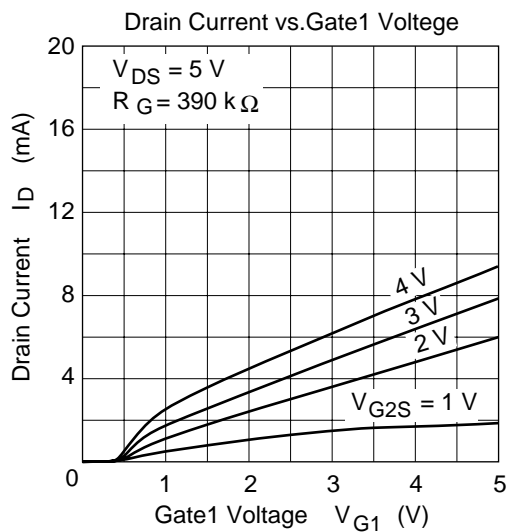
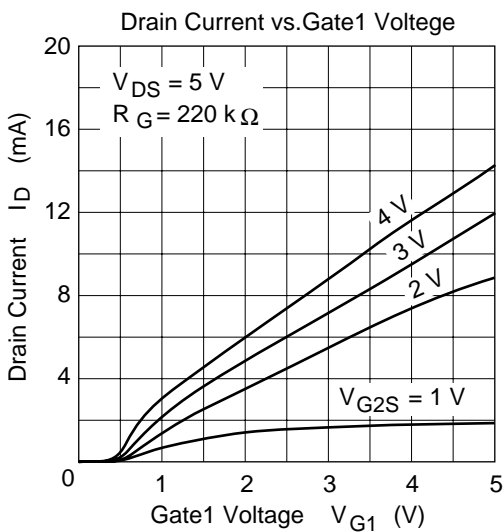


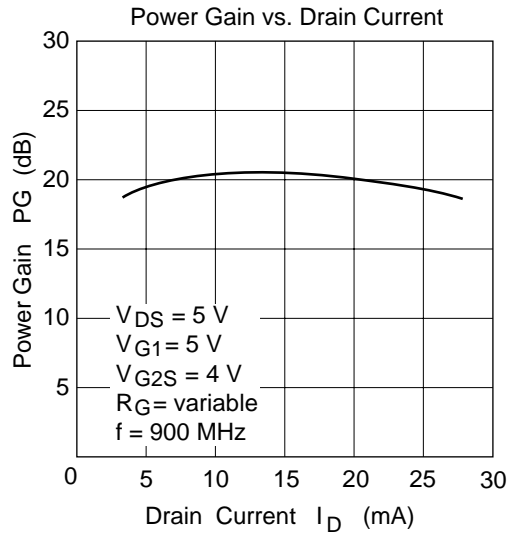
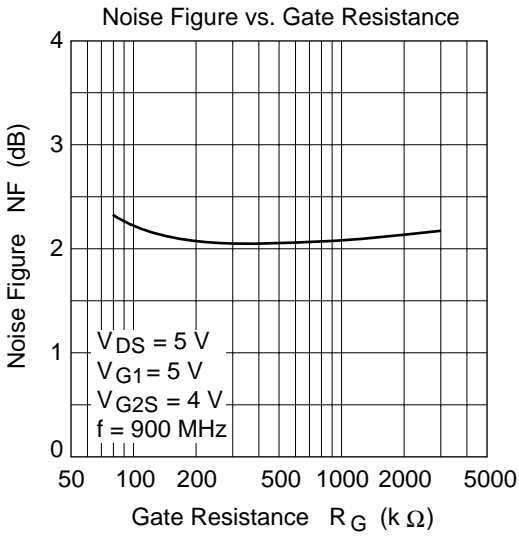
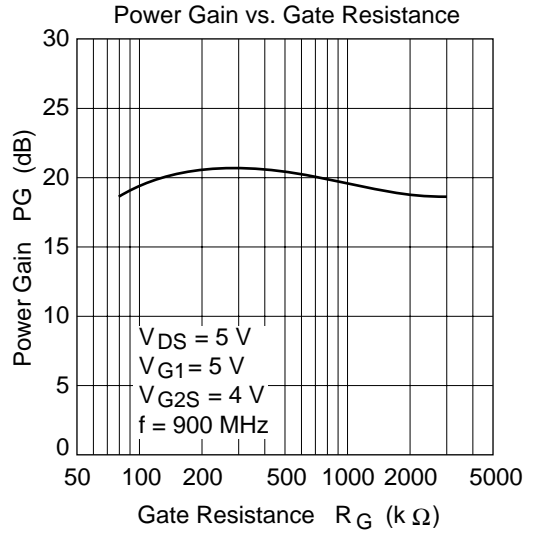
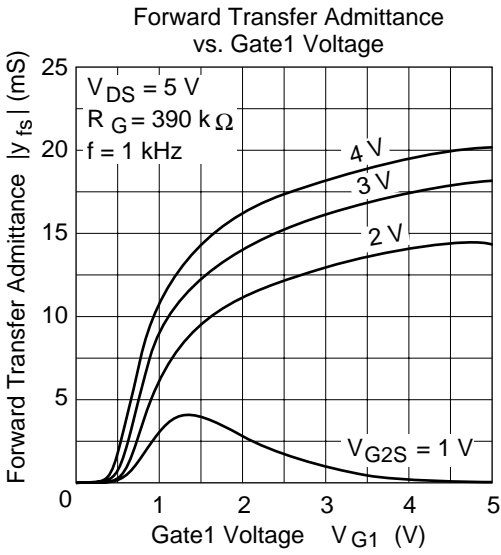
Drain Current vs. Gate2 to Source Voltage

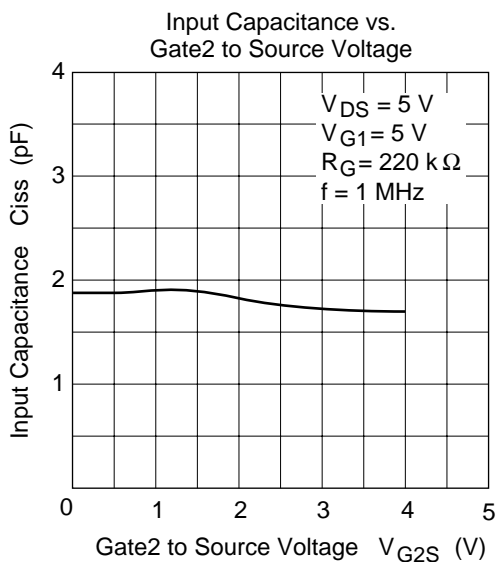
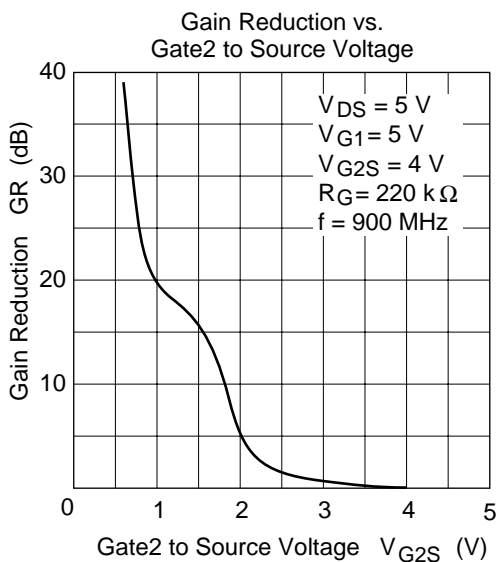
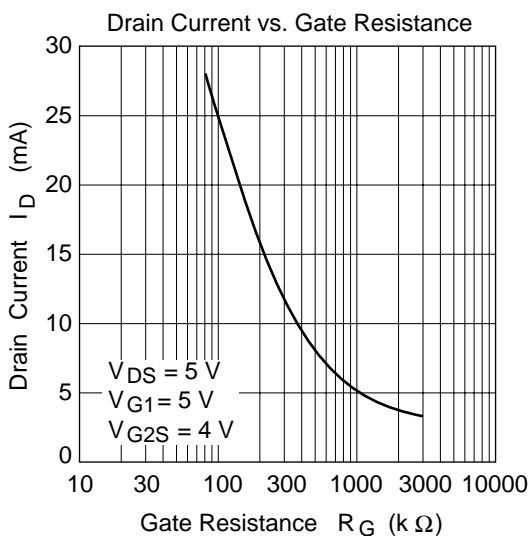
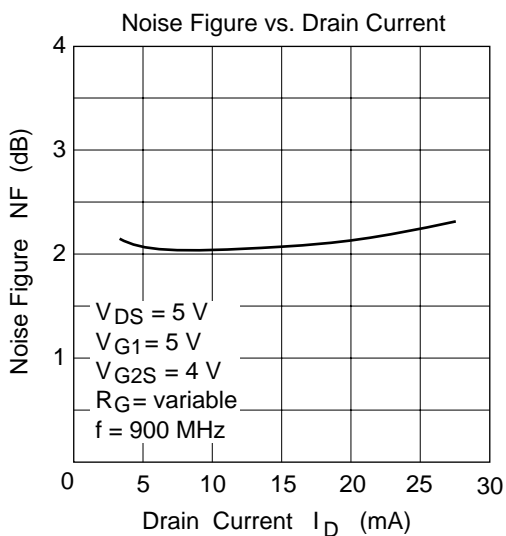


Drain Current vs. Gate1 Voltage

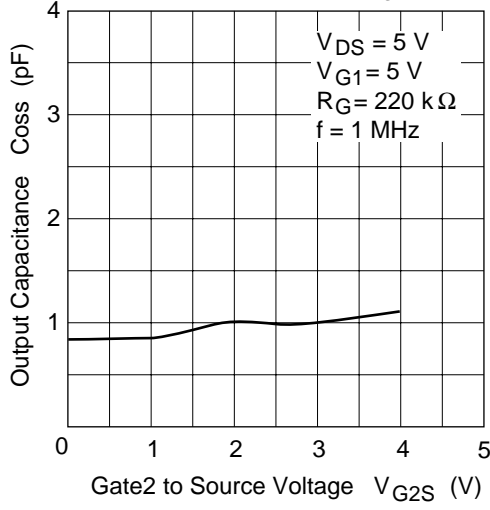








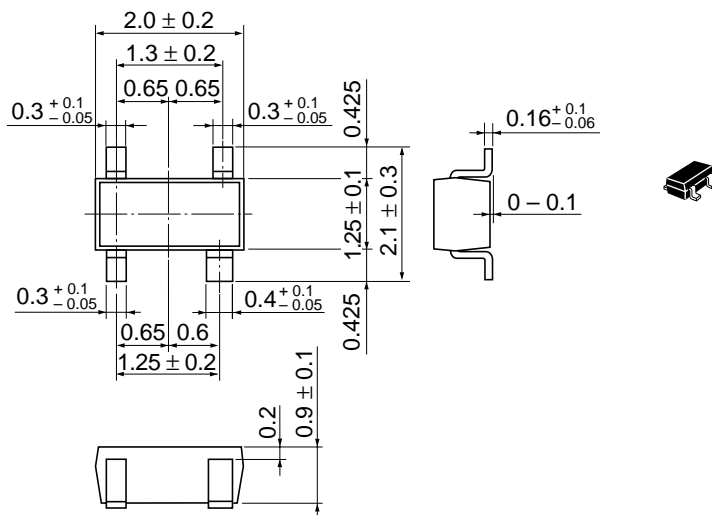
Output Capacitance vs.
Gate2 to Source Voltage



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	CMPAK-4(T)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.006 g

Cautions

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Colophon 2.0



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