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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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BB301M

Build in Biasing Circuit MOS FET IC
VHF RF Amplifier

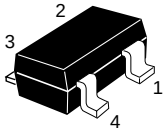
ADE-208-506A (Z)
2nd. Edition
Mar. 2001

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise characteristics;
  (NF = 1.3 dB typ. at f = 200 MHz)
- Withstanding to ESD;
  Build in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; MPAK-4(SOT-143Rmod)

Outline

MPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

Notes: 1. Marking is “AW–”.
2. BB301M is individual type number of HITACHI BBFET.

Absolute Maximum Ratings (Ta = 25°C)

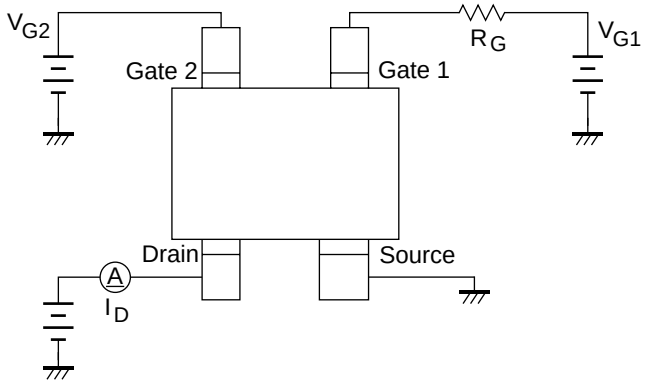
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 – 0	V
Gate2 to source voltage	V_{G2S}	±6	V
Drain current	I_D	25	mA
Channel power dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Electrical Characteristics (Ta = 25°C)

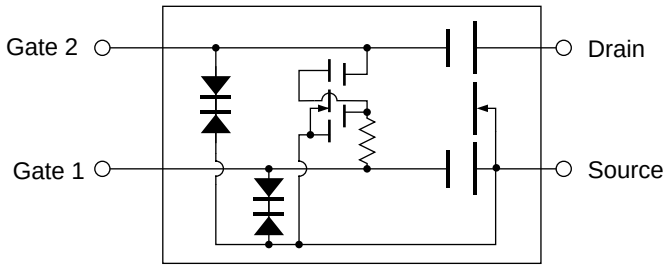
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200µA $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10µA $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	±6	—	—	V	I_{G2} = ±10µA $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5V $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	±100	nA	V_{G2S} = ±5V $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.4	—	1.0	V	V_{DS} = 5V, V_{G2S} = 4V I_D = 100µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.4	—	1.0	V	V_{DS} = 5V, V_{G1S} = 5V I_D = 100µA
Drain current	$I_{D(op)}$	10	15	20	mA	V_{DS} = 5V, V_{G1} = 5V V_{G2S} = 4V R_G = 100kΩ
Forward transfer admittance	$\|y_{fs}\|$	15	20	—	mS	V_{DS} = 5V, V_{G1} = 5V V_{G2S} =4V R_G = 100kΩ, f = 1kHz
Input capacitance	c_{iss}	2.2	3.0	3.9	pF	V_{DS} = 5V, V_{G1} = 5V
Output capacitance	c_{oss}	0.9	1.2	1.6	pF	V_{G2S} =4V, R_G = 100kΩ
Reverse transfer capacitance	c_{rss}	—	0.018	0.04	pF	f = 1MHz
Power gain	PG	22	26	—	dB	V_{DS} = 5V, V_{G1} = 5V V_{G2S} =4V
Noise figure	NF	—	1.3	1.9	dB	R_G = 100kΩ f = 200MHz

Main Characteristics

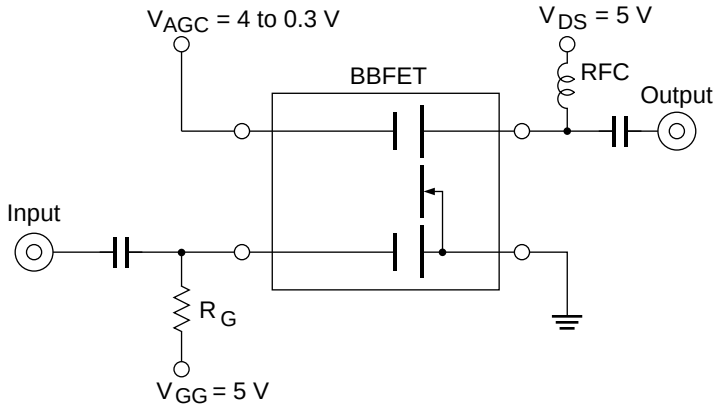
Test Circuit for Operating Items ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)



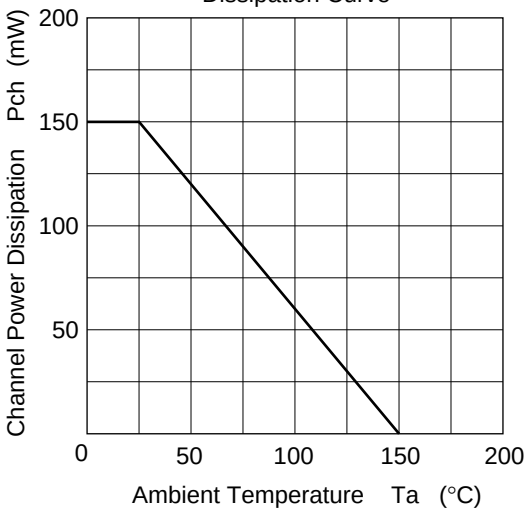
Equivalent Circuit



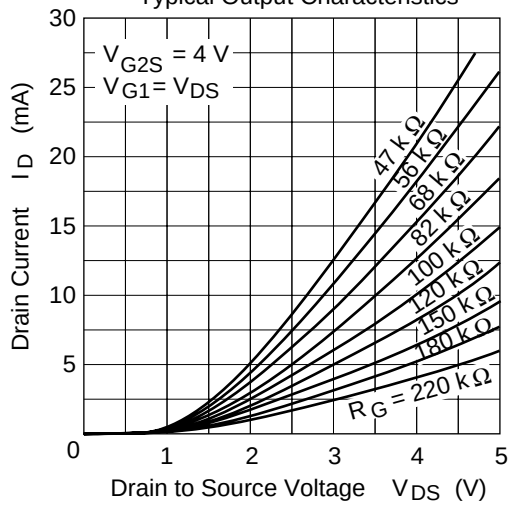
Application Circuit



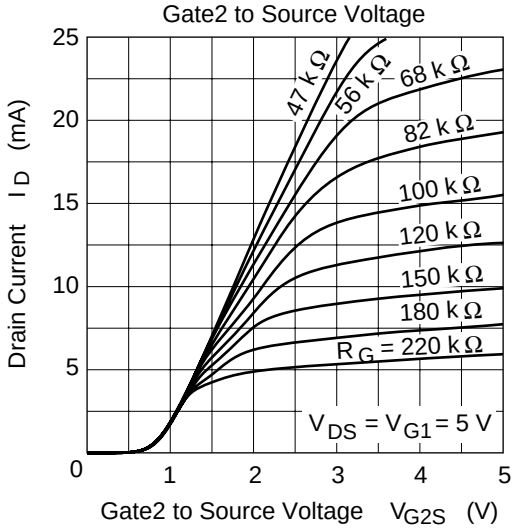
Maximum Channel Power Dissipation Curve



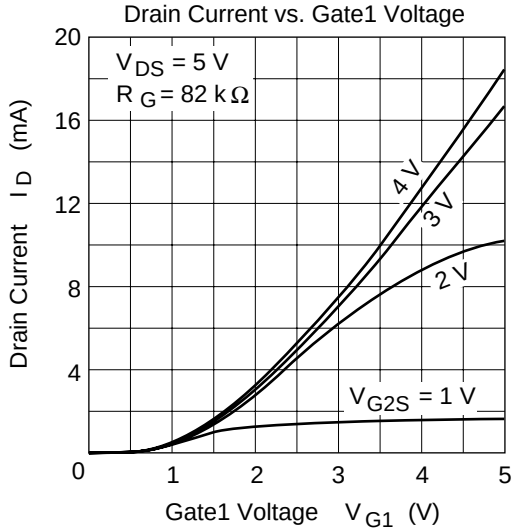
Typical Output Characteristics



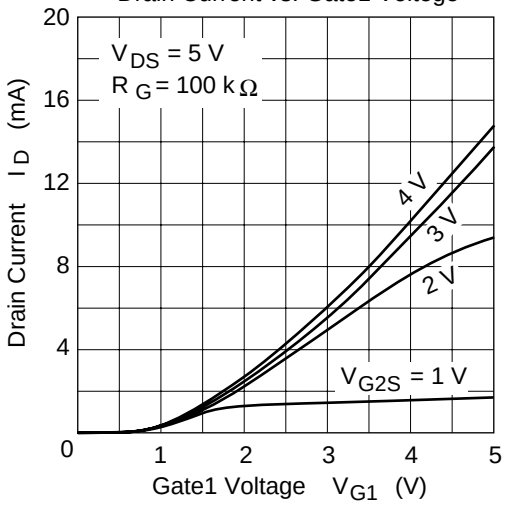
Drain Current vs. Gate2 to Source Voltage



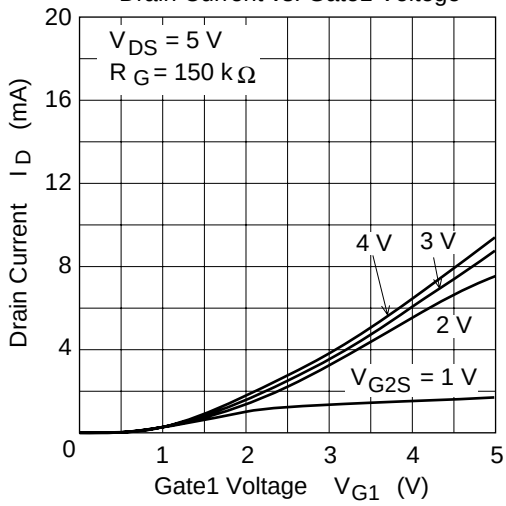
Drain Current vs. Gate1 Voltage



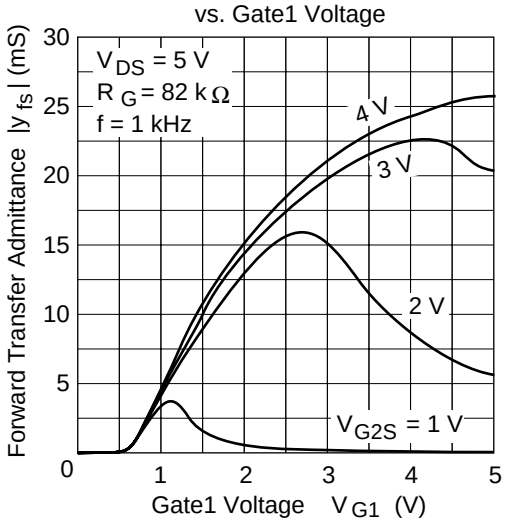
Drain Current vs. Gate1 Voltege



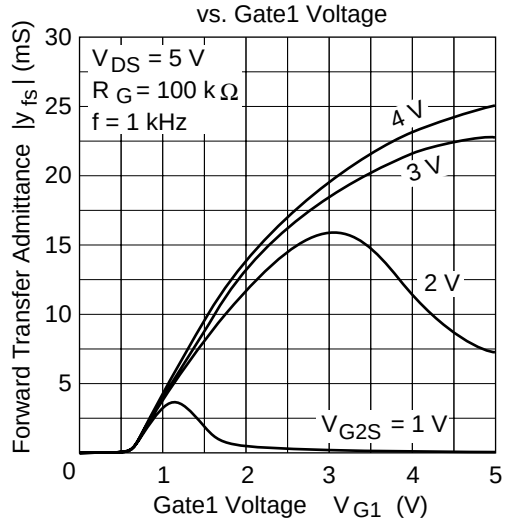
Drain Current vs. Gate1 Voltege



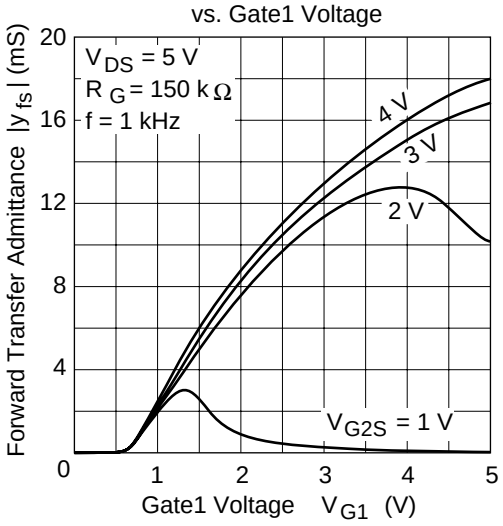
Forward Transfer Admittance vs. Gate1 Voltage



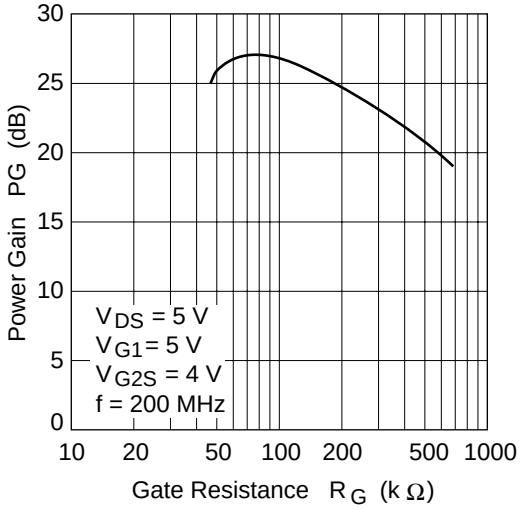
Forward Transfer Admittance vs. Gate1 Voltage



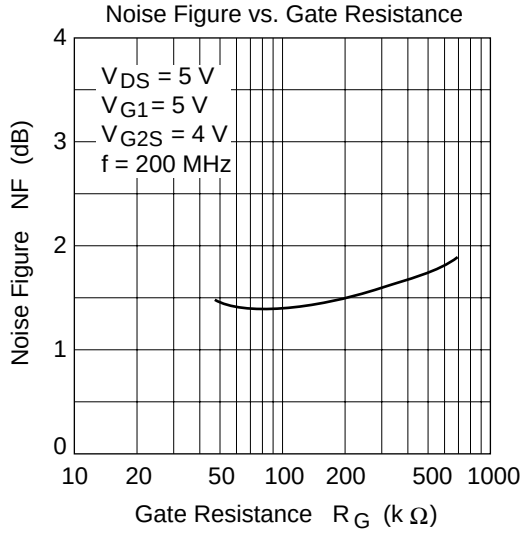
Forward Transfer Admittance vs. Gate1 Voltage



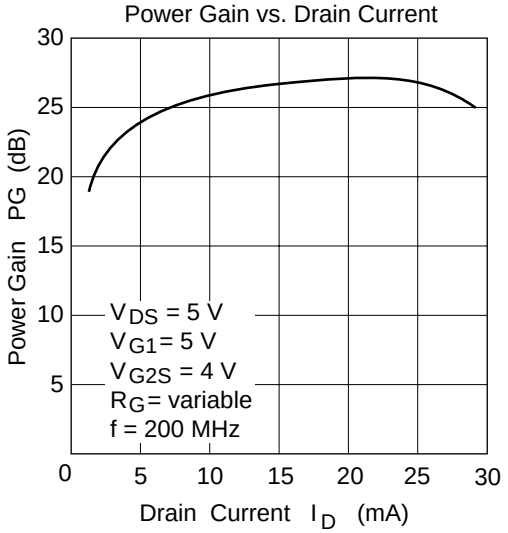
Power Gain vs. Gate Resistance



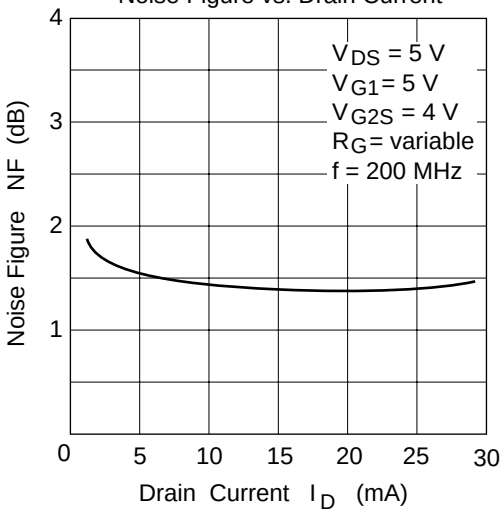
Noise Figure vs. Gate Resistance



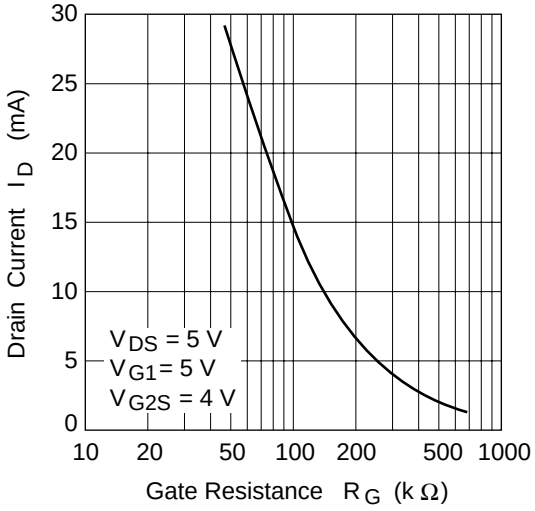
Power Gain vs. Drain Current



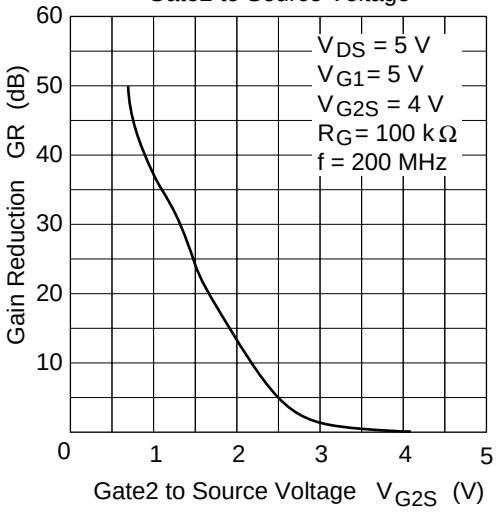
Noise Figure vs. Drain Current



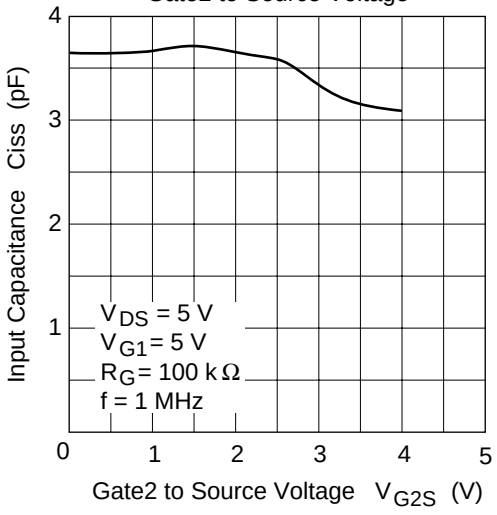
Drain Current vs. Gate Resistance



Gain Reduction vs.
Gate2 to Source Voltage



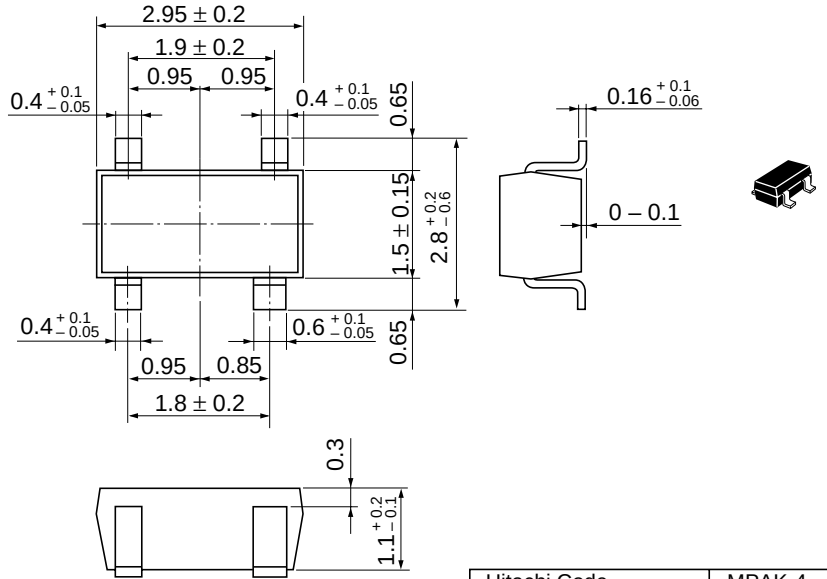
Input Capacitance vs.
Gate2 to Source Voltage



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	MPAK-4
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.013 g

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