To all our customers

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The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

BB302M

Build in Biasing Circuit MOS FET IC
VHF RF Amplifier

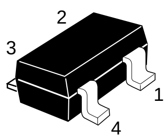
ADE-208-572B(Z)
3rd. Edition
Mar. 2001

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise characteristics;
  (NF = 1.7 dB typ. at f = 200 MHz)
- Withstanding to ESD;
  Build in ESD absorbing diode. Withstand up to 240V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; MPAK-4(SOT-143Rmod)

Outline

MPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

Notes: 1. Marking is “BW –”.
2. BB302M is individual type number of HITACHI BBFET.

Absolute Maximum Ratings (Ta = 25°C)

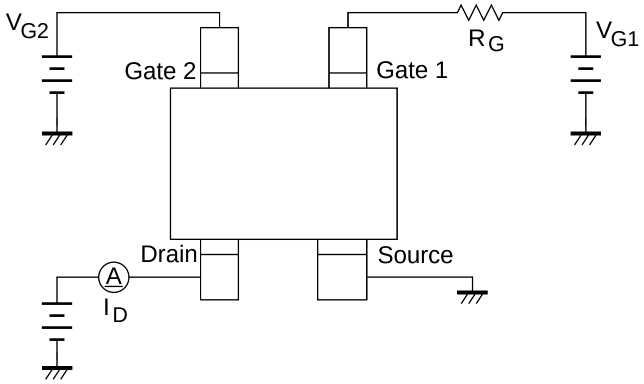
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	12	V
Gate1 to source voltage	V_{G1S}	+10 – 0	V
Gate2 to source voltage	V_{G2S}	±10	V
Drain current	I_D	25	mA
Channel power dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Electrical Characteristics (Ta = 25°C)

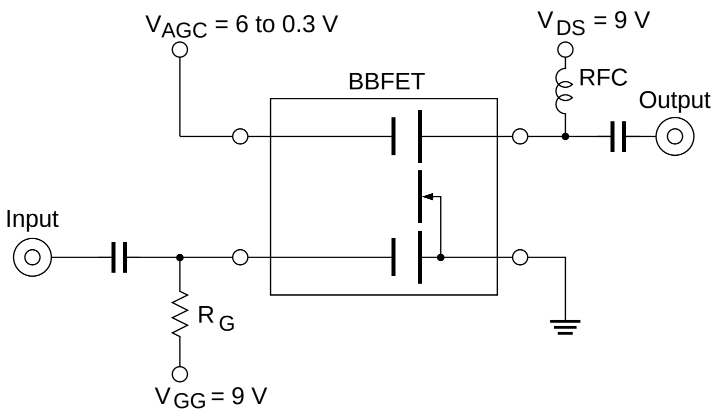
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	12	—	—	V	I_D = 200µA V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+10	—	—	V	I_{G1} = +10µA V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	±10	—	—	V	I_{G2} = ±10µA V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +9V V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	±100	nA	V_{G2S} = ±9V V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.4	—	1.0	V	V_{DS} = 9V, V_{G2S} = 6V I_D = 100µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.4	—	1.0	V	V_{DS} = 9V, V_{G1S} = 9V I_D = 100µA
Drain current	$I_{D(op)}$	9	13	18	mA	V_{DS} = 9V, V_{G1} = 9V V_{G2S} = 6V, R_G = 120kΩ
Forward transfer admittance	$\|y_{fs}\|$	15	20	—	mS	V_{DS} = 9V, V_{G1} = 9V V_{G2S} =6V R_G = 120kΩ, f = 1kHz
Input capacitance	c_{iss}	2.2	3.0	4.0	pF	V_{DS} = 9V, V_{G1} = 9V
Output capacitance	c_{oss}	0.8	1.1	1.5	pF	V_{G2S} =6V, R_G = 120kΩ
Reverse transfer capacitance	c_{rss}	—	0.017	0.04	pF	f = 1MHz
Power gain	PG	22	26	—	dB	V_{DS} = 9V, V_{G1} = 9V V_{G2S} =6V
Noise figure	NF	—	1.7	2.2	dB	R_G = 120kΩ f = 200MHz

Main Characteristics

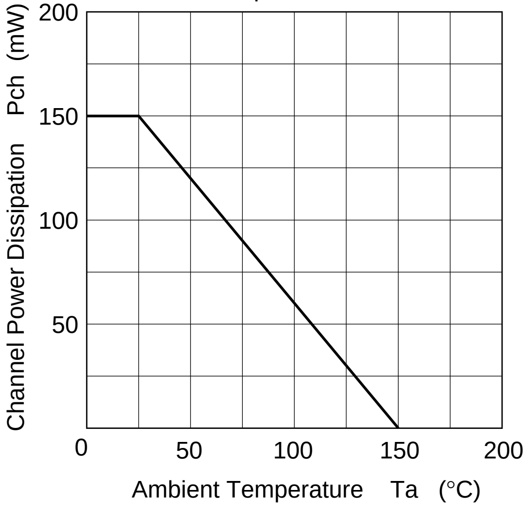
Test Circuit for Operating Items ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)



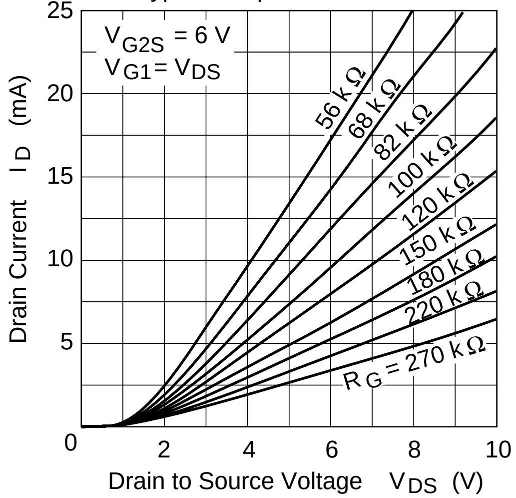
Application Circuit



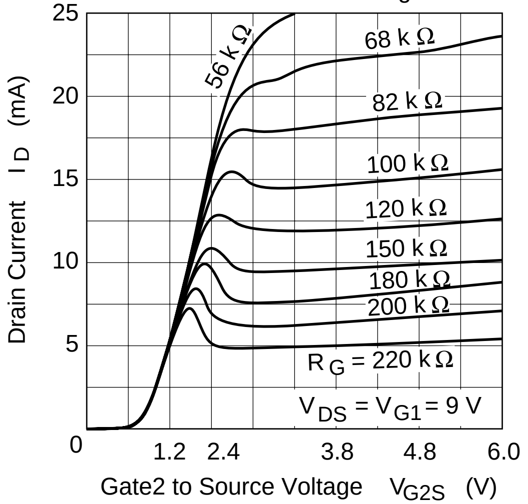
Maximum Channel Power Dissipation Curve



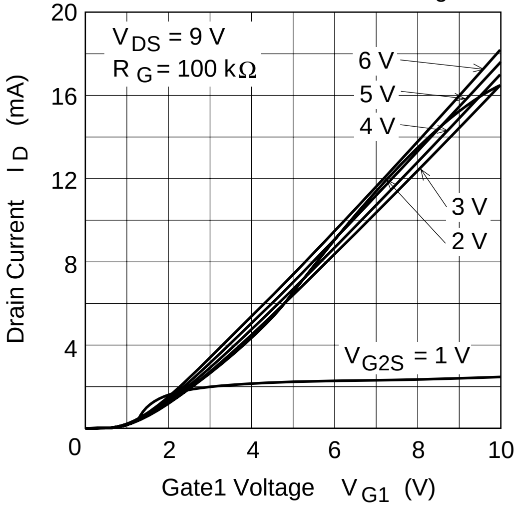
Typical Output Characteristics

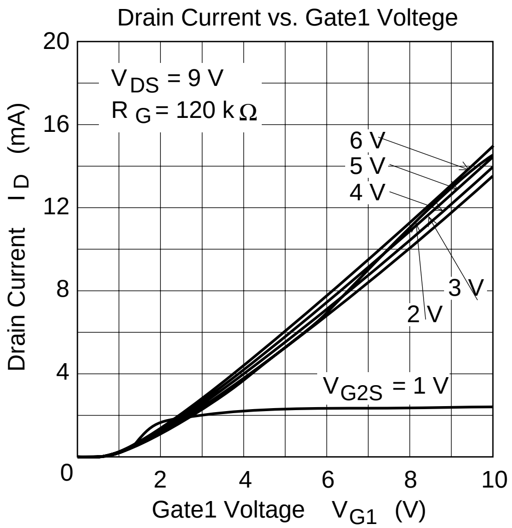


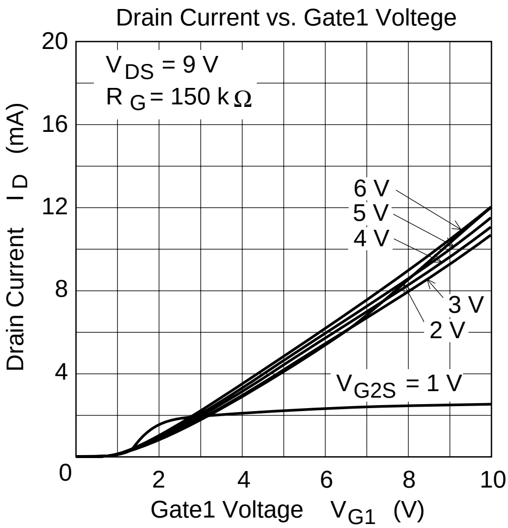
Drain Current vs. Gate2 to Source Voltage

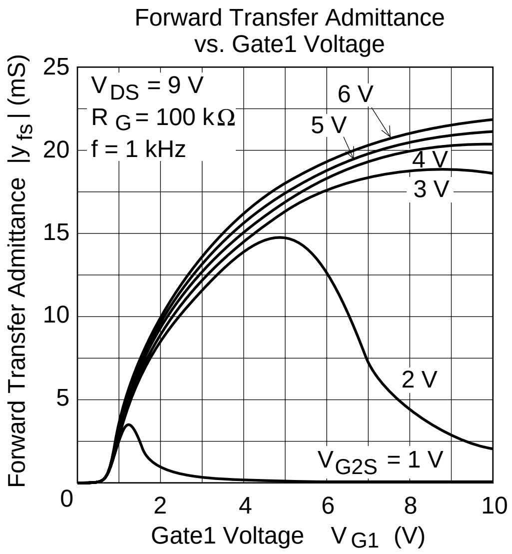


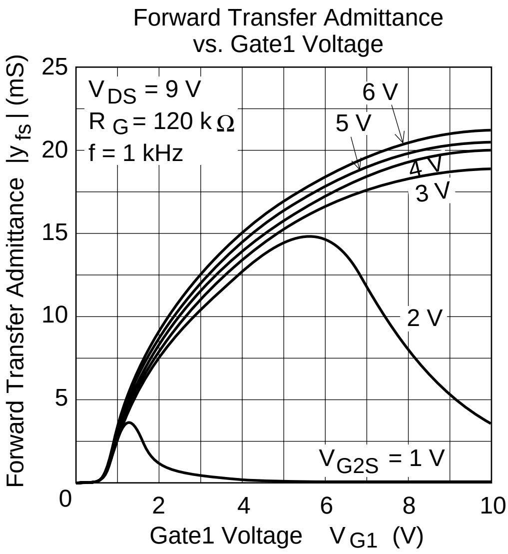
Drain Current vs. Gate1 Voltage

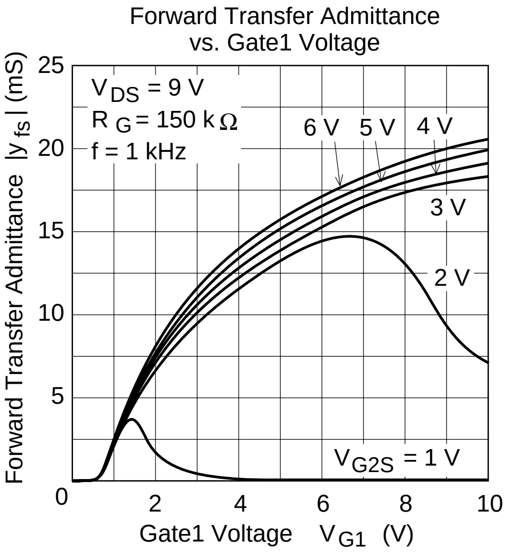


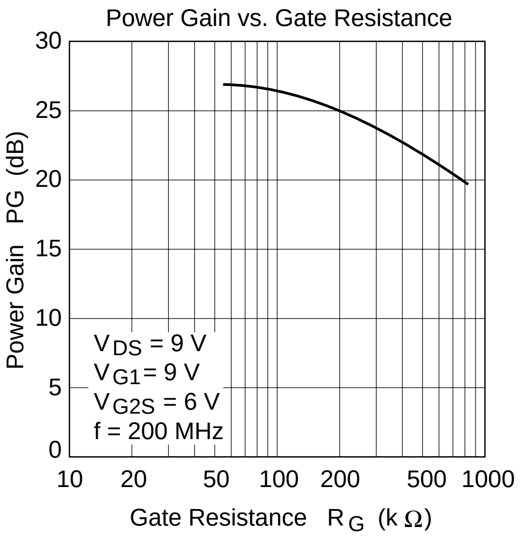

Drain Current vs. Gate1 Voltege
V_{DS} = 9 V
R_G = 120 kΩ
6 V
5 V
4 V
3 V
2 V
V_{G2S} = 1 V
Drain Current I D (mA)
Gate1 Voltage V_{G1} (V)
0
2
4
6
8
10
12
16
20

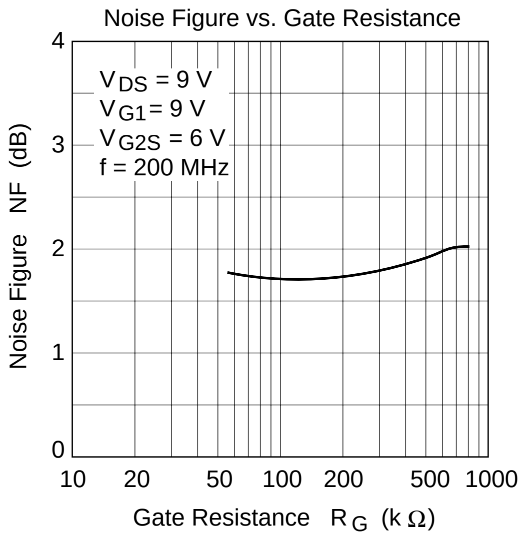

Drain Current vs. Gate1 Voltege
V_{DS} = 9 V
R_G = 150 kΩ
6 V
5 V
4 V
3 V
2 V
V_{G2S} = 1 V
Drain Current I D (mA)
Gate1 Voltage V_{G1} (V)
0
2
4
6
8
10
12
16
20

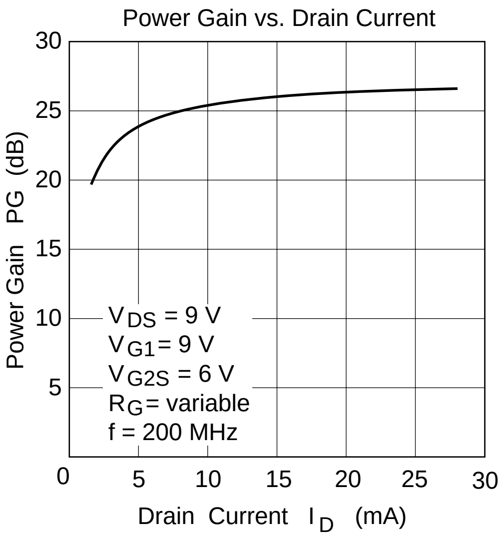

Forward Transfer Admittance
vs. Gate1 Voltage
V_{DS} = 9 V
R_G = 100 kΩ
f = 1 kHz
6 V
5 V
4 V
3 V
2 V
V_{G2S} = 1 V
Forward Transfer Admittance $|y_{fs}|$ (mS)
Gate1 Voltage V_{G1} (V)
0
5
10
15
20
25
2
4
6
8
10

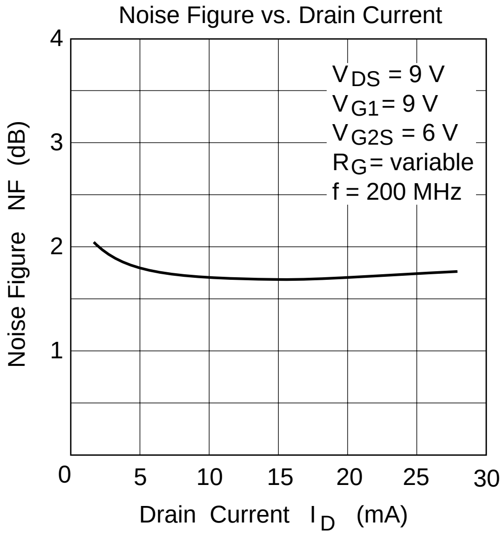

Forward Transfer Admittance
vs. Gate1 Voltage
V_{DS} = 9 V
R_G = 120 kΩ
f = 1 kHz
6 V
5 V
4 V
3 V
2 V
V_{G2S} = 1 V
Forward Transfer Admittance $|y_{fs}|$ (mS)
Gate1 Voltage V_{G1} (V)
0
5
10
15
20
25
2
4
6
8
10

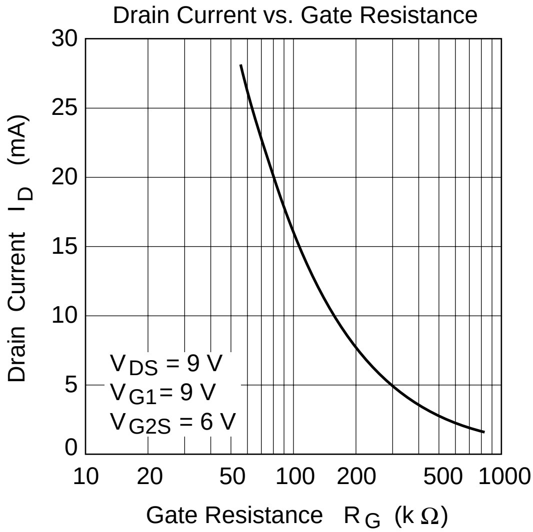

Forward Transfer Admittance vs. Gate1 Voltage
V DS = 9 V
R G = 150 kΩ
f = 1 kHz
6 V 5 V 4 V
3 V
2 V
V G2S = 1 V
Forward Transfer Admittance |y fs| (mS)
25
20
15
10
5
0
2
4
6
8
10
Gate1 Voltage V G1 (V)

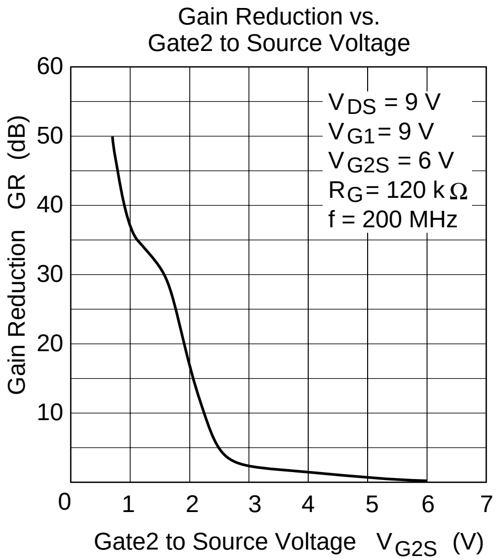

Power Gain vs. Gate Resistance
V DS = 9 V
V G1 = 9 V
V G2S = 6 V
f = 200 MHz
Power Gain PG (dB)
30
25
20
15
10
5
0
10
20
50
100
200
500
1000
Gate Resistance R G (kΩ)

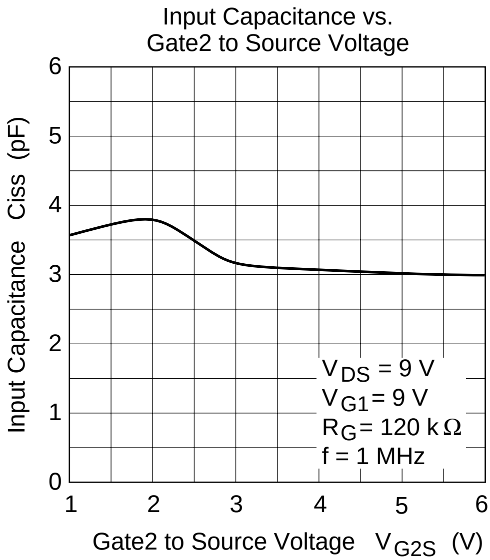

Noise Figure vs. Gate Resistance
V DS = 9 V
V G1 = 9 V
V G2S = 6 V
f = 200 MHz
Noise Figure NF (dB)
4
3
2
1
0
10
20
50
100
200
500
1000
Gate Resistance R G (kΩ)


Power Gain vs. Drain Current
V DS = 9 V
V G1 = 9 V
V G2S = 6 V
R G = variable
f = 200 MHz
Power Gain PG (dB)
30
25
20
15
10
5
0
5
10
15
20
25
30
Drain Current I D (mA)

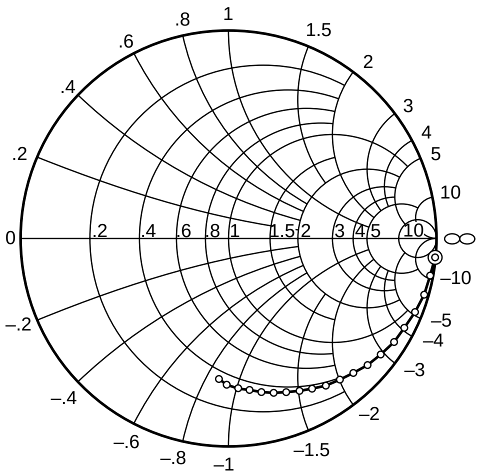

Noise Figure vs. Drain Current
Noise Figure NF (dB)
Drain Current I_D (mA)
V_DS = 9 V
V_G1 = 9 V
V_G2S = 6 V
R_G = variable
f = 200 MHz
0 5 10 15 20 25 30
1 2 3 4


Drain Current vs. Gate Resistance
Drain Current I_D (mA)
Gate Resistance R_G (k Ω)
V_DS = 9 V
V_G1 = 9 V
V_G2S = 6 V
10 20 50 100 200 500 1000
0 5 10 15 20 25 30


Gain Reduction vs.
Gate2 to Source Voltage
Gain Reduction GR (dB)
Gate2 to Source Voltage V_G2S (V)
V_DS = 9 V
V_G1 = 9 V
V_G2S = 6 V
R_G = 120 k Ω
f = 200 MHz
0 1 2 3 4 5 6 7
10 20 30 40 50 60

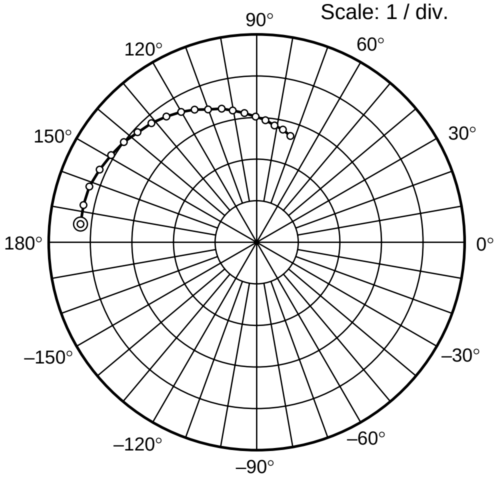

Input Capacitance vs.
Gate2 to Source Voltage
Input Capacitance Ciss (pF)
Gate2 to Source Voltage V_G2S (V)
V_DS = 9 V
V_G1 = 9 V
R_G = 120 k Ω
f = 1 MHz
1 2 3 4 5 6
0 1 2 3 4 5 6

S11 Parameter vs. Frequency



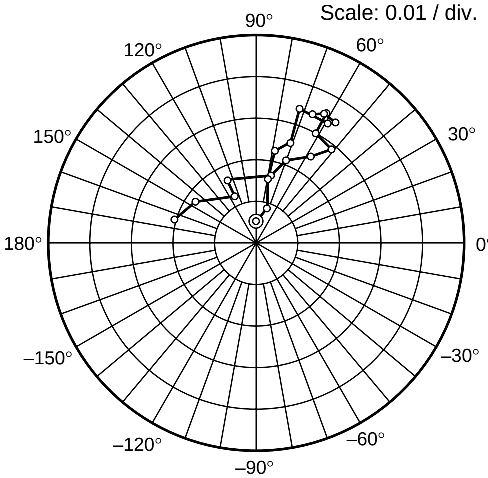
Test Condition : V_{DS} = 9 V , V_{G1} = 9 V
V_{G2S} = 6 V , R_G = 120 kΩ
50 to 1000 MHz (50 MHz step)

S21 Parameter vs. Frequency



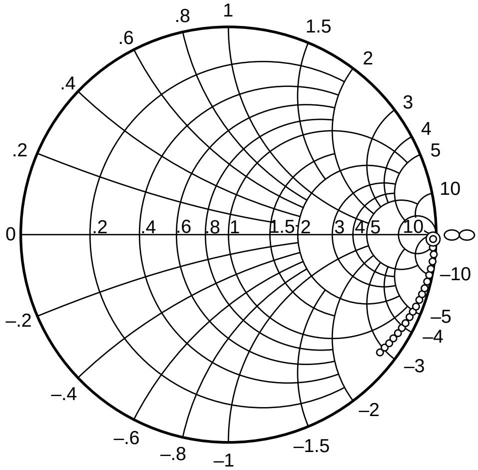
Test Condition : V_{DS} = 9 V , V_{G1} = 9 V
V_{G2S} = 6 V , R_G = 120 kΩ
50 to 1000 MHz (50 MHz step)

S12 Parameter vs. Frequency



Test Condition : V_{DS} = 9 V , V_{G1} = 9 V
V_{G2S} = 6 V , R_G = 120 kΩ
50 to 1000 MHz (50 MHz step)

S22 Parameter vs. Frequency



Test Condition : V_{DS} = 9 V , V_{G1} = 9 V
V_{G2S} = 6 V , R_G = 120 kΩ
50 to 1000 MHz (50 MHz step)

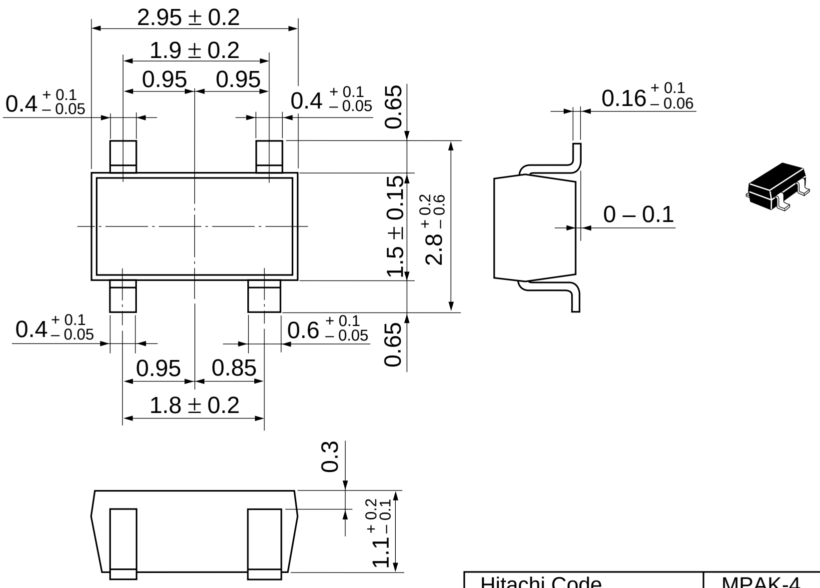
Sparameter (V_{DS} = V_{G1} = 9V, V_{G2S} = 6V, R_G = 120kΩ, Zo = 50Ω)

	S11		S21		S12		S22	
f (MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	0.988	–5.2	2.13	174.1	0.00052	90.0	0.985	–1.3
100	0.986	–10.4	2.13	167.9	0.00087	72.5	0.993	–3.6
150	0.979	–16.0	2.12	161.6	0.00156	79.4	0.992	–5.5
200	0.964	–21.5	2.08	155.2	0.00226	78.4	0.990	–7.5
250	0.948	–26.9	2.04	149.1	0.00254	71.0	0.987	–9.6
300	0.939	–32.0	2.00	143.0	0.00339	72.0	0.985	–11.4
350	0.920	–37.3	1.95	137.3	0.00335	59.0	0.982	–13.3
400	0.904	–42.3	1.91	131.5	0.00338	66.3	0.978	–15.3
450	0.885	–47.1	1.86	125.7	0.00351	62.2	0.974	–17.1
500	0.864	–51.7	1.81	120.1	0.00347	56.6	0.970	–18.9
550	0.848	–56.5	1.76	115.1	0.00355	61.5	0.966	–21.0
600	0.826	–60.9	1.70	110.1	0.00300	61.4	0.961	–22.7
650	0.808	–65.0	1.66	104.7	0.00289	51.1	0.957	–24.5
700	0.789	–69.4	1.61	100.3	0.00246	57.6	0.952	–26.6
750	0.773	–73.7	1.56	95.4	0.00211	70.0	0.947	–28.3
800	0.755	–77.9	1.51	90.5	0.00166	77.5	0.943	–30.2
850	0.735	–82.1	1.47	85.9	0.00165	114.5	0.937	–32.2
900	0.721	–86.3	1.42	81.3	0.00123	114.5	0.933	–34.1
950	0.703	–90.7	1.39	76.9	0.00176	145.8	0.927	–35.9
1000	0.677	–93.9	1.34	72.4	0.00204	164.0	0.923	–37.9

Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	MPAK-4
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.013 g

Cautions

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