To all our customers

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Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

BB501C

Build in Biasing Circuit MOS FET IC
UHF RF Amplifier

RENESAS

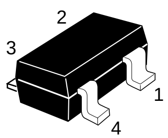
ADE-208-701D (Z)
5th. Edition
Mar. 2001

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- High gain;
  PG = 21.5 dB typ. at f = 900 MHz
- Low noise;
  NF = 1.85 dB typ. at f = 900 MHz
- Withstanding to ESD;
  Build in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; CMPAK-4(SOT-343mod)

Outline

CMPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

Notes: 1. Marking is “AS –”.
2. BB501C is individual type number of HITACHI BBFET.

Absolute Maximum Ratings (Ta = 25°C)

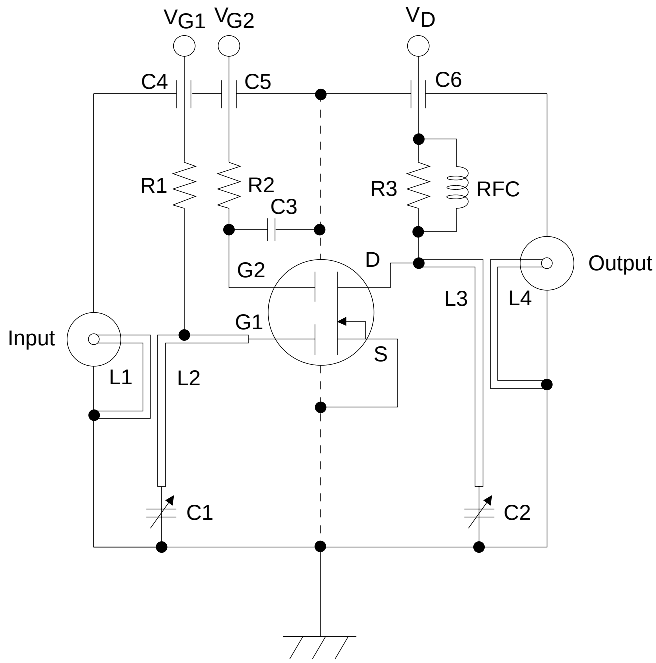
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 – 0	V
Gate2 to source voltage	V_{G2S}	+6 – 0	V
Drain current	I_D	20	mA
Channel power dissipation	Pch	100	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200µA $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10µA $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10µA $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5V $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5V $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.7	1.0	V	V_{DS} = 5V, V_{G2S} = 4V I_D = 100µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.7	1.0	V	V_{DS} = 5V, V_{G1S} = 5V I_D = 100µA
Drain current	$I_{D(op)}$	7	10	13	mA	V_{DS} = 5V, V_{G1} = 5V V_{G2S} = 4V, R_G = 47kΩ
Forward transfer admittance	$\|y_{fs}\|$	19	24	29	mS	V_{DS} = 5V, V_{G1} = 5V V_{G2S} =4V R_G = 47kΩ, f = 1kHz
Input capacitance	c_{iss}	1.4	1.7	2.0	pF	V_{DS} = 5V, V_{G1} = 5V
Output capacitance	c_{oss}	0.7	1.1	1.5	pF	V_{G2S} =4V, R_G = 47kΩ
Reverse transfer capacitance	c_{rss}	—	0.019	0.04	pF	f = 1MHz
Power gain	PG	17	21.5	—	dB	V_{DS} = 5V, V_{G1} = 5V V_{G2S} =4V, R_G = 47kΩ
Noise figure	NF	—	1.85	2.4	dB	f = 900MHz

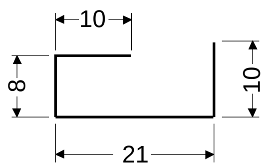
Main Characteristics

900MHz Power Gain, Noise Figure Test Circuit

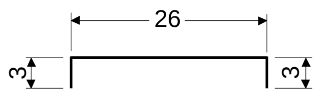


C1, C2 :	Variable Capacitor (10pF MAX)
C3 :	Disk Capacitor (1000pF)
C4 to C6 :	Air Capacitor (1000pF)
R1 :	47 kΩ
R2 :	47 kΩ
R3 :	4.7 kΩ

L1 :

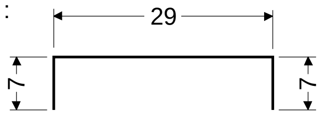


L2 :

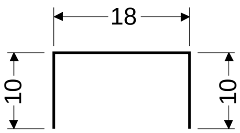


(ϕ1mm Copper wire)
Unit : mm

L3 :

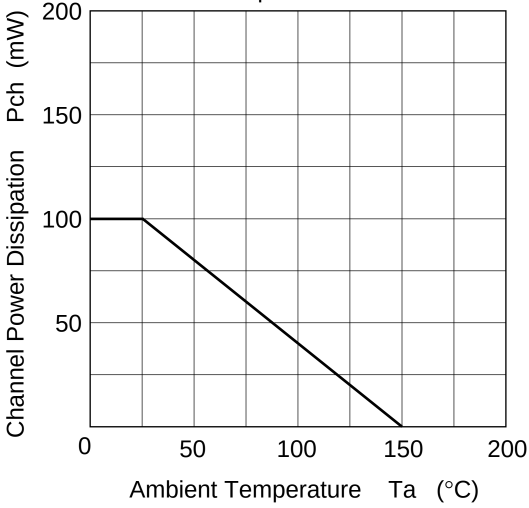


L4 :

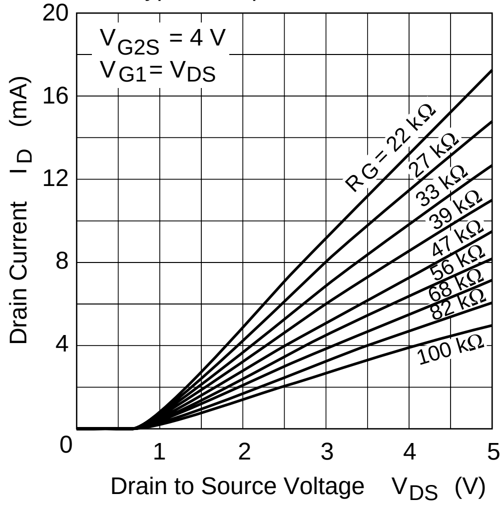


RFC : ϕ1mm Copper wire with enamel 4turns inside dia 6mm

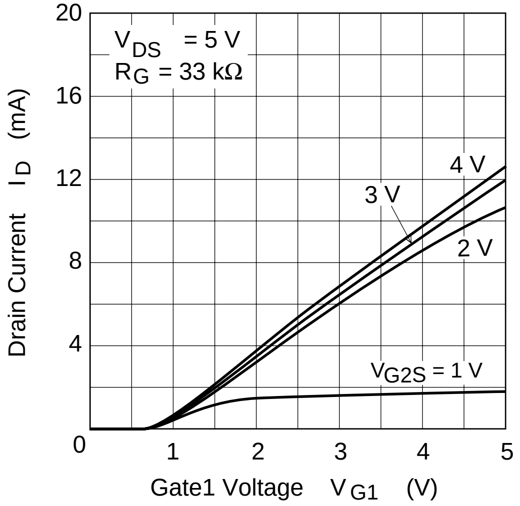
Maximum Channel Power Dissipation Curve



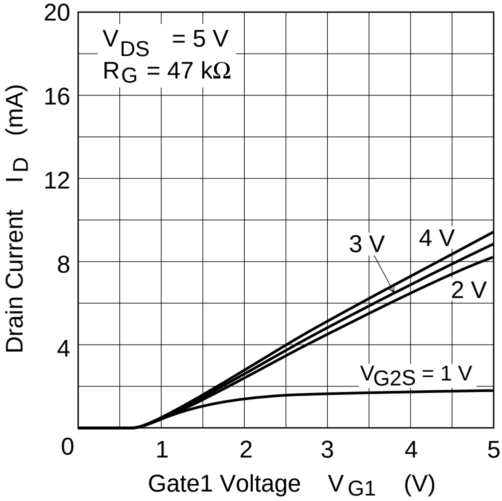
Typical Output Characteristics



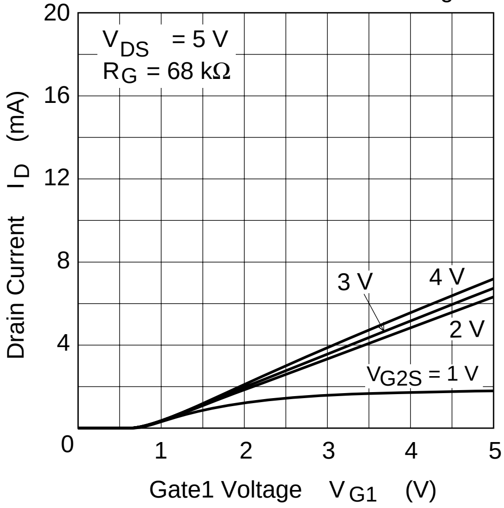
Drain Current vs. Gate1 Voltage



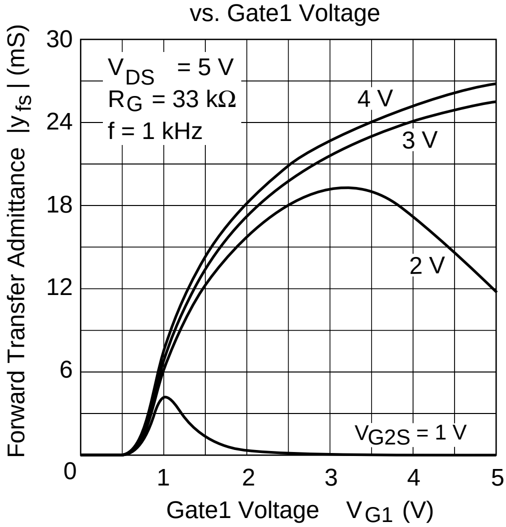
Drain Current vs. Gate1 Voltage



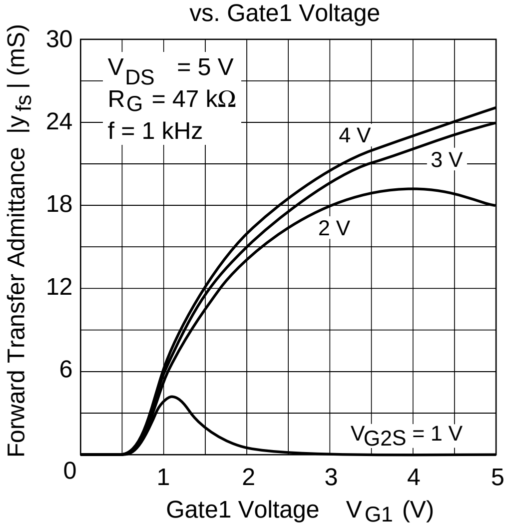
Drain Current vs. Gate1 Voltage



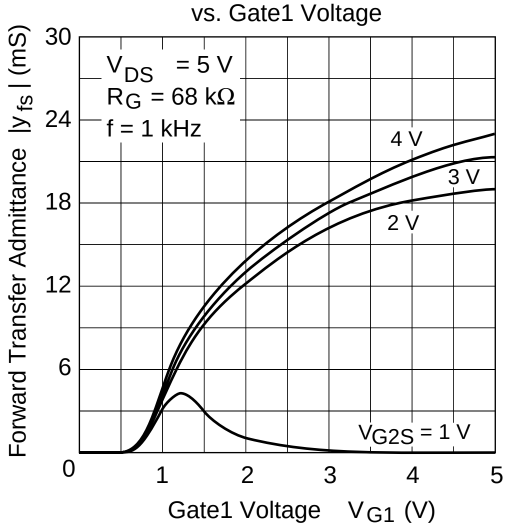
Forward Transfer Admittance vs. Gate1 Voltage



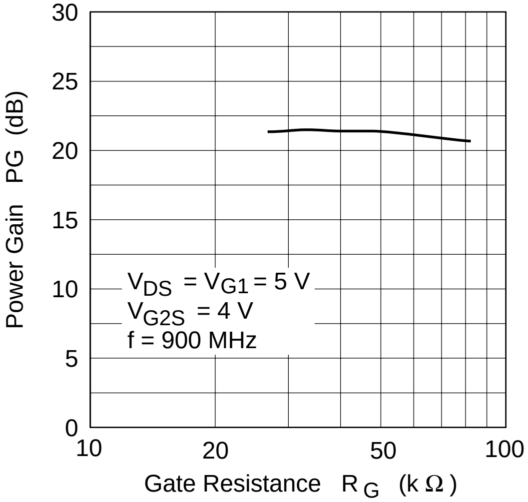
Forward Transfer Admittance vs. Gate1 Voltage



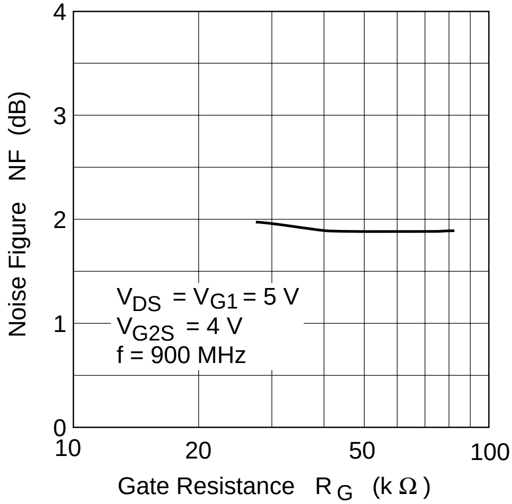
Forward Transfer Admittance vs. Gate1 Voltage



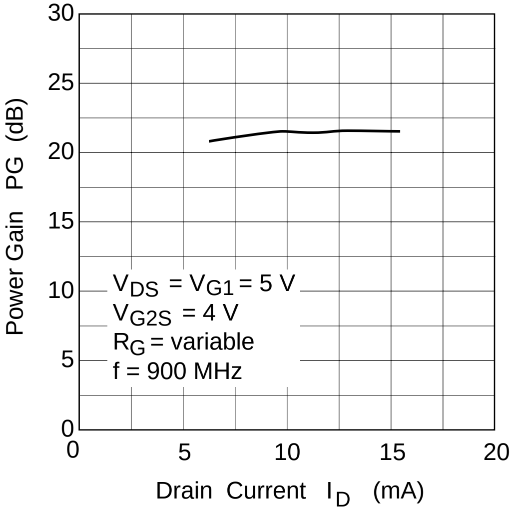
Power Gain vs. Gate Resistance



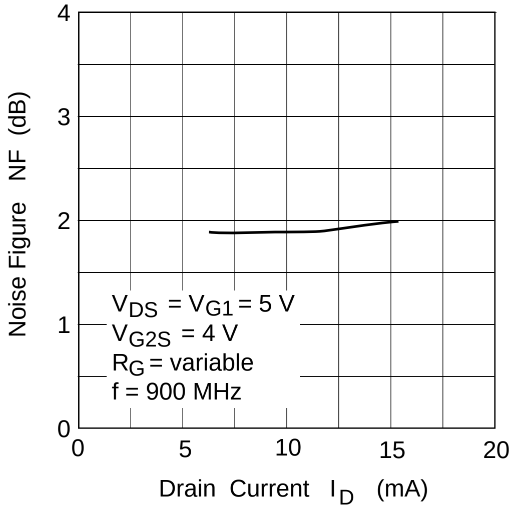
Noise Figure vs. Gate Resistance

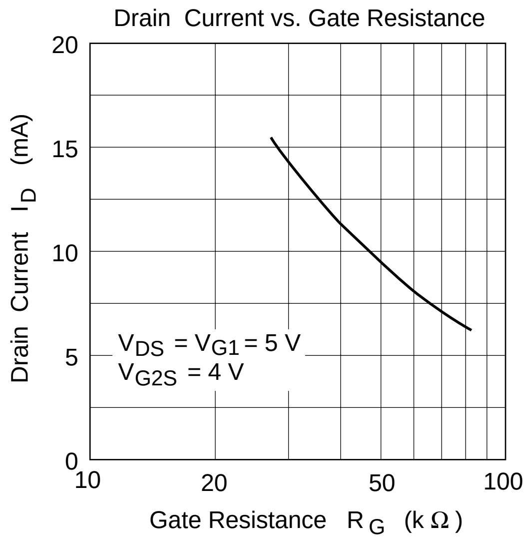


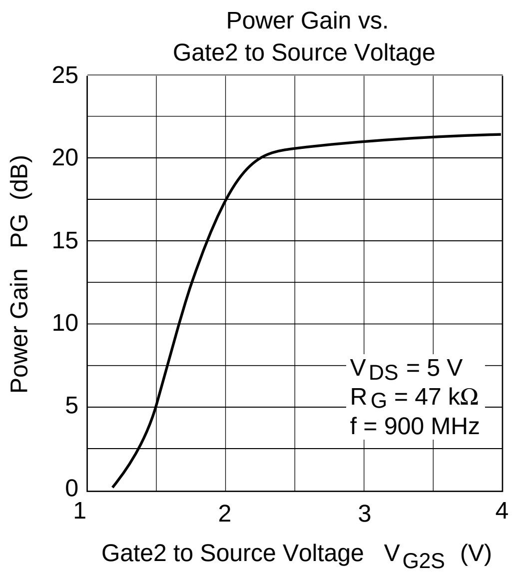
Power Gain vs. Drain Current

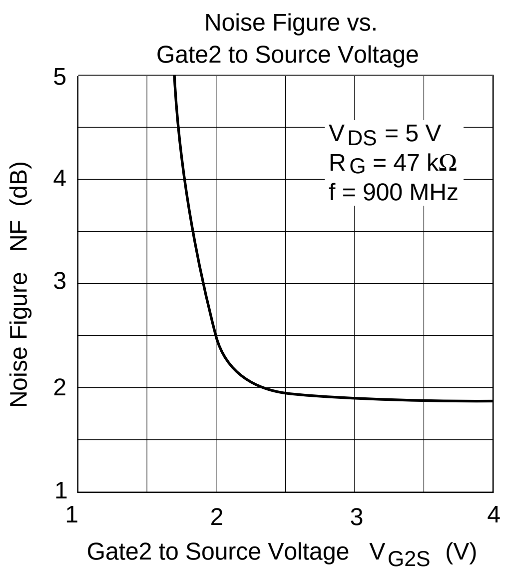


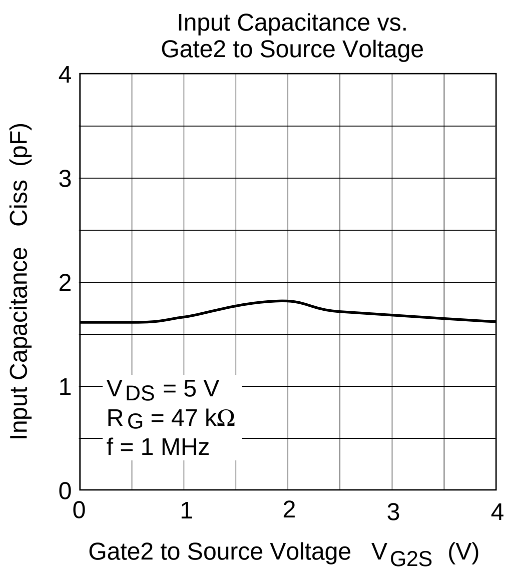
Noise Figure vs. Drain Current

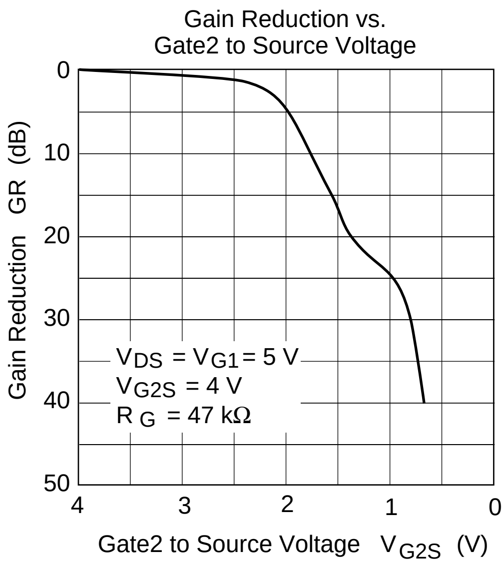



Drain Current vs. Gate Resistance
20
15
10
5
0
10
20
50
100
Drain Current I D (mA)
Gate Resistance R G (k Ω)
V DS = V G1 = 5 V
V G2S = 4 V

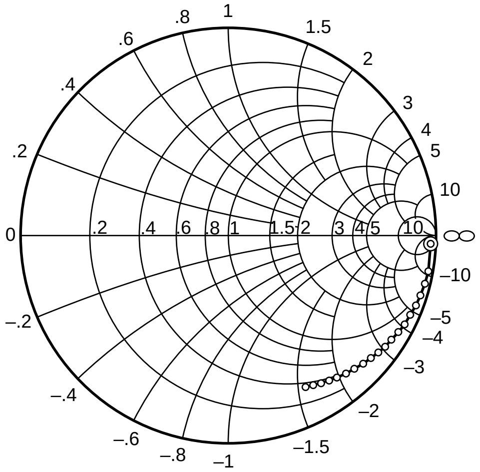

Power Gain vs.
Gate2 to Source Voltage
25
20
15
10
5
0
1
2
3
4
Power Gain PG (dB)
Gate2 to Source Voltage V G2S (V)
V DS = 5 V
R G = 47 kΩ
f = 900 MHz


Noise Figure vs.
Gate2 to Source Voltage
5
4
3
2
1
1
2
3
4
Noise Figure NF (dB)
Gate2 to Source Voltage V G2S (V)
V DS = 5 V
R G = 47 kΩ
f = 900 MHz


Input Capacitance vs.
Gate2 to Source Voltage
4
3
2
1
0
0
1
2
3
4
Input Capacitance Ciss (pF)
Gate2 to Source Voltage V G2S (V)
V DS = 5 V
R G = 47 kΩ
f = 1 MHz


Gain Reduction vs.
Gate2 to Source Voltage
Gain Reduction GR (dB)
0
10
20
30
40
50
4
3
2
1
0
Gate2 to Source Voltage V G2S (V)
VDS = VG1 = 5 V
VG2S = 4 V
R G = 47 kΩ

S11 Parameter vs. Frequency

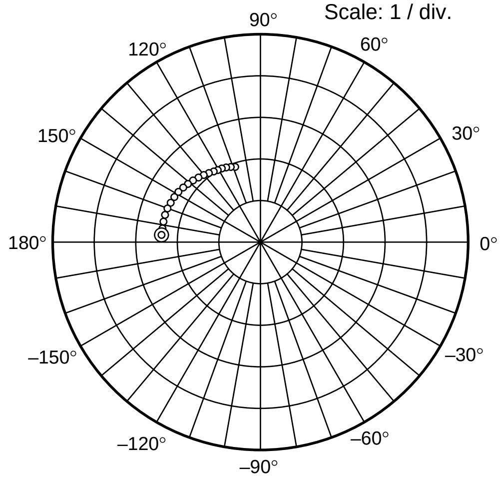


Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 47 k Ω ,
Zo = 50 Ω

50 to 1000 MHz (50 MHz step)

S21 Parameter vs. Frequency

Scale: 1 / div.

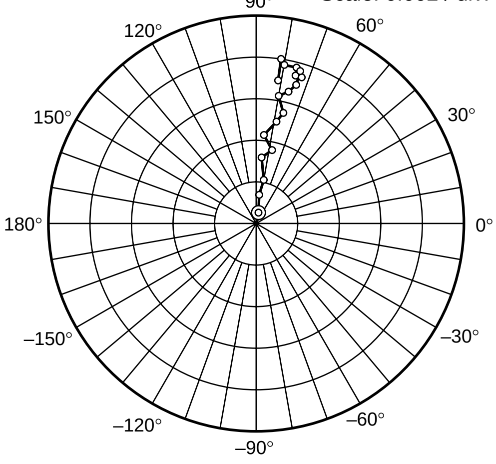


Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 47 k Ω ,
Zo = 50 Ω

50 to 1000 MHz (50 MHz step)

S12 Parameter vs. Frequency

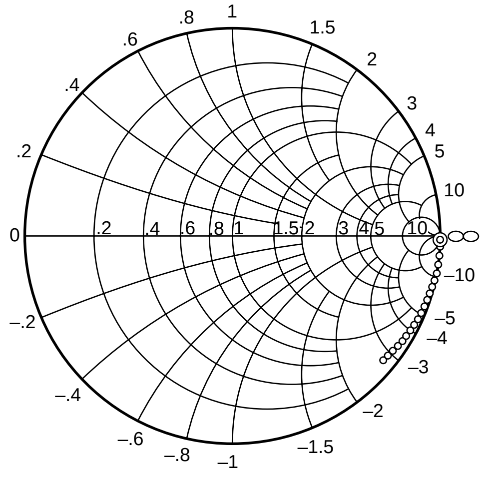
Scale: 0.002 / div.



Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 47 k Ω ,
Zo = 50 Ω

50 to 1000 MHz (50 MHz step)

S22 Parameter vs. Frequency



Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 47 k Ω ,
Zo = 50 Ω

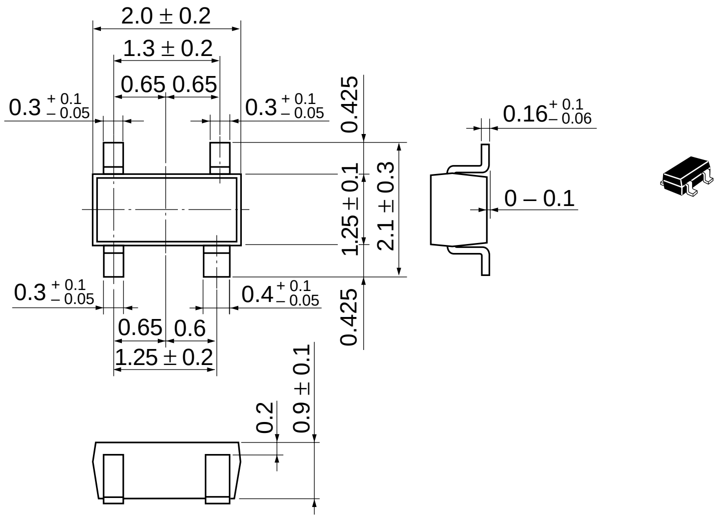
50 to 1000 MHz (50 MHz step)

Sparameter ($V_{DS} = V_{G1} = 5V$, $V_{G2S} = 4V$, $R_G = 47k\Omega$, $Zo = 50\Omega$)

	S11		S21		S12		S22	
f (MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	0.974	–2.8	2.40	176.4	0.00057	78.1	0.997	–2.0
100	0.974	–10.0	2.38	172.2	0.00144	82.4	0.998	–4.2
150	0.974	–13.6	2.38	168.4	0.00211	78.7	0.997	–6.0
200	0.965	–16.5	2.37	164.1	0.00316	84.8	0.995	–8.1
250	0.963	–20.0	2.35	160.4	0.00358	76.3	0.994	–10.2
300	0.953	–23.7	2.32	156.8	0.00431	84.0	0.992	–12.2
350	0.947	–26.8	2.30	152.9	0.00503	79.0	0.990	–14.2
400	0.942	–29.6	2.28	148.6	0.00545	76.6	0.987	–16.2
450	0.929	–32.8	2.26	144.9	0.00630	80.3	0.984	–18.1
500	0.923	–35.4	2.21	141.2	0.00646	76.1	0.981	–20.2
550	0.912	–38.5	2.19	137.6	0.00693	73.7	0.977	–22.1
600	0.903	–41.2	2.15	134.2	0.00732	72.9	0.974	–24.1
650	0.886	–44.2	2.12	130.6	0.00729	74.6	0.971	–26.0
700	0.879	–46.8	2.08	127.4	0.00733	72.0	0.967	–27.8
750	0.873	–49.2	2.06	124.3	0.00762	74.5	0.962	–29.7
800	0.859	–52.4	2.03	120.8	0.00756	73.7	0.959	–31.7
850	0.846	–55.4	2.00	117.3	0.00772	75.5	0.955	–33.6
900	0.836	–58.0	1.96	114.3	0.00775	79.6	0.951	–35.5
950	0.827	–60.4	1.93	111.0	0.00801	81.7	0.946	–37.3
1000	0.815	–62.8	1.89	108.0	0.00704	81.0	0.942	–39.4

Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	CMPAK-4(T)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.006 g

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Colophon 2.0