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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# 2SJ528(L), 2SJ528(S)

Silicon P Channel MOS FET  
High Speed Power Switching

**RENESAS**

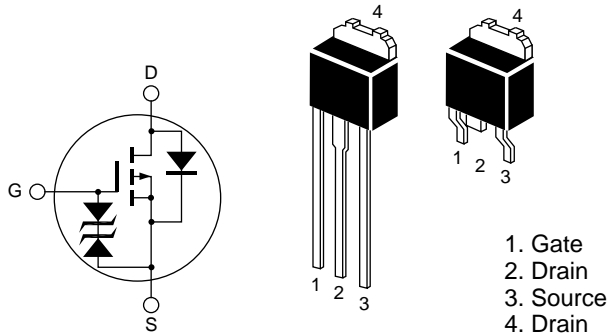
ADE-208-641A (Z)  
2nd. Edition  
Jul. 1998

## Features

- Low on-resistance  $R_{DS(on)} = 0.17 \Omega$  typ.
- 4 V gate drive devices
- High speed switching

## Outline

DPAK-2



## 2SJ528(L),2SJ528(S)

### Absolute Maximum Ratings (Ta = 25°C)

| Item                                   | Symbol                          | Ratings     | Unit |
|--|---------------------------------|-------------|------|
| Drain to source voltage                | $V_{DSS}$                       | -60         | V    |
| Gate to source voltage                 | $V_{GSS}$                       | ±20         | V    |
| Drain current                          | $I_D$                           | -7          | A    |
| Drain peak current                     | $I_{D(pulse)}$ <sup>Note1</sup> | -28         | A    |
| Body-drain diode reverse drain current | $I_{DR}$                        | -7          | A    |
| Avalanche current                      | $I_{AP}$ <sup>Note3</sup>       | -7          | A    |
| Avalanche energy                       | $E_{AR}$ <sup>Note3</sup>       | 4.2         | mJ   |
| Channel dissipation                    | $P_{ch}$ <sup>Note2</sup>       | 20          | W    |
| Channel temperature                    | Tch                             | 150         | °C   |
| Storage temperature                    | Tstg                            | -55 to +150 | °C   |

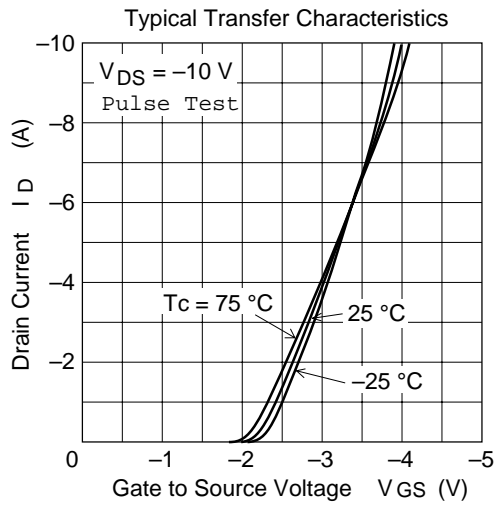
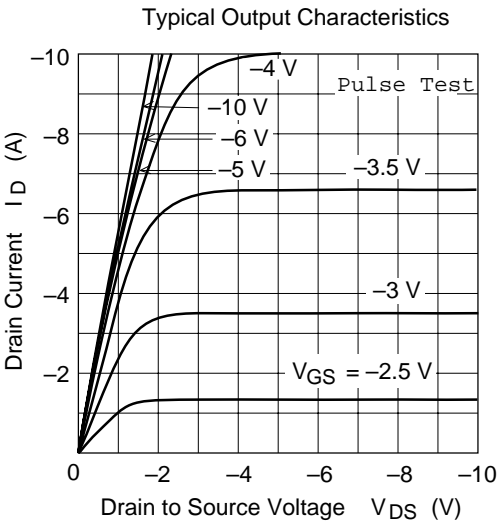
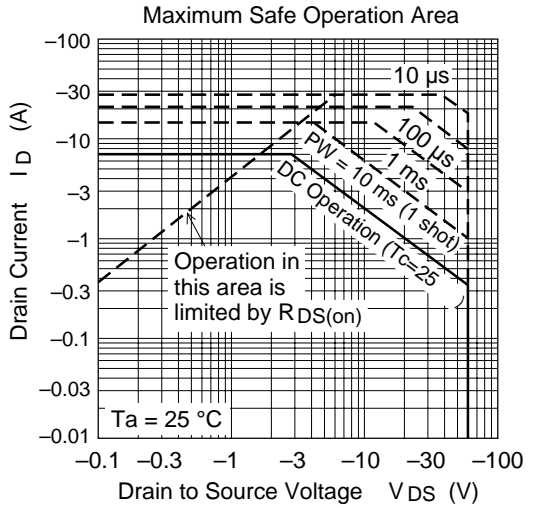
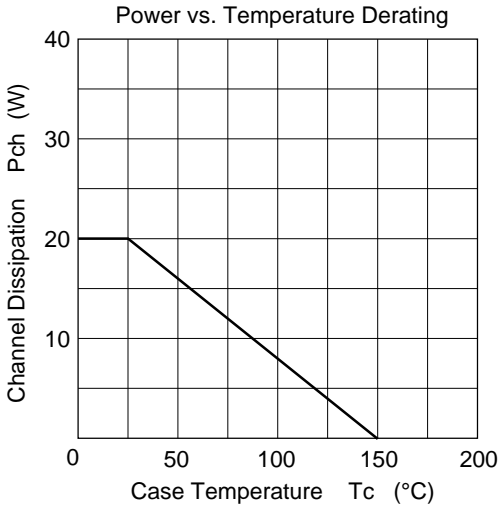
Note: 1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$   
2. Value at  $T_c = 25^\circ C$   
3. Value at  $T_{ch} = 25^\circ C$ ,  $R_g \geq 50 \Omega$

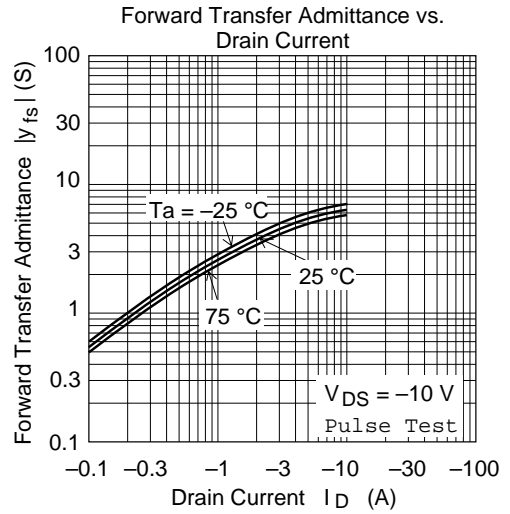
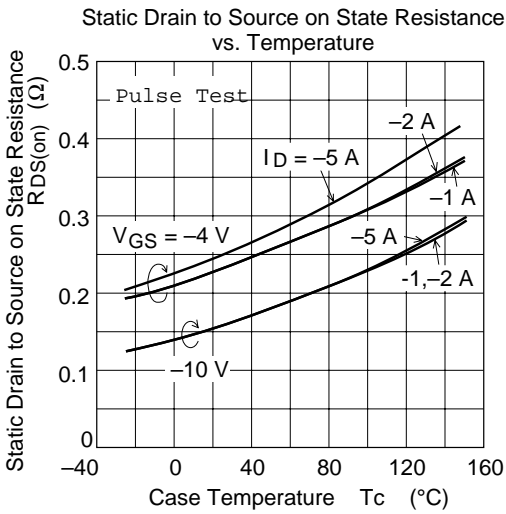
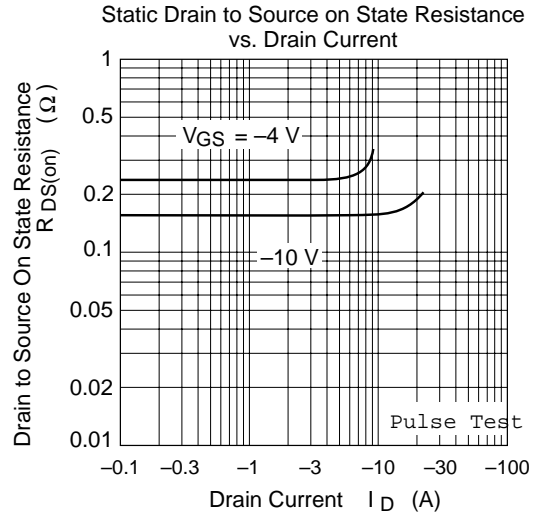
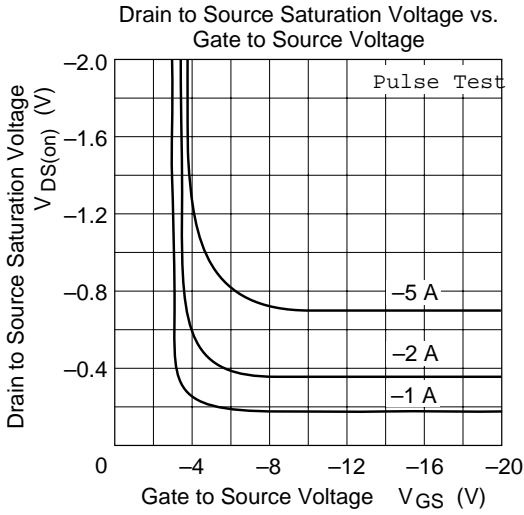
## Electrical Characteristics (Ta = 25°C)

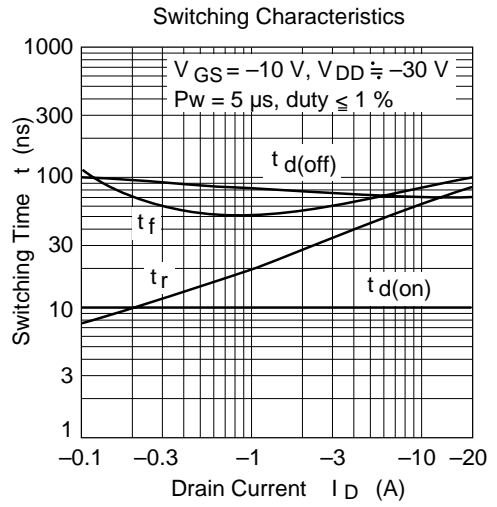
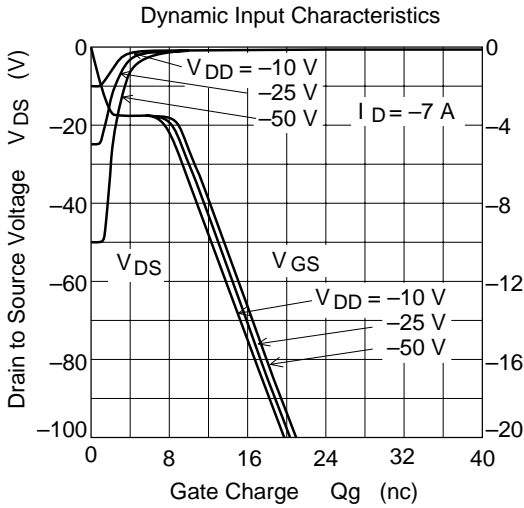
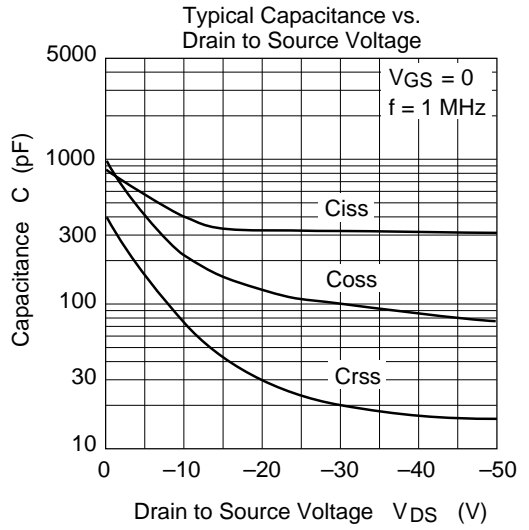
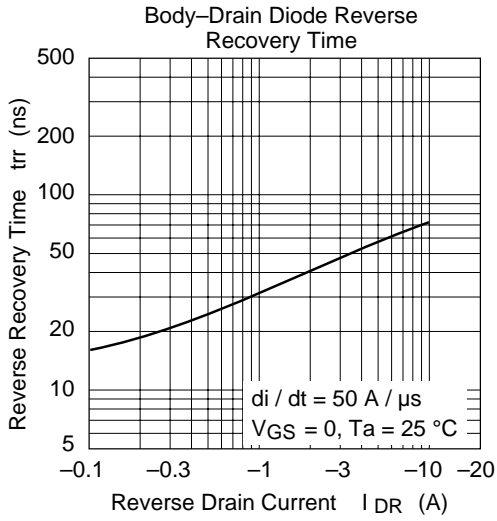
| Item                                       | Symbol        | Min      | Typ  | Max      | Unit          | Test Conditions  |
|--|---------------|----------|------|----------|---------------|--|
| Drain to source breakdown voltage          | $V_{(BR)DSS}$ | -60      | —    | —        | V             | $I_D = -10\text{mA}$ , $V_{GS} = 0$                                    |
| Gate to source breakdown voltage           | $V_{(BR)GSS}$ | $\pm 20$ | —    | —        | V             | $I_G = \pm 100\mu\text{A}$ , $V_{DS} = 0$                              |
| Zero gate voltage drain current            | $I_{DSS}$     | —        | —    | -10      | $\mu\text{A}$ | $V_{DS} = -60\text{V}$ , $V_{GS} = 0$                                  |
| Gate to source leak current                | $I_{GSS}$     | —        | —    | $\pm 10$ | $\mu\text{A}$ | $V_{GS} = \pm 16\text{V}$ , $V_{DS} = 0$                               |
| Gate to source cutoff voltage              | $V_{GS(off)}$ | -1.0     | —    | -2.0     | V             | $I_D = -1\text{mA}$ , $V_{DS} = -10\text{V}$                           |
| Static drain to source on state resistance | $R_{DS(on)}$  | —        | 0.17 | 0.22     | $\Omega$      | $I_D = -4\text{A}$ , $V_{GS} = -10\text{V}$ <sup>Note4</sup>           |
|  | $R_{DS(on)}$  | —        | 0.24 | 0.37     | $\Omega$      | $I_D = -4\text{A}$ , $V_{GS} = -4\text{V}$ <sup>Note4</sup>            |
| Forward transfer admittance                | $ y_{fs} $    | 3.0      | 5.0  | —        | S             | $I_D = -4\text{A}$ , $V_{DS} = -10\text{V}$ <sup>Note4</sup>           |
| Input capacitance                          | $C_{iss}$     | —        | 400  | —        | pF            | $V_{DS} = -10\text{V}$   |
| Output capacitance                         | $C_{oss}$     | —        | 220  | —        | pF            | $V_{GS} = 0$   |
| Reverse transfer capacitance               | $C_{rss}$     | —        | 75   | —        | pF            | $f = 1\text{MHz}$  |
| Turn-on delay time                         | $t_{d(on)}$   | —        | 10   | —        | ns            | $V_{GS} = -10\text{V}$ , $I_D = -4\text{A}$                            |
| Rise time                                  | $t_r$         | —        | 40   | —        | ns            | $R_L = 7.5\Omega$  |
| Turn-off delay time                        | $t_{d(off)}$  | —        | 75   | —        | ns            |  |
| Fall time                                  | $t_f$         | —        | 65   | —        | ns            |  |
| Body-drain diode forward voltage           | $V_{DF}$      | —        | -1.1 | —        | V             | $I_F = -7\text{A}$ , $V_{GS} = 0$                                      |
| Body-drain diode reverse recovery time     | $t_{rr}$      | —        | 65   | —        | ns            | $I_F = -7\text{A}$ , $V_{GS} = 0$<br>$diF/dt = 50\text{A}/\mu\text{s}$ |

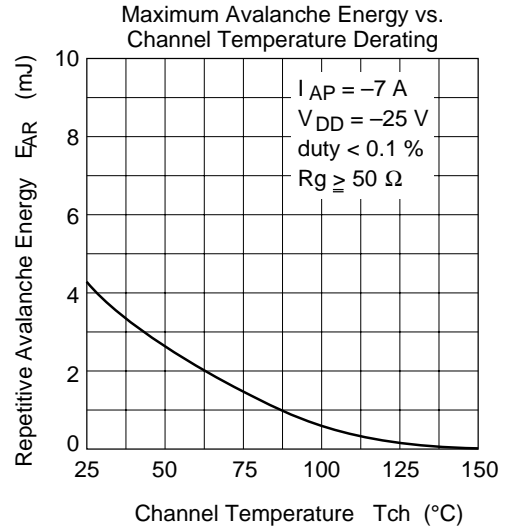
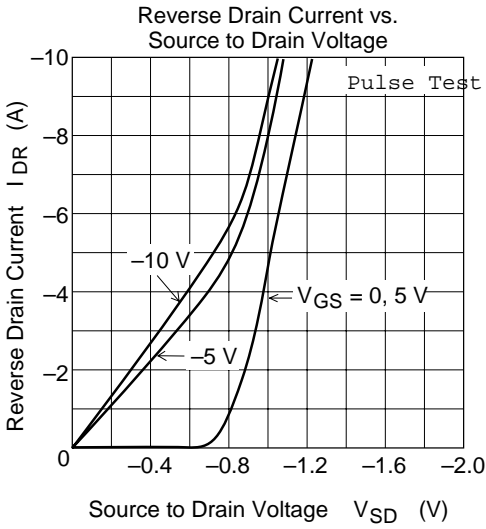
Note: 4. Pulse test

Main Characteristics

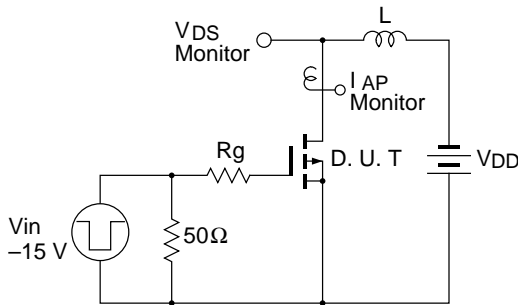






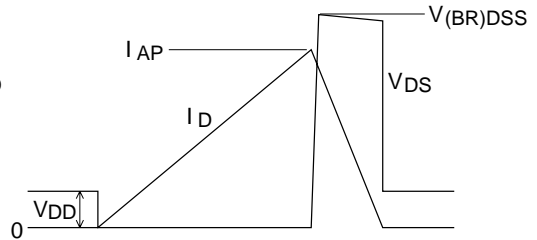


Avalanche Test Circuit

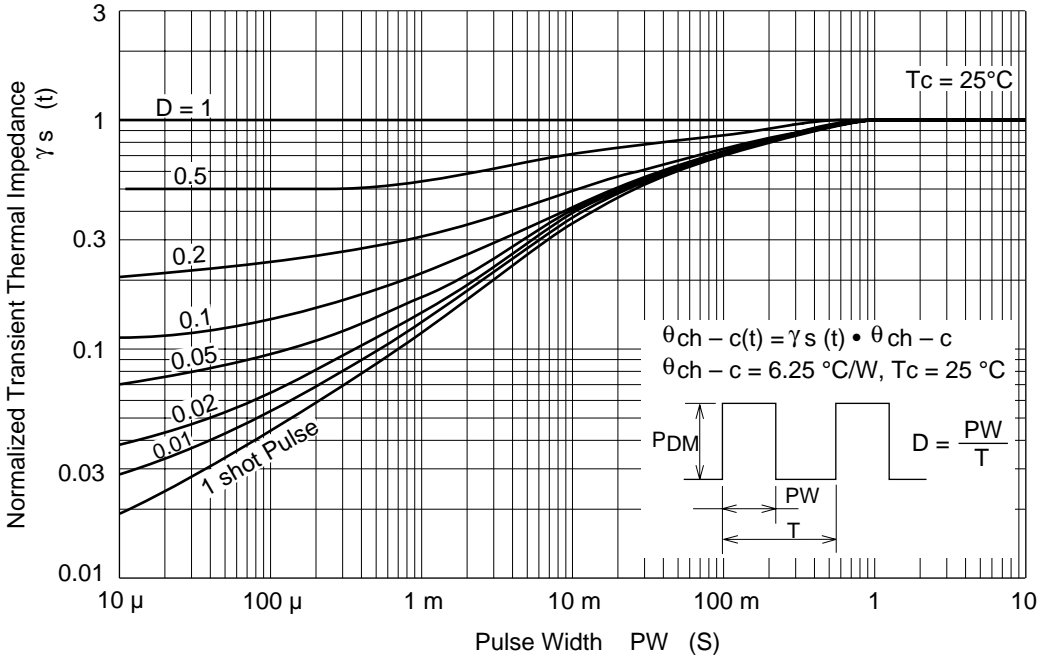


Avalanche Waveform

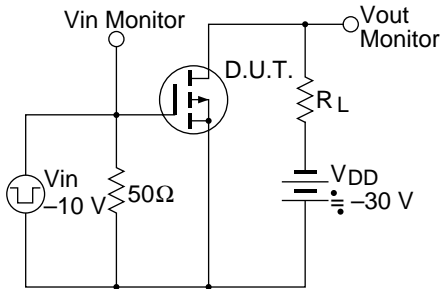
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



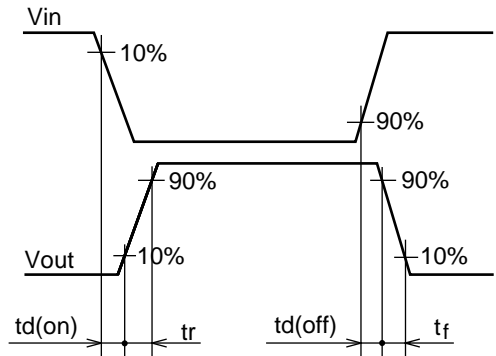
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Waveform

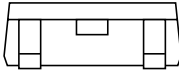
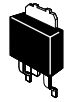
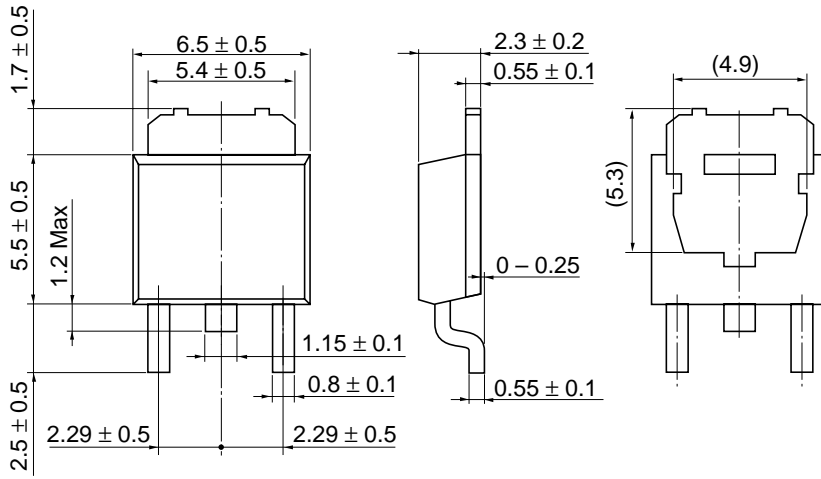




# 2SJ528(L),2SJ528(S)

As of January, 2001

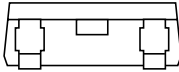
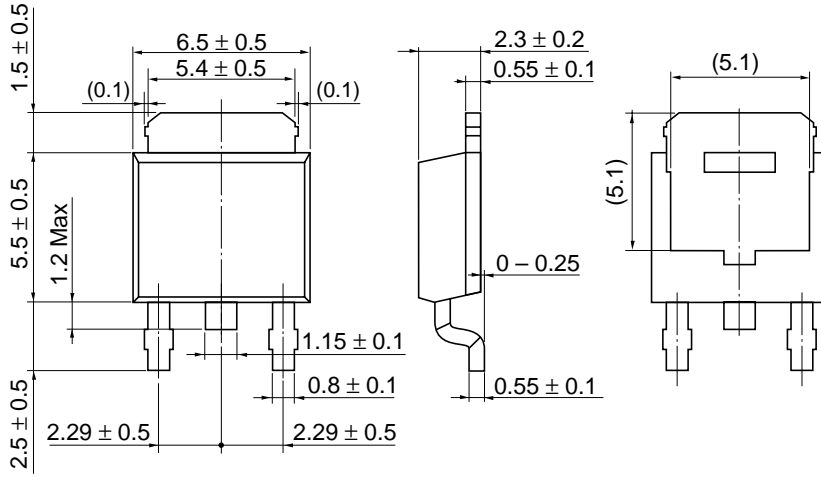
Unit: mm



|                        |                  |
|------------------------|------------------|
| Hitachi Code           | DPAK (S)-(1),(2) |
| JEDEC                  | —                |
| EIAJ                   | Conforms         |
| Mass (reference value) | 0.28 g           |

As of January, 2001

Unit: mm



|                        |              |
|------------------------|--------------|
| Hitachi Code           | DPAK (S)-(3) |
| JEDEC                  | —            |
| EIAJ                   | Conforms     |
| Mass (reference value) | 0.28 g       |

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