To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

RENESAS
Renesas Technology Corp.

Cautions

HAT2058R/HAT2058RJ

Silicon N Channel Power MOS FET
High Speed Power Switching

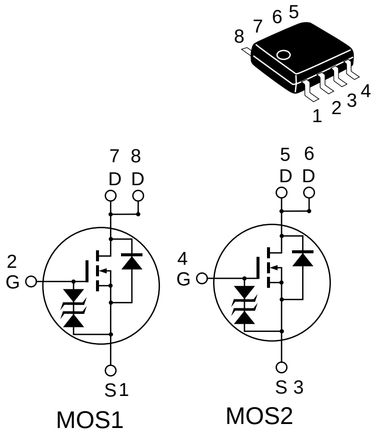
ADE-208-934 (Z)
1st. Edition
Mar. 2001

Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting
- "J" is for Automotive application
  High temperature D-S leakage guarantee
  Avalanche rating

Outline

SOP-8



1, 3	Source
2, 4	Gate
5, 6, 7, 8	Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings HAT2058R	Ratings HAT2058RJ	Unit
Drain to source voltage	V_{DSS}	100	100	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	4	4	A
Drain peak current	I_D (pulse) [Note1]	32	32	A
Body-drain diode reverse drain current	I_{DR}	4	4	A
Avalanche current	I_{AP} [Note4]	—	4	A
Avalanche energy	E_{AR} [Note4]	—	1.6	mJ
Channel dissipation	Pch [Note2]	2	2	W
	Pch [Note3]	3	3	W
Channel temperature	Tch	150	150	°C
Storage temperature	Tstg	–55 to +150	–55 to +150	°C

Notes:
1. PW ≤ 10 µs, duty cycle ≤ 1%
2. 1 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s
3. 2 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s
4. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics (Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage		$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage		$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 μA, V_{DS} = 0
Zero gate voltage drain current	HAT2058R	I_{DSS}	—	—	1	μA	V_{DS} = 100 V, V_{GS} = 0
	HAT2058RJ	I_{DSS}	—	—	0.1	μA	
Zero gate voltage drain current	HAT2058R	I_{DSS}	—	—	—	μA	V_{DS} = 80 V, V_{GS} = 0
	HAT2058RJ	I_{DSS}	—	—	10	μA	Ta = 125°C
Gate to source cutoff voltage		I_{GSS}	—	—	±10	μA	V_{GS} = ±16 V, V_{DS} = 0
Static drain to source on state resistance		$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward transfer admittance		$\|y_{fs}\|$	3	5	—	S	I_D = 2 A*1, V_{DS} = 10 V
Static drain to source on state resistance		$R_{DS(on)}$	—	120	145	mΩ	I_D = 2 A*1, V_{GS} = 10 V
		$R_{DS(on)}$	—	150	180	mΩ	I_D = 2 A*1, V_{GS} = 4 V
Input capacitance		Ciss	—	420	—	pF	V_{DS} = 10 V, V_{GS} = 0
Output capacitance		Coss	—	180	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	100	—	pF	
Turn-on delay time		td(on)	—	10	—	ns	V_{GS} = 10 V, I_D = 2 A
Rise time		tr	—	30	—	ns	V_{DD} ≅ 30 V
Turn-off delay time		td(off)	—	110	—	ns	
Fall time		tf	—	60	—	ns	
Body-drain diode forward voltage		V_{DF}	—	0.85	1.1	V	I_F = 4 A, V_{GS} = 0*1
Body-drain diode reverse recovery time		trr	—	75	—	ns	I_F = 4 A, V_{GS} = 0 diF/dt = 50 A/μs

Note: 1. Pulse test

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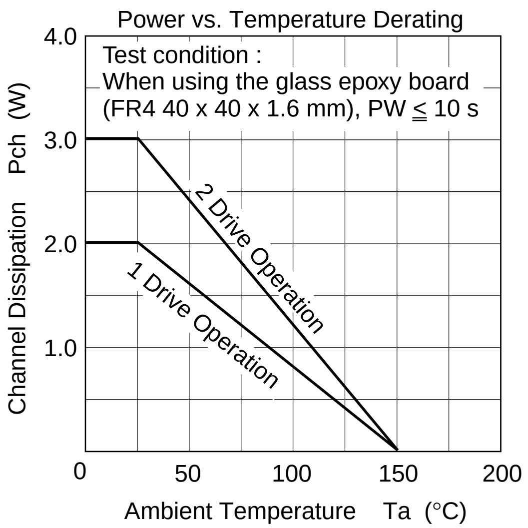
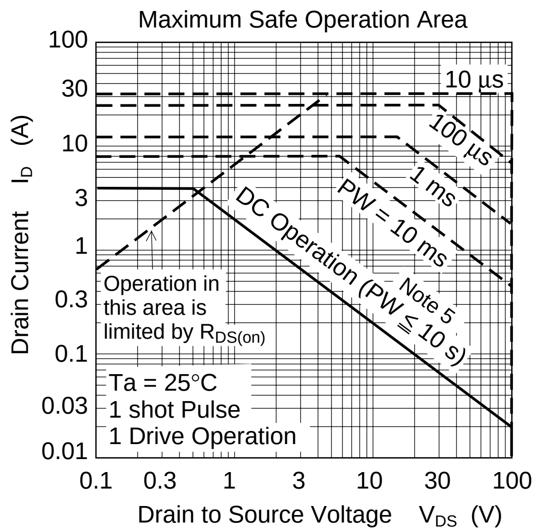
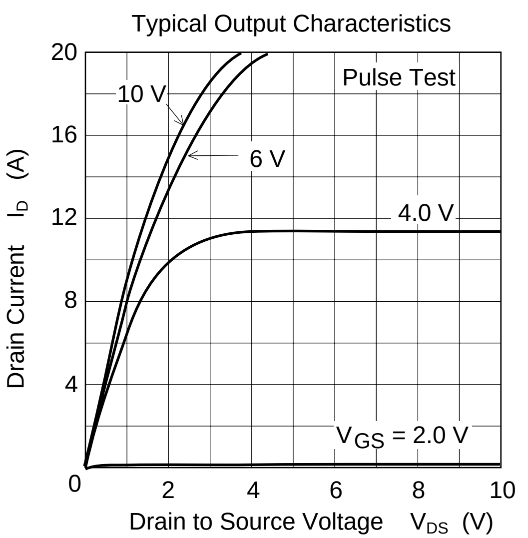
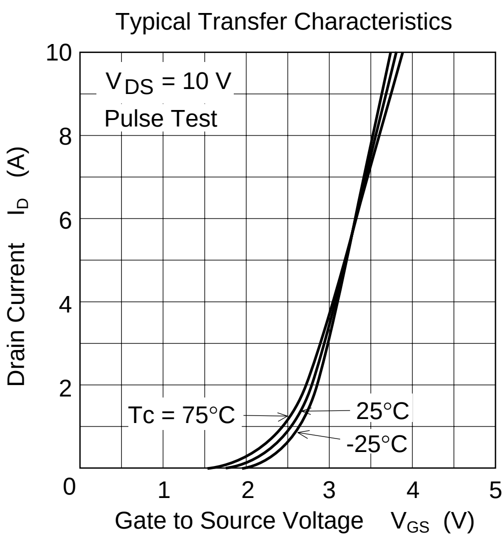
Main Characteristics



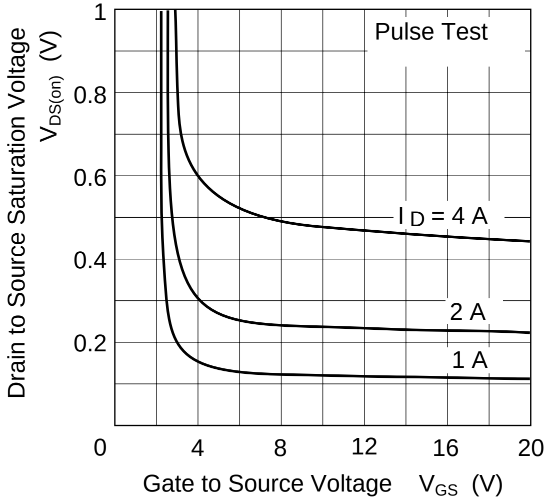


Note 6:
When using the glass epoxy board
(FR4 40 x 40 x 1.6 mm)

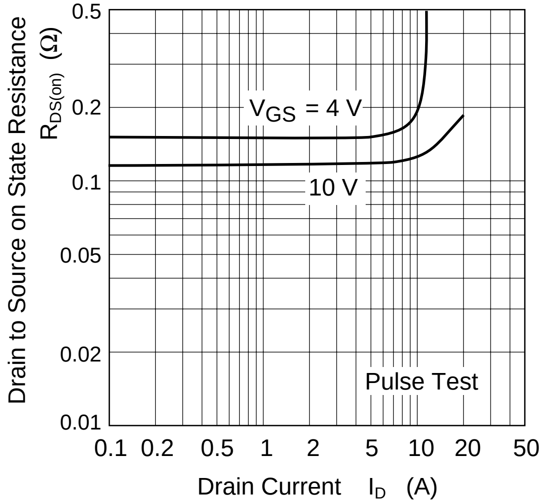




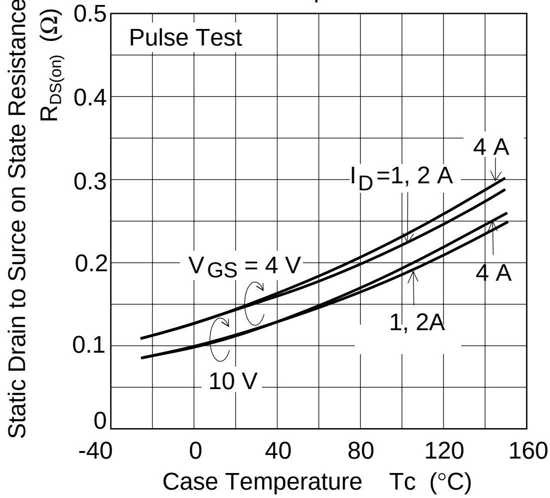
Drain to Source Saturation Voltage vs. Gate to Source Voltage



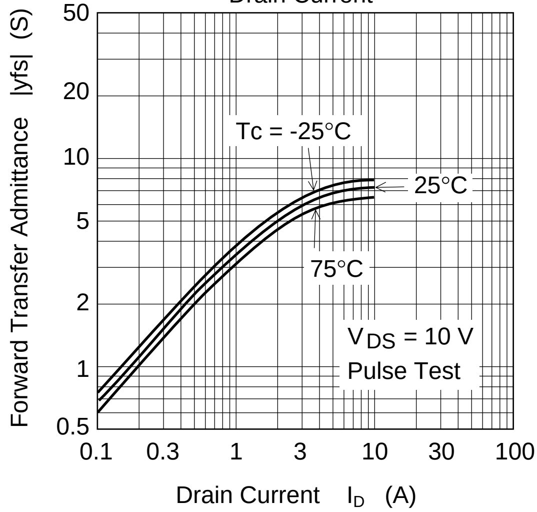
Static Drain to Source on State Resistance vs. Drain Current

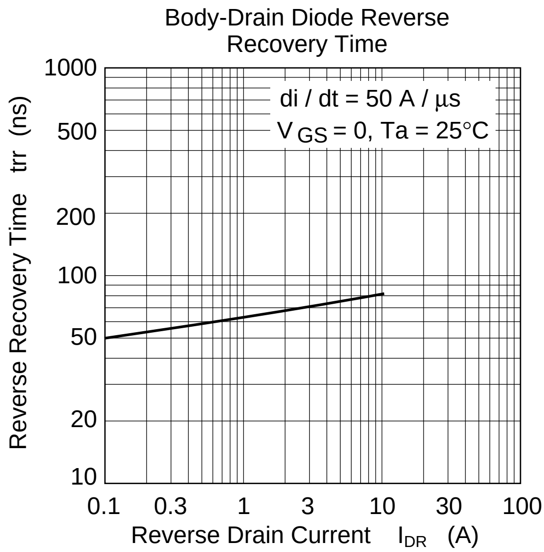


Static Drain to Source on State Resistance vs. Temperature

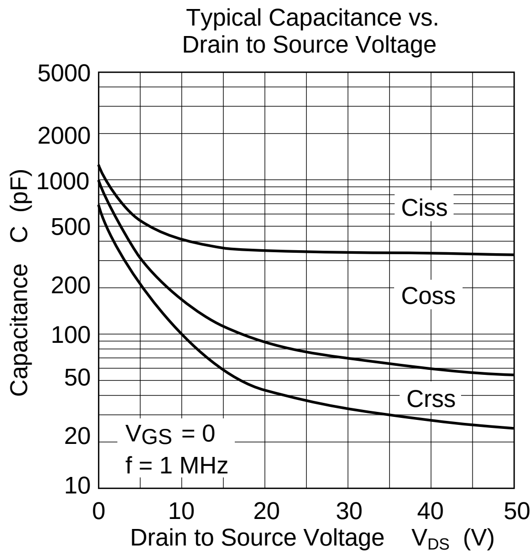


Forward Transfer Admittance vs. Drain Current

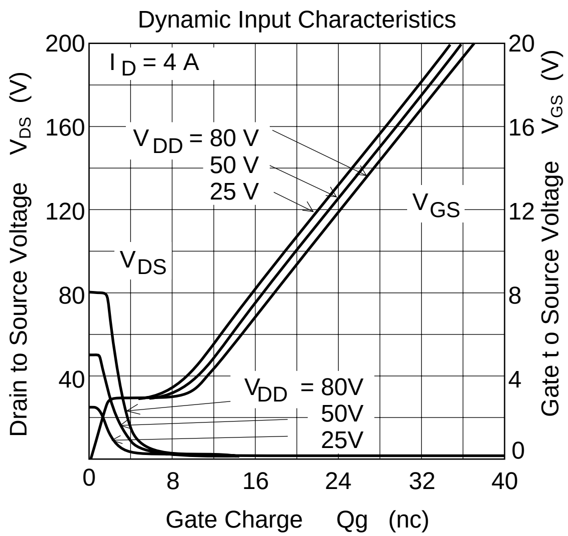




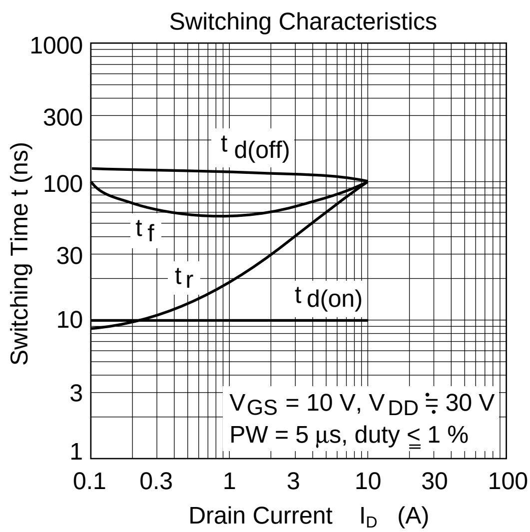
Body-Drain Diode Reverse Recovery Time
di / dt = 50 A / µs
V GS = 0, Ta = 25°C
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.1
0.3
1
3
10
30
100
Reverse Drain Current IDR (A)



Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
5000
2000
1000
500
200
100
50
20
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

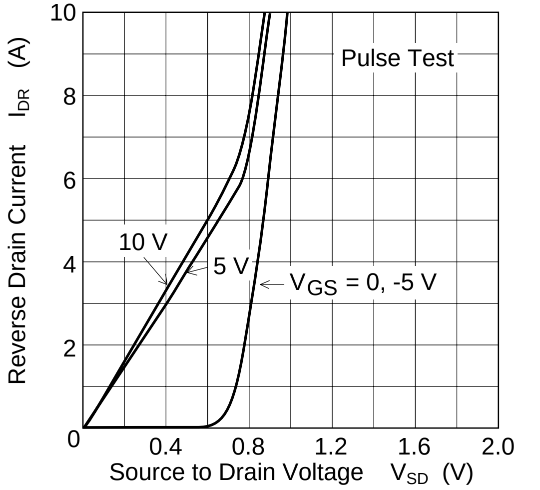


Dynamic Input Characteristics
I D = 4 A
Drain to Source Voltage VDS (V)
200
160
120
80
40
Gate t o Source Voltage VGS (V)
20
16
12
8
4
0
V DD = 80 V
50 V
25 V
VGS
VDS
VDD = 80V
50V
25V
0
8
16
24
32
40
Gate Charge Qg (nc)

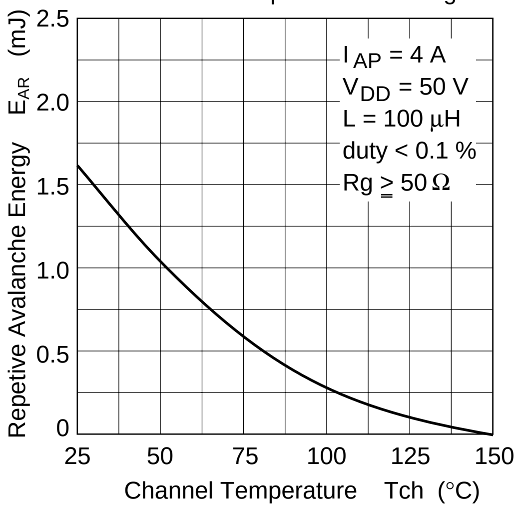


Switching Characteristics
Switching Time t (ns)
1000
300
100
30
10
3
1
t d(off)
t f
t r
t d(on)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦ 1 %
0.1
0.3
1
3
10
30
100
Drain Current ID (A)

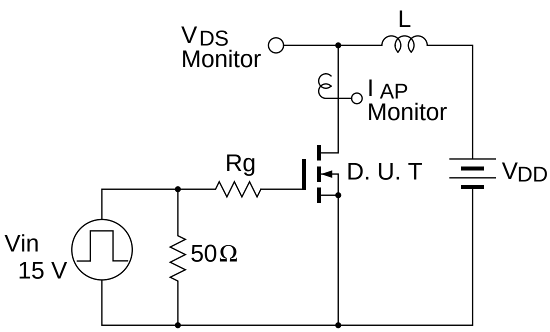
Reverse Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

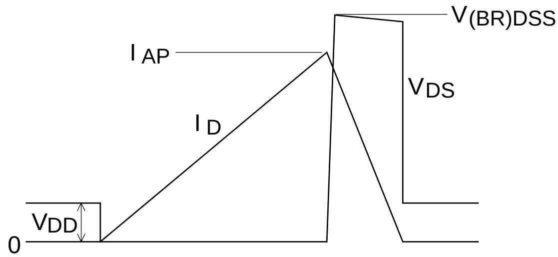


Avalanche Test Circuit

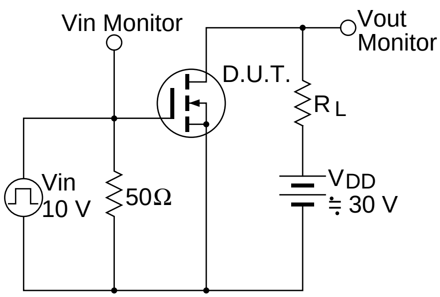


Avalanche Waveform

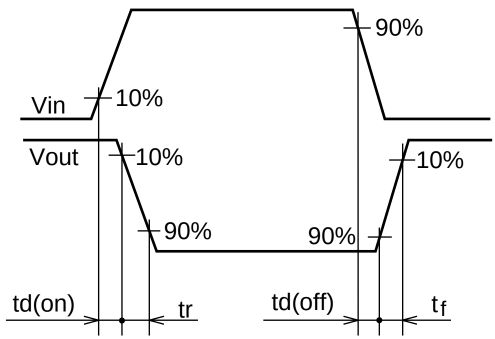
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

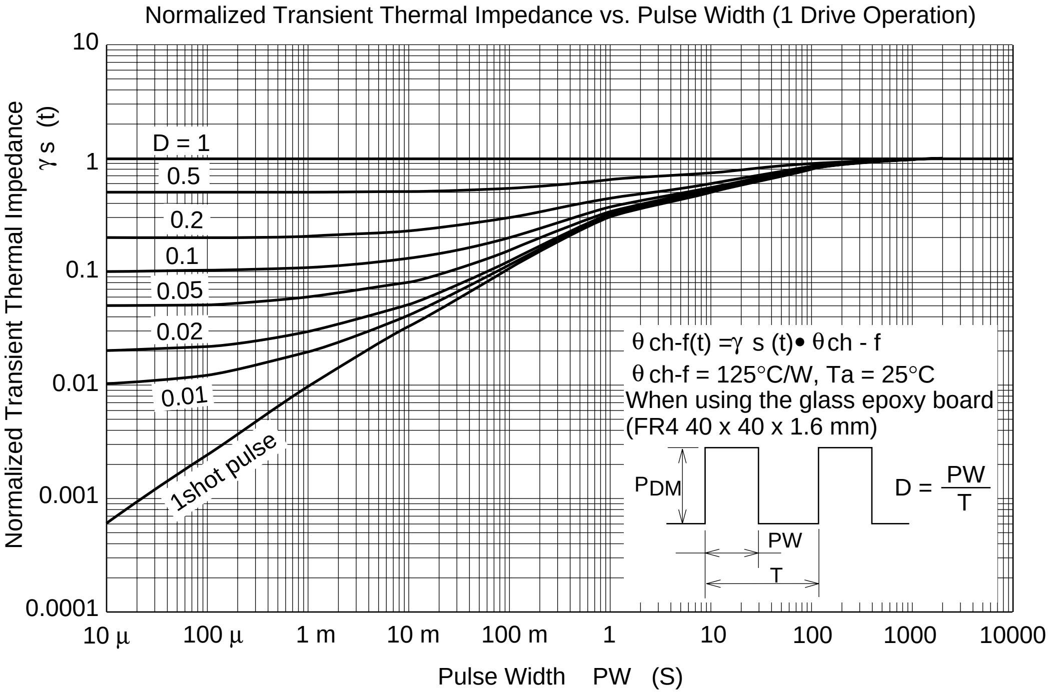


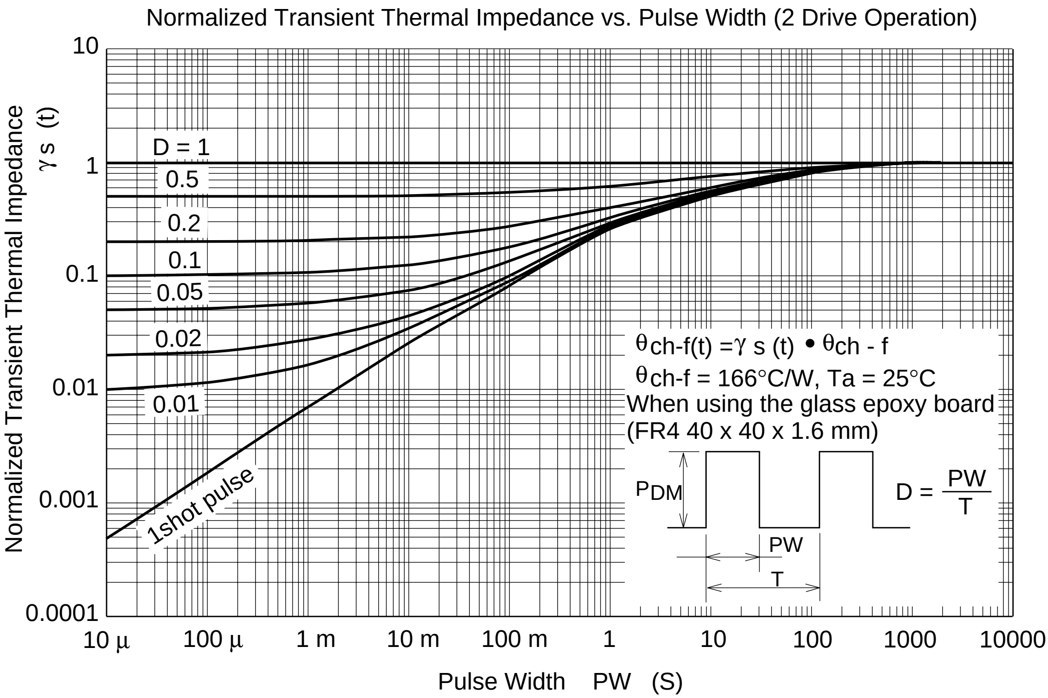
Switching Time Test Circuit



Switching Time Waveform

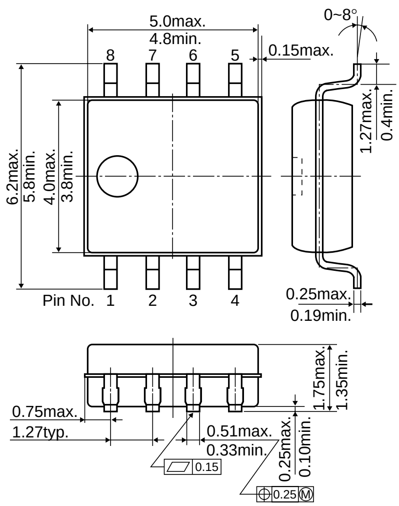


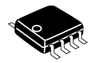

Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)
Normalized Transient Thermal Impedance γs (t)
10
1
0.1
0.01
0.001
0.0001
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch-f(t) = γs (t)• θch - f
θch-f = 125°C/W, Ta = 25°C
When using the glass epoxy board
(FR4 40 x 40 x 1.6 mm)
PDM
PW
T
D = PW/T
10 µ
100 µ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)
Normalized Transient Thermal Impedance γs (t)
10
1
0.1
0.01
0.001
0.0001
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch-f(t) = γs (t) • θch - f
θch-f = 166°C/W, Ta = 25°C
When using the glass epoxy board
(FR4 40 x 40 x 1.6 mm)
PDM
PW
T
D = PW/T
10 µ
100 µ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)

Package Dimensions

Unit: mm





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