

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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# HAT2088R

Silicon N Channel MOSFET  
High Speed Power Switching

**RENESAS**

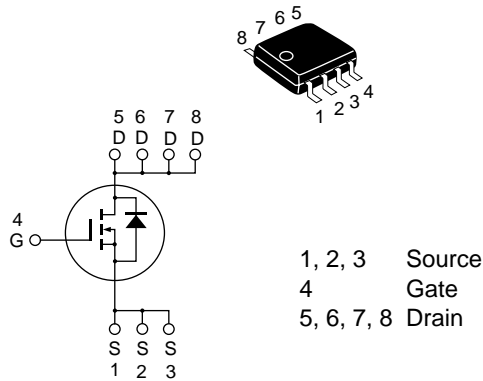
ADE-208-1234 (Z)  
1st. Edition  
Mar. 2001

## Features

- Low on-resistance
- Low leakage current
- High density mounting

## Outline

SOP-8



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	200	V
Gate to source voltage	$V_{GSS}$	±30	V
Drain current	$I_D$	2	A
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	16	A
Body-drain diode reverse drain current	$I_{DR}$	2	A
Channel dissipation	$P_{ch}$ <sup>Note 2</sup>	2.5	W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

Notes: 1.  $PW \leq 10 \mu s$  and duty cycle  $\leq 1\%$

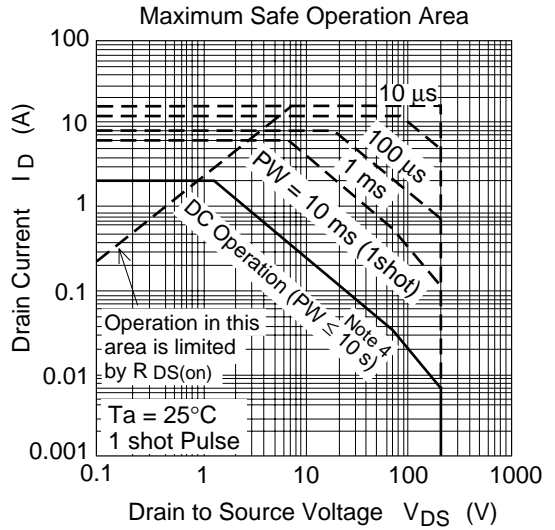
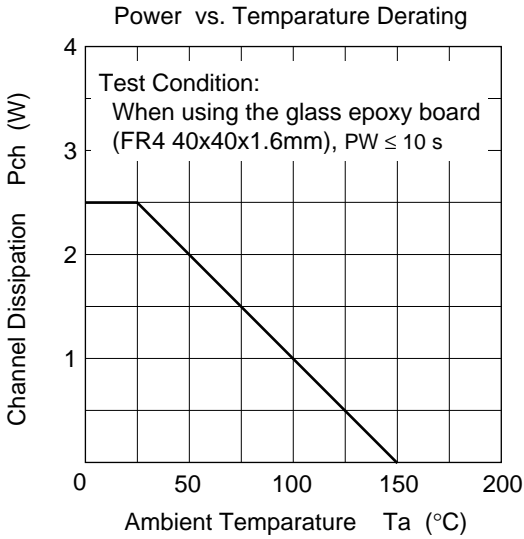
2. When using the glass epoxy board (FR4 40 × 40 × 1.6 mm),  $PW \leq 10 s$

## Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 30\text{V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 200\text{V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$V_{DS} = 10\text{V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.35	0.44	$\Omega$	$I_D = 1\text{A}$ , $V_{GS} = 10\text{V}$ <sup>Note3</sup>
Forward transfer admittance	$ y_{fs} $	1.5	2.5	—	S	$I_D = 1\text{A}$ , $V_{DS} = 10\text{V}$ <sup>Note3</sup>
Input capacitance	$C_{iss}$	—	450	—	pF	$V_{DS} = 25\text{V}$ , $V_{GS} = 0$
Output capacitance	$C_{oss}$	—	65	—	pF	$f = 1 \text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	—	13	—	pF	
Total gate charge	$Q_g$	—	13	—	nC	$V_{DD} = 160 \text{ V}$
Gate to source charge	$Q_{gs}$	—	2	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	6	—	nC	$I_D = 2 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	19	—	ns	$V_{GS} = 10\text{V}$ , $I_D = 1\text{A}$
Rise time	$t_r$	—	8.5	—	ns	$V_{DD} \cong 100\text{V}$
Turn-off delay time	$t_{d(off)}$	—	48	—	ns	$R_L = 100\Omega$
Fall time	$t_f$	—	11	—	ns	$R_g = 10\Omega$
Body-drain diode forward voltage	$V_{DF}$	—	0.8	1.2	V	$I_F = 2\text{A}$ , $V_{GS} = 0$ <sup>Note 3</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	65	—	ns	$I_F = 2\text{A}$ , $V_{GS} = 0$ $diF/dt = 100\text{A}/\mu\text{s}$

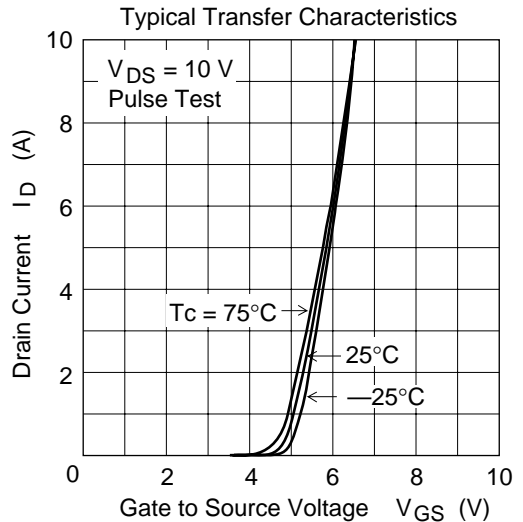
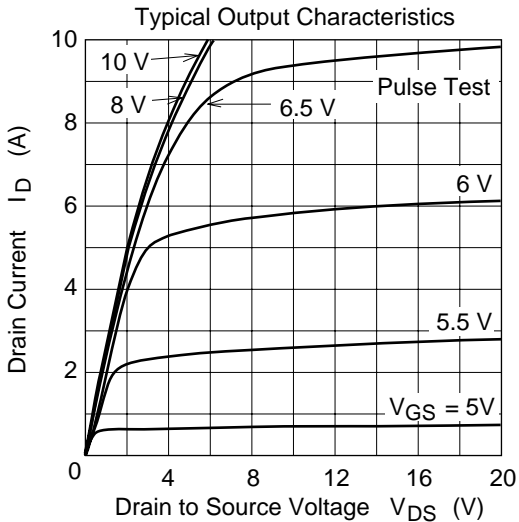
Note: 3. Pulse test

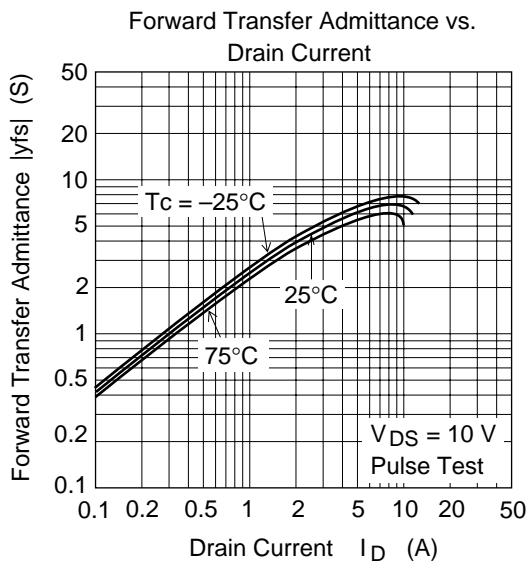
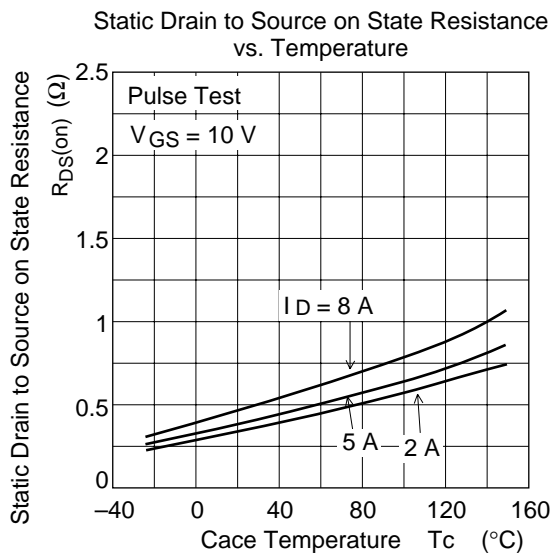
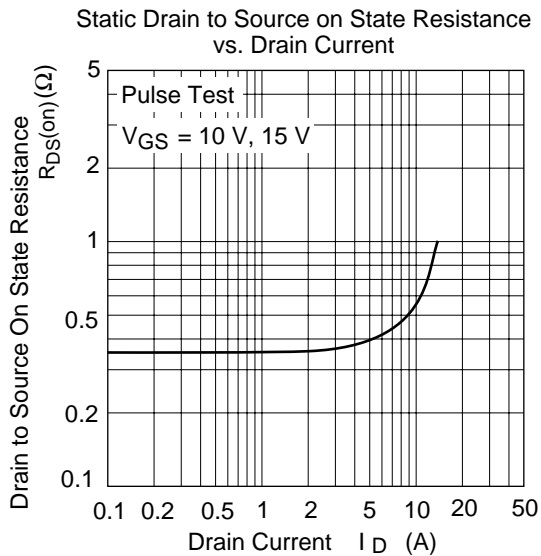
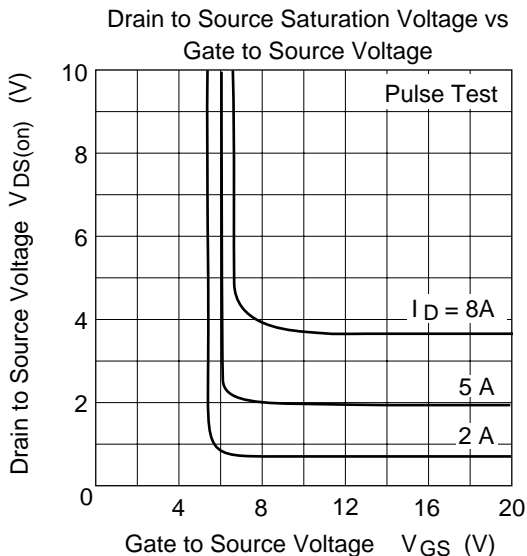
## Main Characteristics



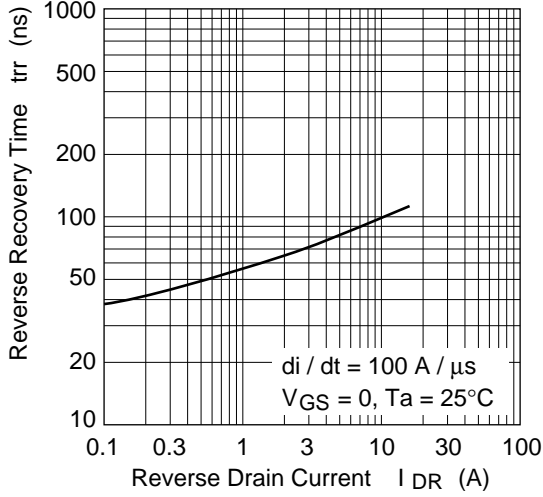
Notes 4:

When using the glass epoxy board  
(FR4 40x40x1.6mm)

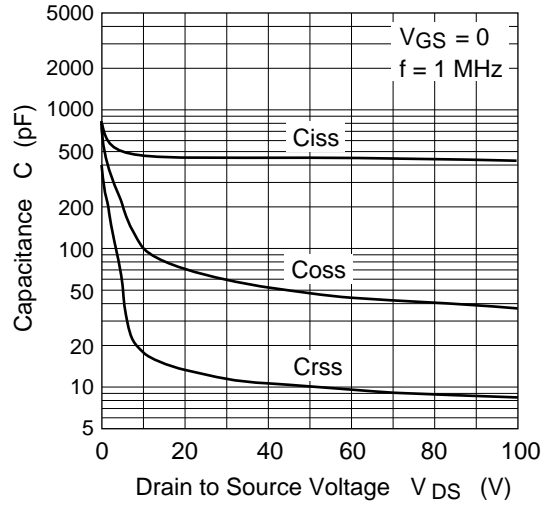




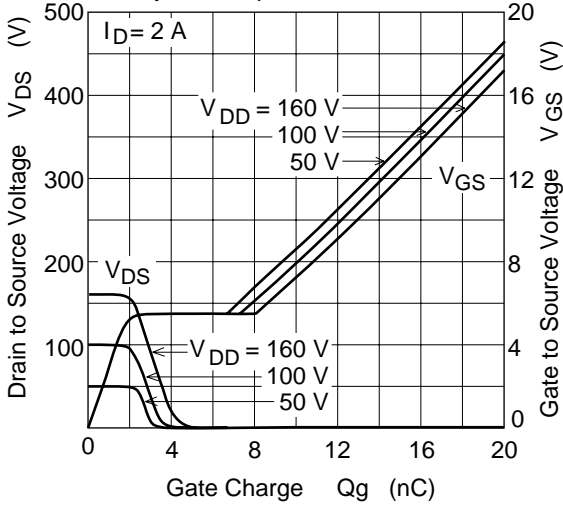
Body-Drain Diode Reverse Recovery Time



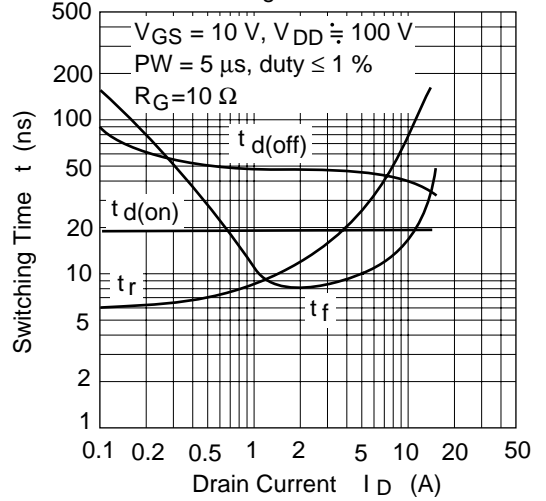
Typical Capacitance vs. Drain to Source Voltage



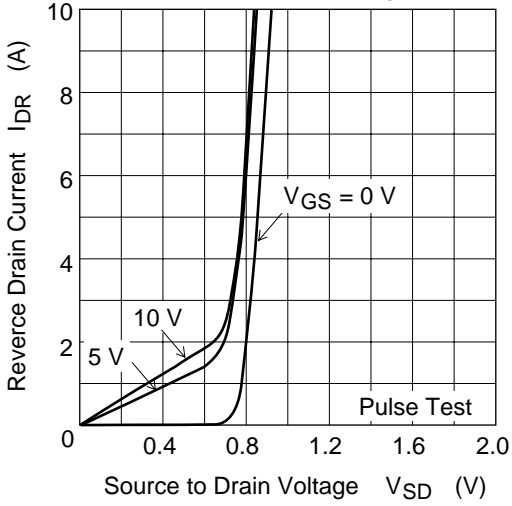
Dynamic Input Characteristics



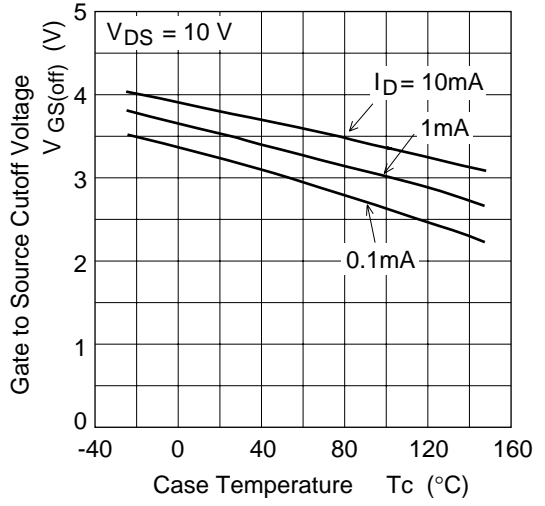
Switching Characteristics



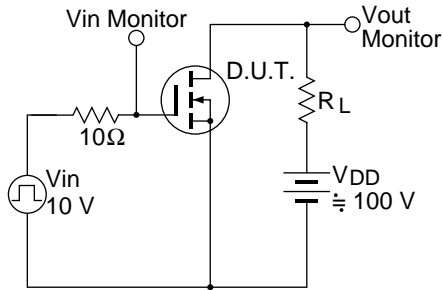
Reverse Drain Current vs. Source to Drain Voltage



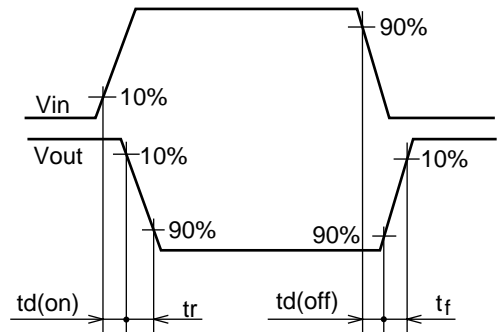
Gate to Source Cutoff Voltage vs. Case Temperature

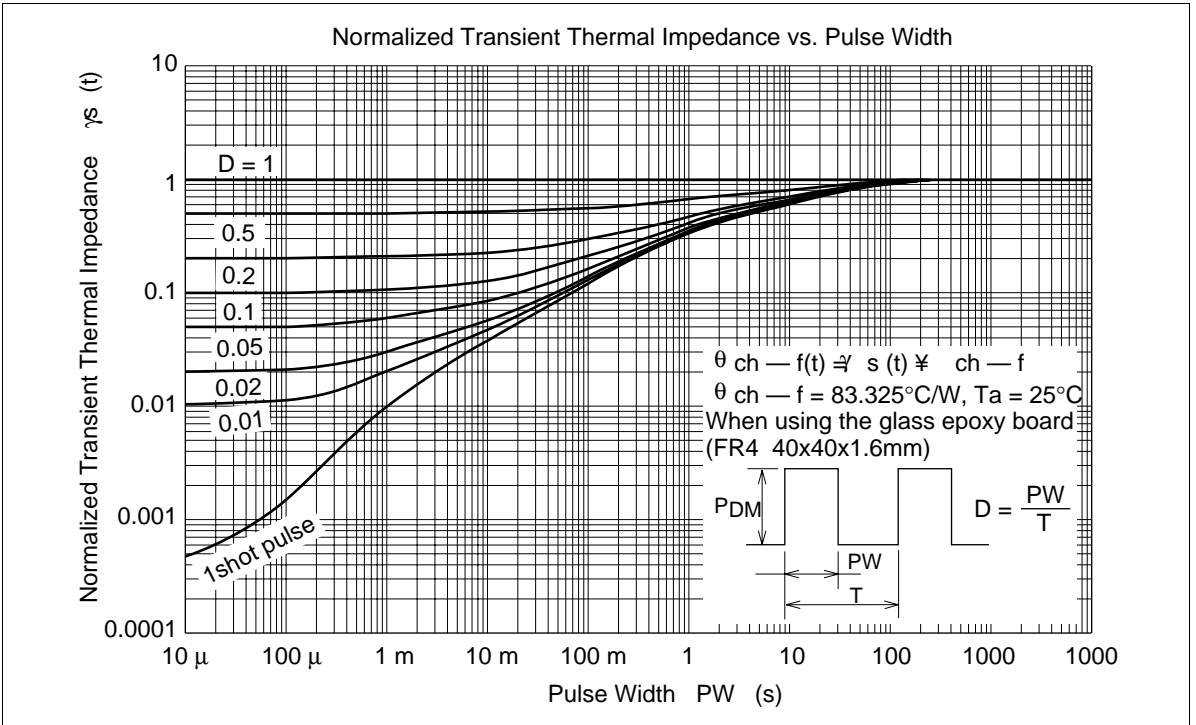


Switching Time Test Circuit



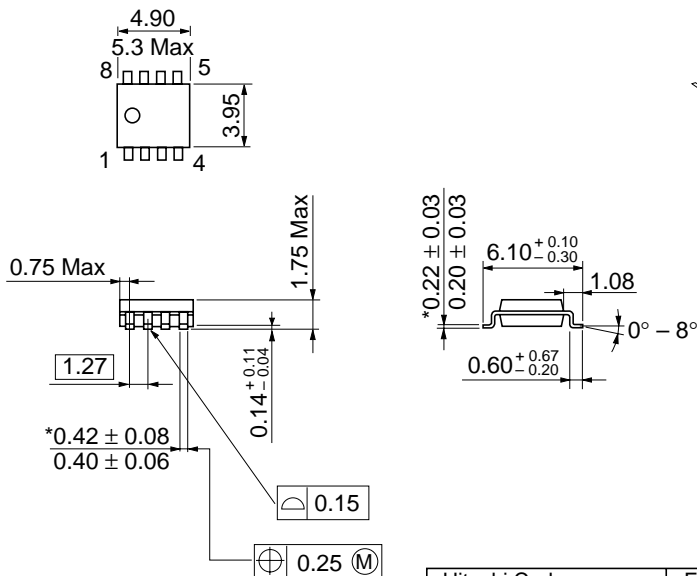
Switching Time Waveform





Package Dimensions

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.085 g

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## Hitachi, Ltd.

Semiconductor & Integrated Circuits  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL      NorthAmerica      : <http://semiconductor.hitachi.com/>  
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### For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe Ltd.  
Electronic Components Group  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 585200

Hitachi Europe GmbH  
Electronic Components Group  
Dornacher StraÙe 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.  
Hitachi Tower  
16 Collyer Quay #20-00  
Singapore 049318  
Tel: <65>-538-6533/538-8577  
Fax: <65>-538-6933/538-3877  
URL: <http://www.hitachi.com.sg>

Hitachi Asia Ltd.  
(Taipei Branch Office)  
4/F, No. 167, Tun Hwa North Road  
Hung-Kuo Building  
Taipei (105), Taiwan  
Tel: <886>-(2)-2718-3666  
Fax: <886>-(2)-2718-8180  
Telex: 23222 HAS-TP  
URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower  
World Finance Centre,  
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Tsim Sha Tsui, Kowloon  
Hong Kong  
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Fax: <852>-(2)-730-0281  
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