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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HAT2137H

Silicon N Channel Power MOS FET
Power Switching

ADE-208-1579B (Z)

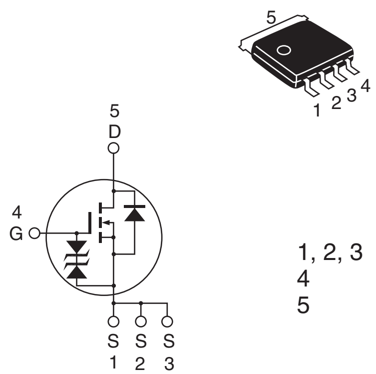
Preliminary
3rd. Edition
Dec. 2002

Features

- Capable of 7 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 3.8 mΩ typ. (at V_{GS} = 10 V)

Outline

LFPAK



1, 2, 3 Source
4 Gate
5 Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	40	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	45	A
Drain peak current	$I_{D(pulse)}$ Note1	180	A
Body-drain diode reverse drain current	I_{DR}	45	A
Avalanche current	I_{AP} Note 3	30	A
Avalanche energy	E_{AR} Note 3	72	mJ
Channel dissipation	Pch Note2	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to + 150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

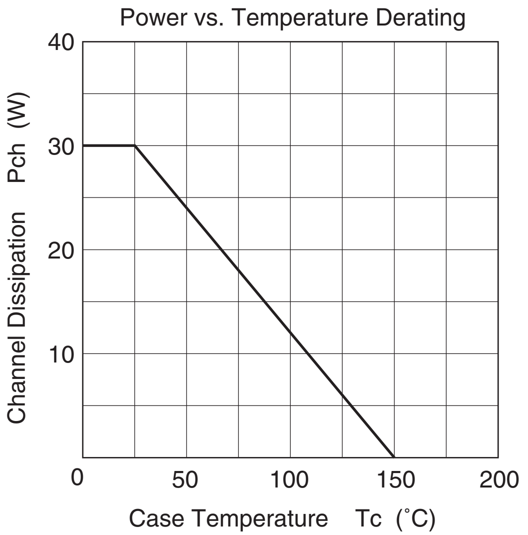
Electrical Characteristics

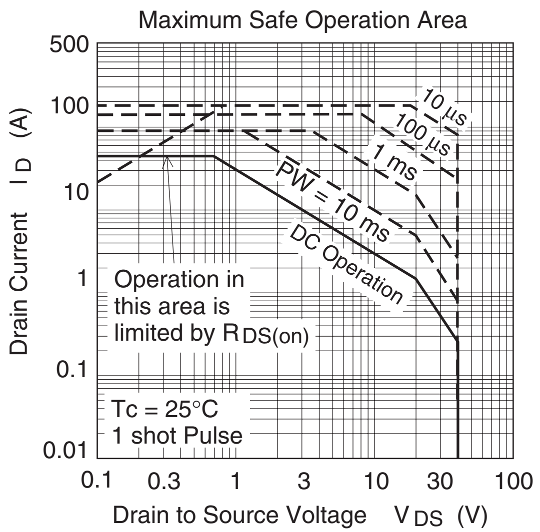
(Ta = 25°C)

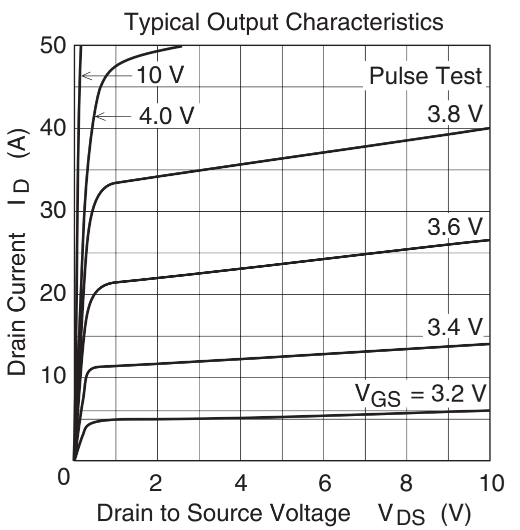
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	± 10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 40 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	3.8	4.8	mΩ	I_D = 22.5 A, V_{GS} = 10 V Note3
	$R_{DS(on)}$	—	4.4	6.0	mΩ	I_D = 22.5 A, V_{GS} = 7 V Note3
Forward transfer admittance	$\|y_{fs}\|$	38	64	—	S	I_D = 22.5 A, V_{DS} = 10 V Note3
Input capacitance	Ciss	—	6200	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	780	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	410	—	pF	f = 1 MHz
Total gate charge	Qg	—	95	—	nc	V_{DD} = 10 V
Gate to source charge	Qgs	—	24	—	nc	V_{GS} = 10 V
Gate to drain charge	Qgd	—	14	—	nc	I_D = 45 A
Turn-on delay time	$t_{d(on)}$	—	27	—	ns	V_{GS} = 10 V, I_D = 22.5 A
Rise time	t_r	—	50	—	ns	V_{DD} ≅ 10 V
Turn-off delay time	$t_{d(off)}$	—	90	—	ns	R_L = 0.44 Ω
Fall time	t_f	—	14	—	ns	Rg = 4.7 Ω
Body–drain diode forward voltage	V_{DF}	—	0.84	1.10	V	IF = 45 A, V_{GS} = 0 Note3
Body–drain diode reverse recovery time	t_{rr}	—	40	—	ns	IF = 45 A, V_{GS} = 0 diF/ dt = 100 A/ µs

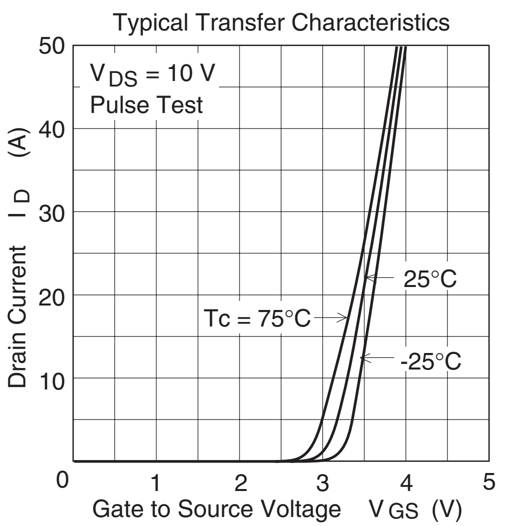
Notes: 3. Pulse test

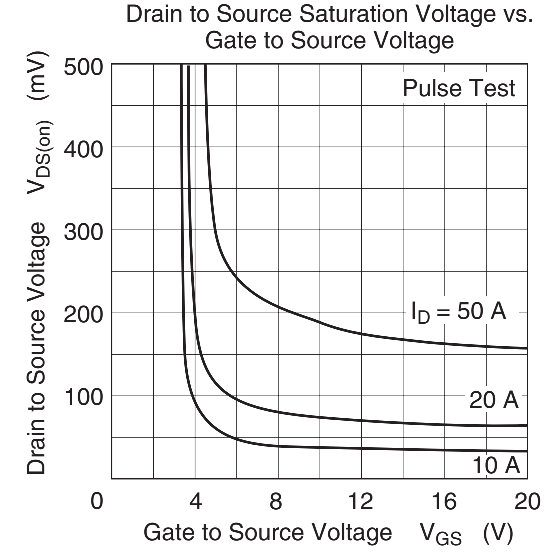
Main Characteristics

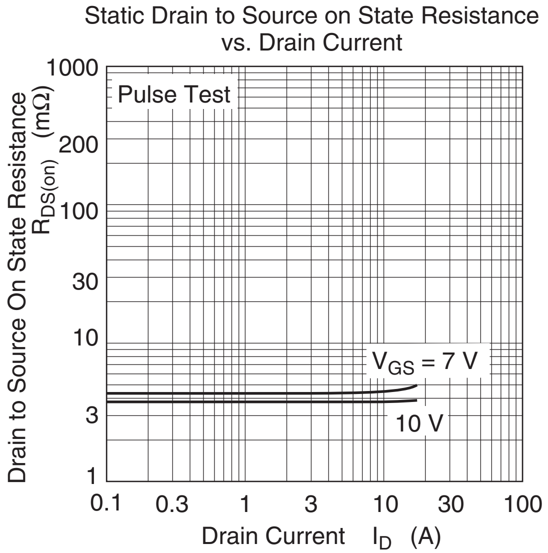


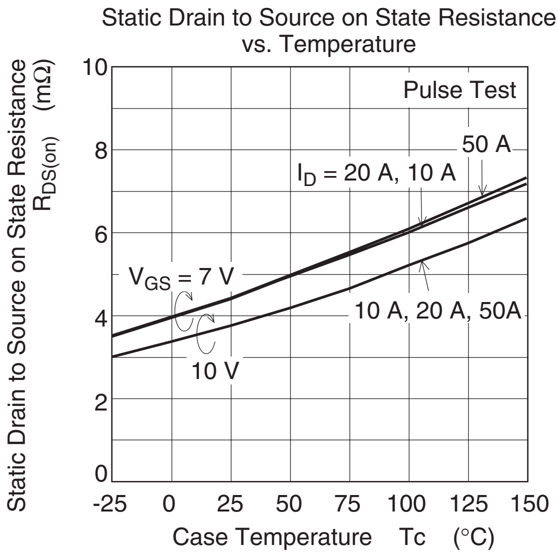


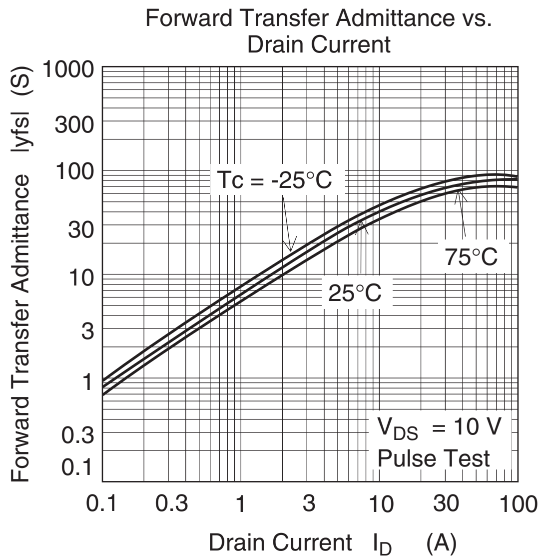





Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I_D = 50 A
20 A
10 A
Drain to Source Voltage V_DS(on) (mV)
500
400
300
200
100
0
4
8
12
16
20
Gate to Source Voltage V_GS (V)


Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V_GS = 7 V
10 V
Drain to Source On State Resistance R_DS(on) (mΩ)
1000
200
100
30
10
3
1
0.1
0.3
1
3
10
30
100
Drain Current I_D (A)


Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
50 A
I_D = 20 A, 10 A
V_GS = 7 V
10 A, 20 A, 50A
10 V
Static Drain to Source on State Resistance R_DS(on) (mΩ)
10
8
6
4
2
0
-25
0
25
50
75
100
125
150
Case Temperature Tc (°C)


Forward Transfer Admittance vs.
Drain Current
Tc = -25°C
75°C
25°C
V_DS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
1000
300
100
30
10
3
1
0.3
0.1
0.1
0.3
1
3
10
30
100
Drain Current I_D (A)

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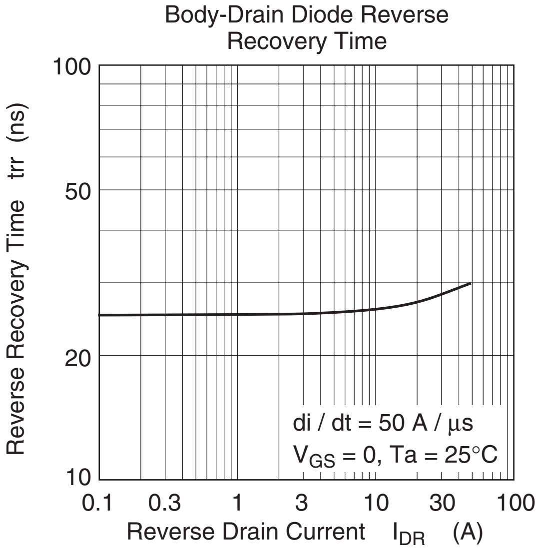
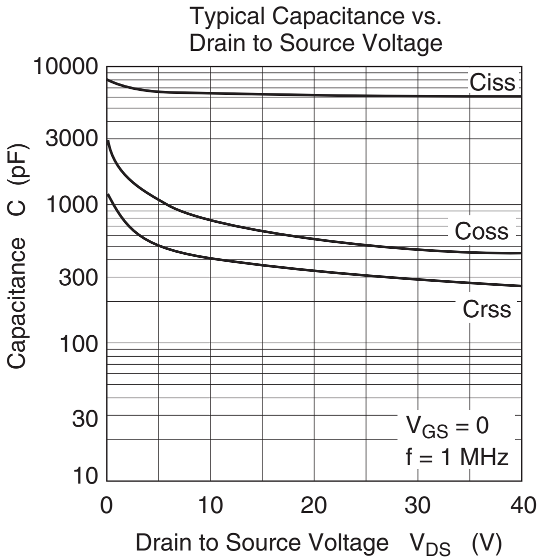
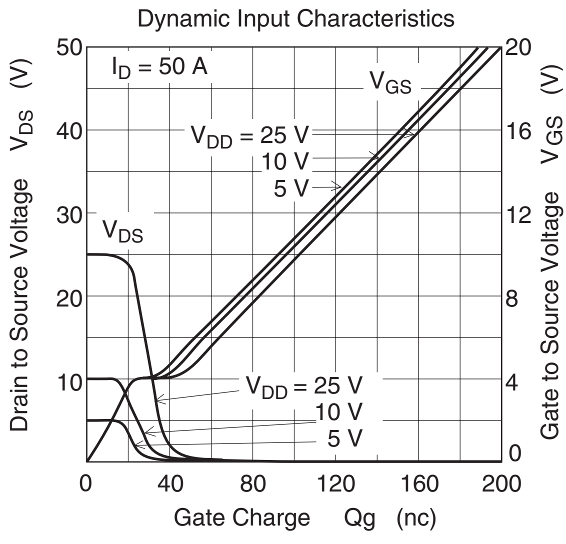
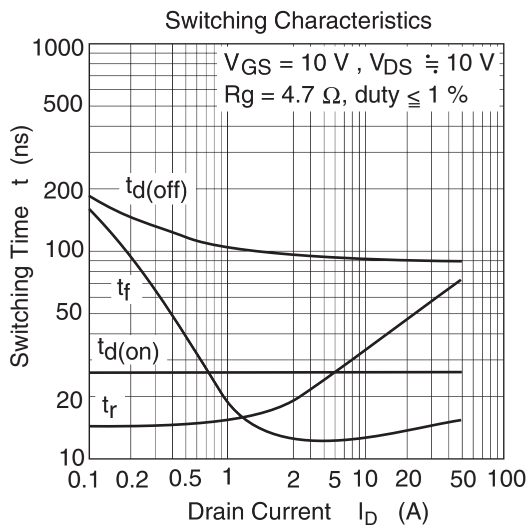
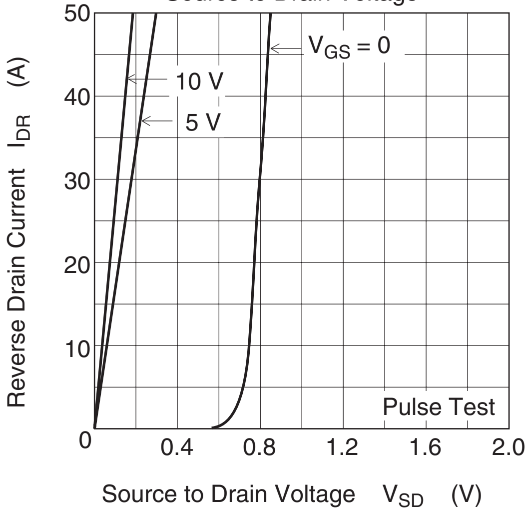

Body-Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
100
50
20
10
0.1
0.3
1
3
10
30
100
Reverse Drain Current I_{DR} (A)
di / dt = 50 A / µs
V_{GS} = 0, Ta = 25°C


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
0
10
20
30
40
Drain to Source Voltage V_{DS} (V)
Ciss
Coss
Crss
V_{GS} = 0
f = 1 MHz

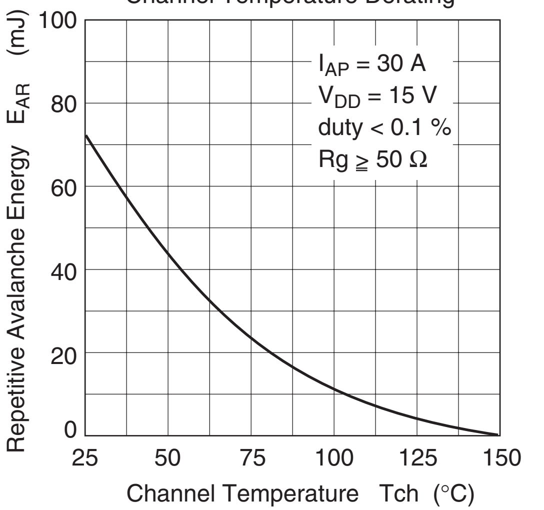

Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
50
40
30
20
10
0
20
16
12
8
4
0
40
80
120
160
200
Gate Charge Qg (nc)
I_D = 50 A
V_{GS}
V_{DD} = 25 V
10 V
5 V
V_{DS}
V_{DD} = 25 V
10 V
5 V


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
0.1
0.2
0.5
1
2
5
10
20
50
100
Drain Current I_D (A)
V_{GS} = 10 V , V_{DS} ≒ 10 V
Rg = 4.7 Ω, duty ≦ 1 %
$t_{d(off)}$
t_f
$t_{d(on)}$
t_r

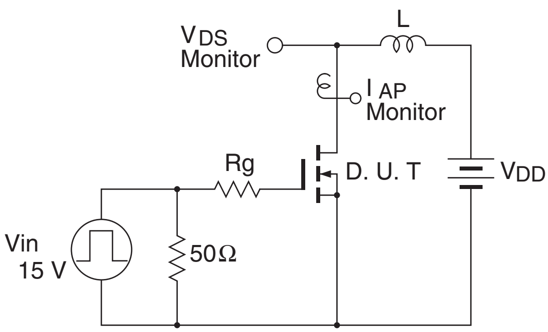
Reverse Drain Current vs. Source to Drain Voltage



Maximum Avalanche Energy vs. Channel Temperature Derating

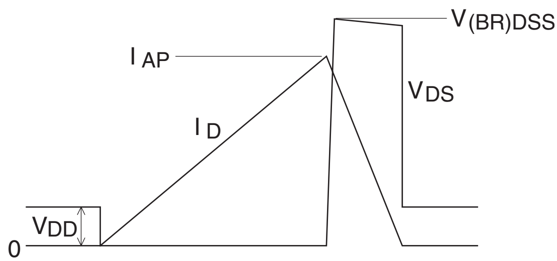


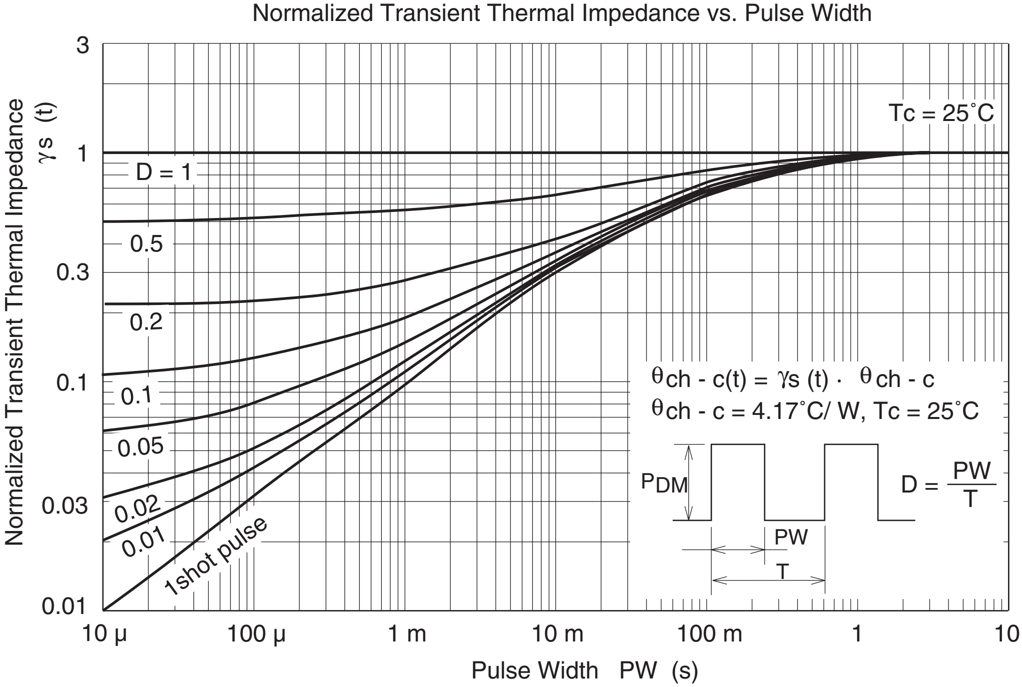
Avalanche Test Circuit

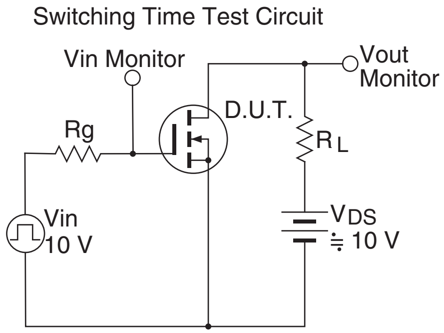


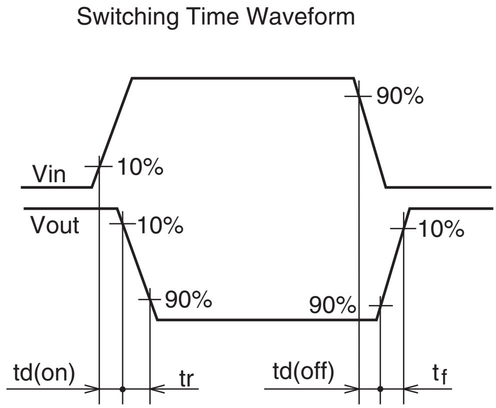
Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \bullet I_{AP}{}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



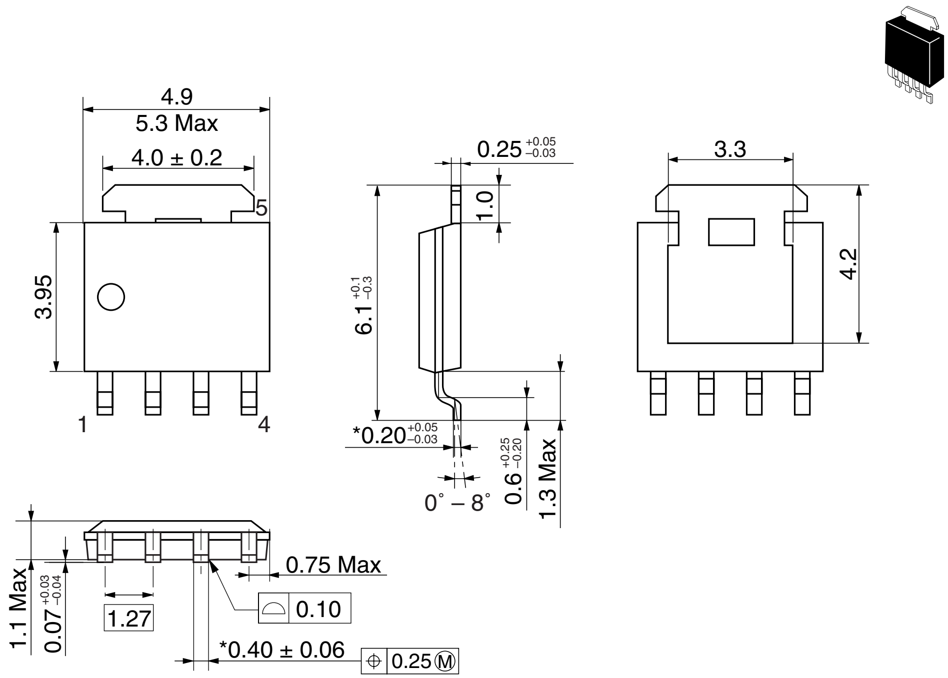

Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch - c(t) = γs (t) · θch - c
θch - c = 4.17°C/ W, Tc = 25°C
PDM
D = PW / T
PW
T
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (s)


Switching Time Test Circuit
Vin Monitor
Vout Monitor
D.U.T.
Rg
RL
Vin
10 V
VDS
≒ 10 V


Switching Time Waveform
Vin
Vout
90%
10%
10%
10%
90%
90%
td(on)
tr
td(off)
tf

Package Dimensions

As of July, 2002
Unit: mm



Hitachi Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

*Ni/Pd/Au plating

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