

HAT2139H

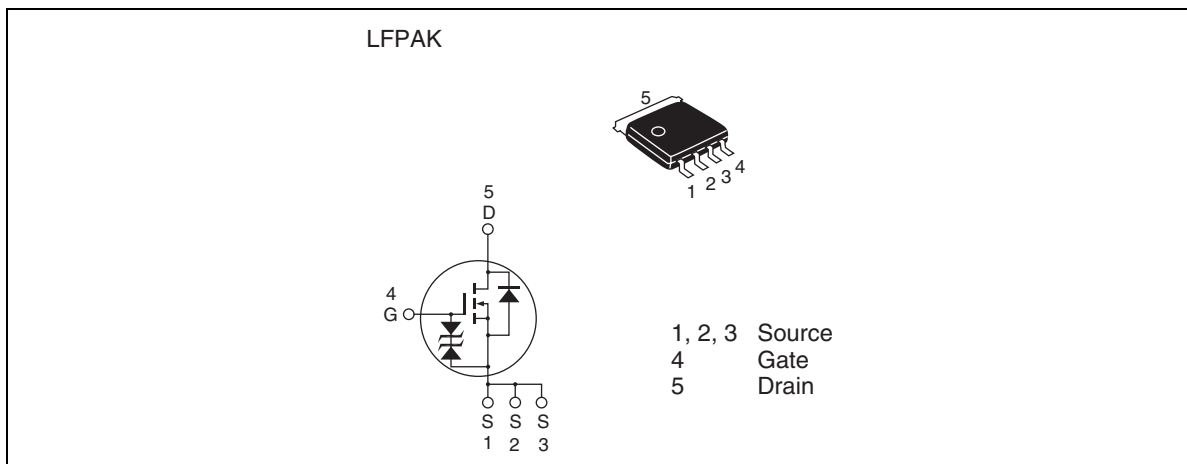
Silicon N Channel Power MOS FET
Power Switching

REJ03G0055-0400Z
(Previous ADE-208-1580A(Z))
Rev.4.00
Jul.15.2003

Features

- Capable of 7 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 9 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	40	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	20	A
Drain peak current	I _{D(pulse)} ^{Note1}	80	A
Body-drain diode reverse drain current	I _{DR}	20	A
Avalanche current	I _{AP} ^{Note 3}	10	A
Avalanche energy	E _{AR} ^{Note 3}	8	mJ
Channel dissipation	P _{ch} ^{Note2}	15	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

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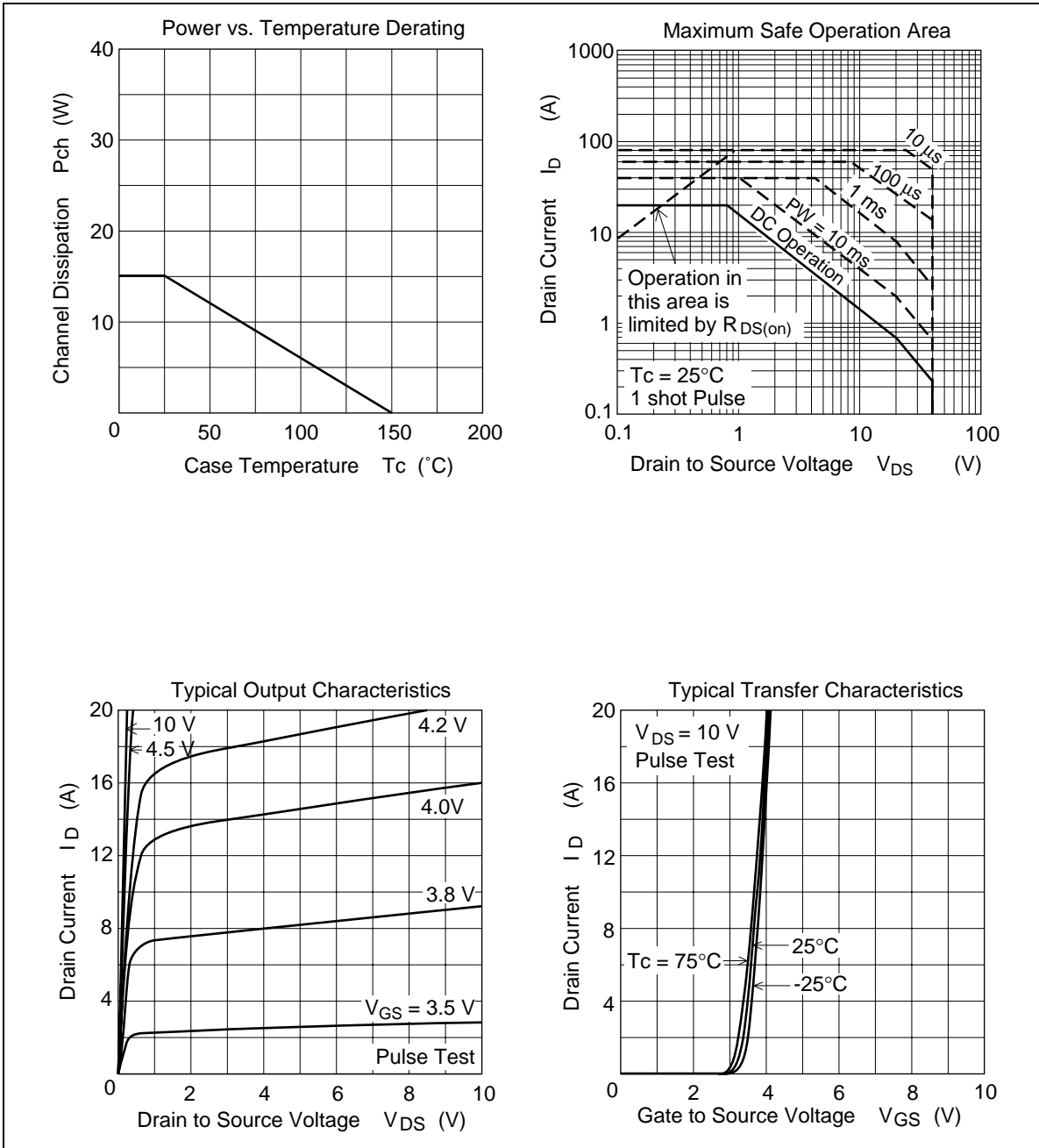
Electrical Characteristics

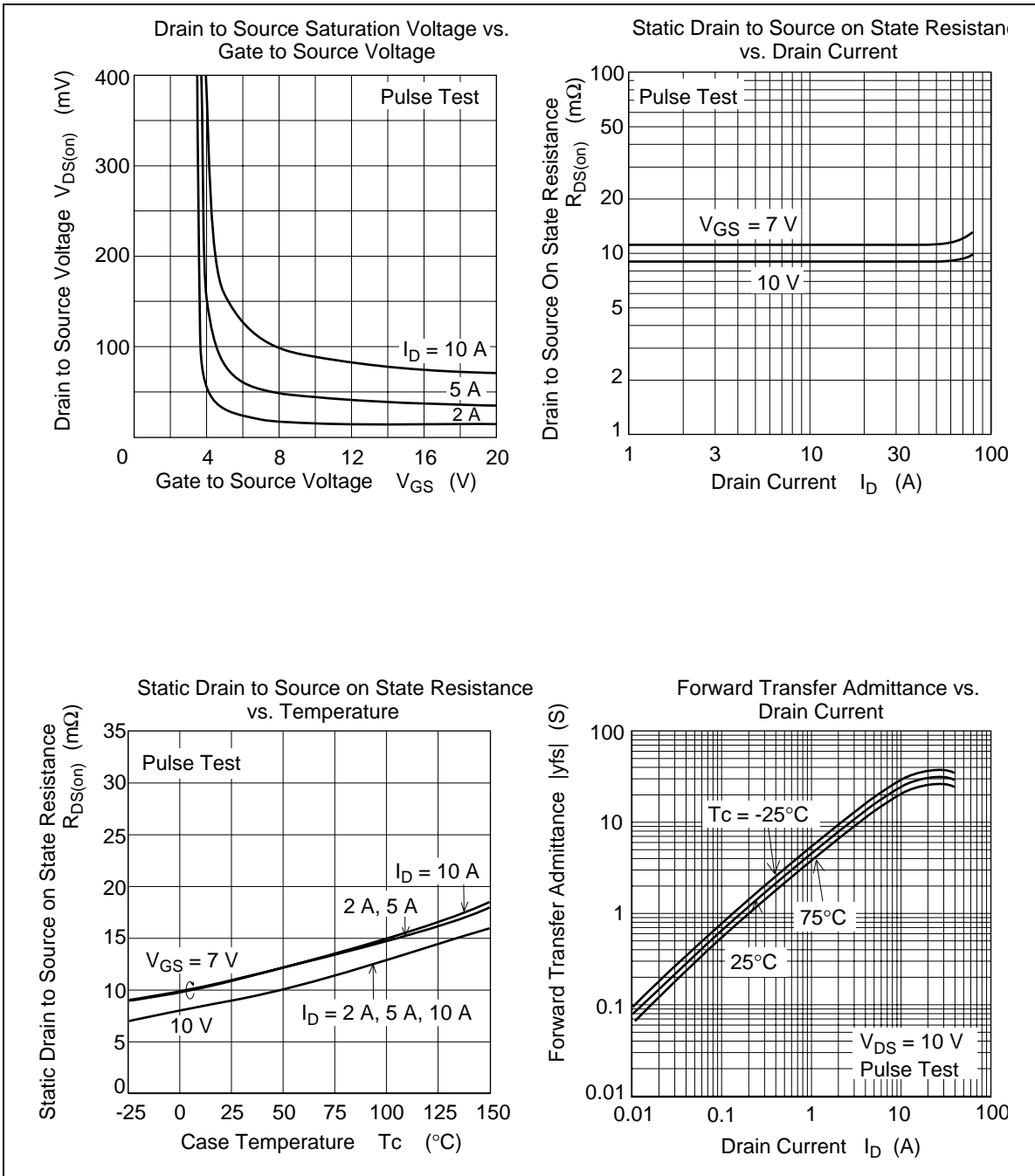
(Ta = 25°C)

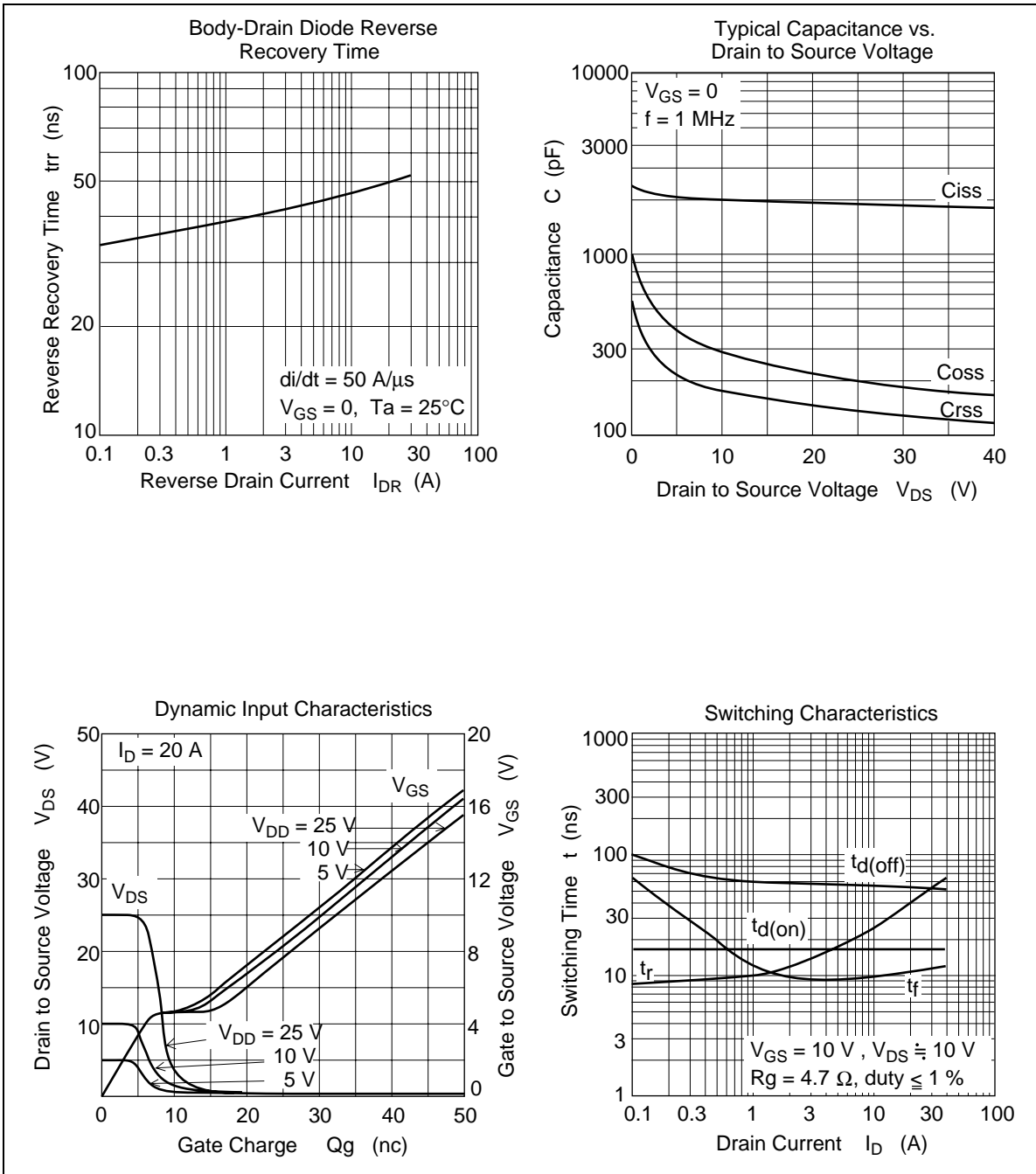
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 40 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	9.0	11.5	$\text{m}\Omega$	$I_D = 10 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	11.0	15.0	$\text{m}\Omega$	$I_D = 10 \text{ A}$, $V_{GS} = 7 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	15	25	—	S	$I_D = 10 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	2000	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	290	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	175	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	30	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	8	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	5	—	nc	$I_D = 20 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	17	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$
Rise time	t_r	—	23	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	58	—	ns	$R_L = 1.0 \text{ }\Omega$
Fall time	t_f	—	10	—	ns	$R_g = 4.7 \text{ }\Omega$
Body–drain diode forward voltage	V_{DF}	—	0.83	1.08	V	$I_F = 20 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body–drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = 20 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu\text{s}$

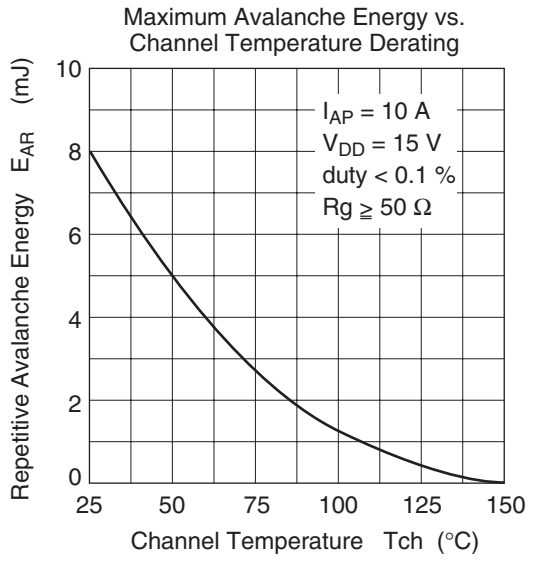
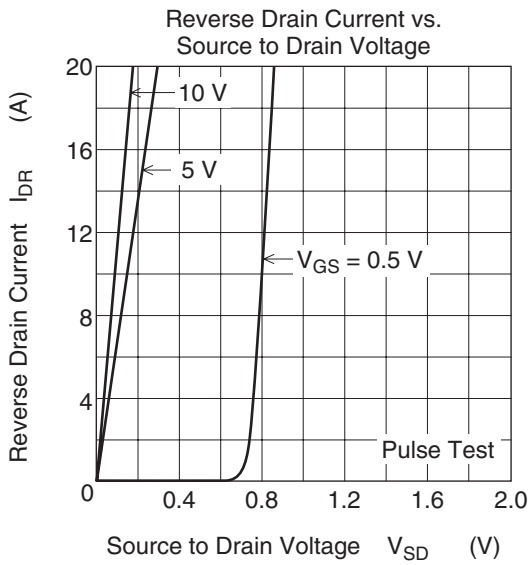
Notes: 4. Pulse test

Main Characteristics

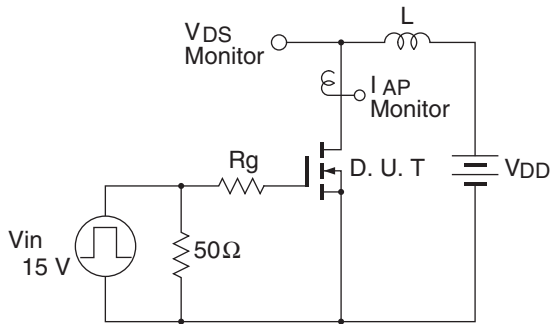






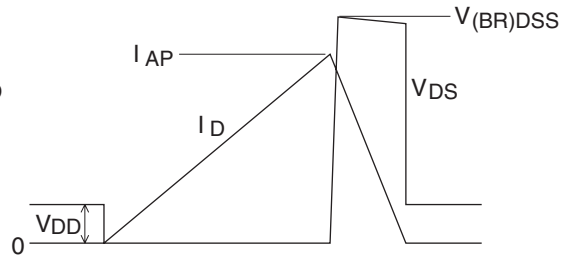


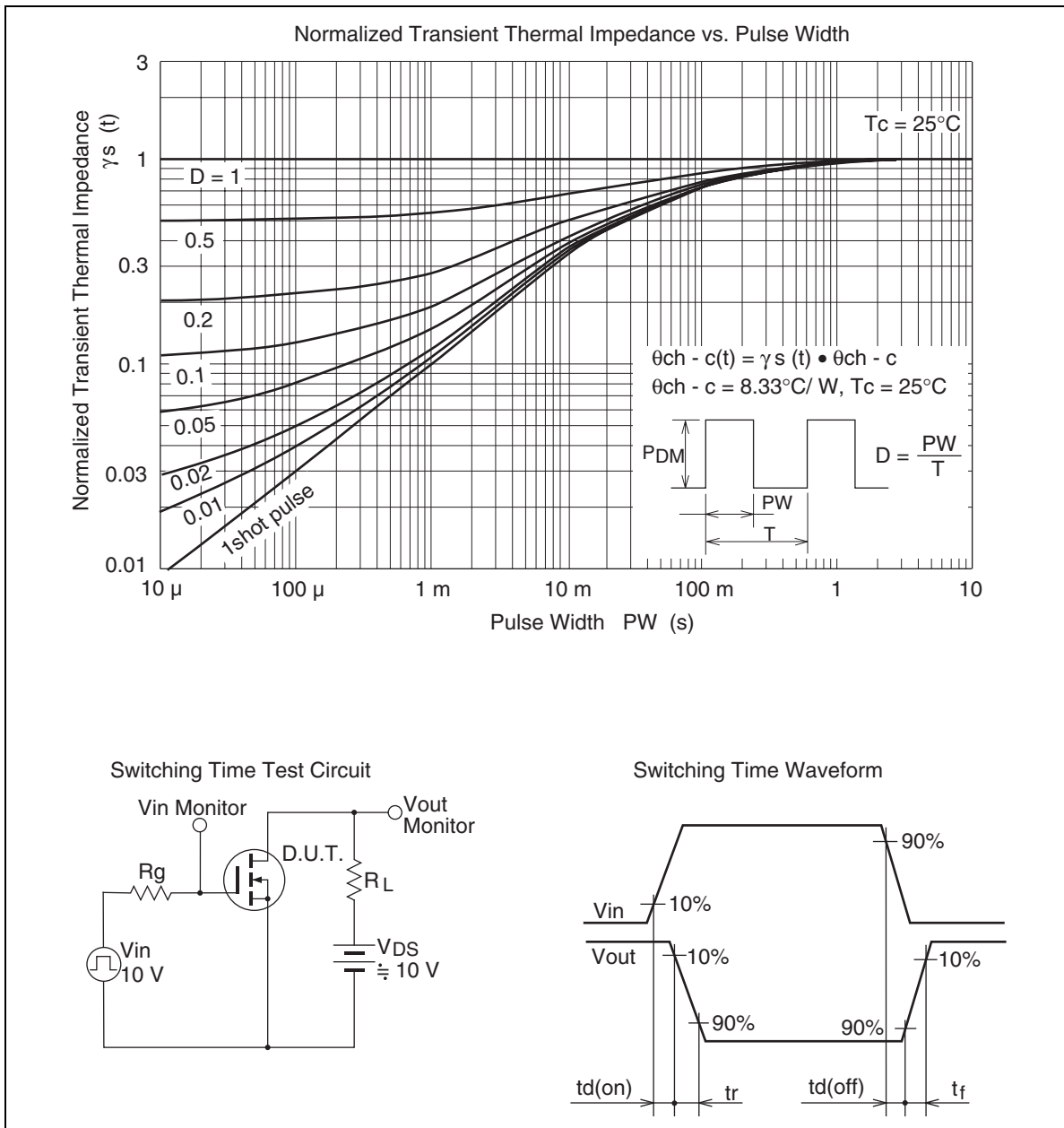
Avalanche Test Circuit



Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

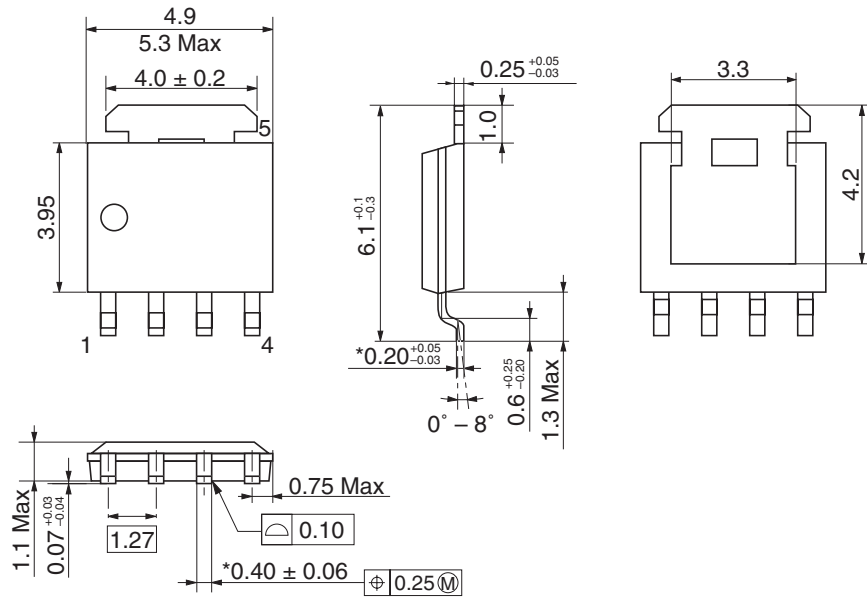
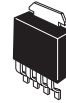




Package Dimensions

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

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Keep safety first in your circuit designs!

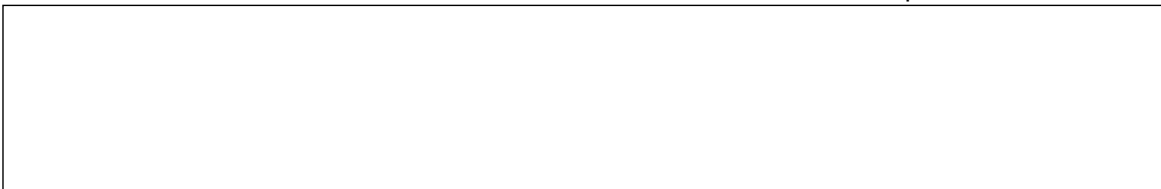
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