To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HAT2141H

Silicon N Channel Power MOS FET
Power Switching

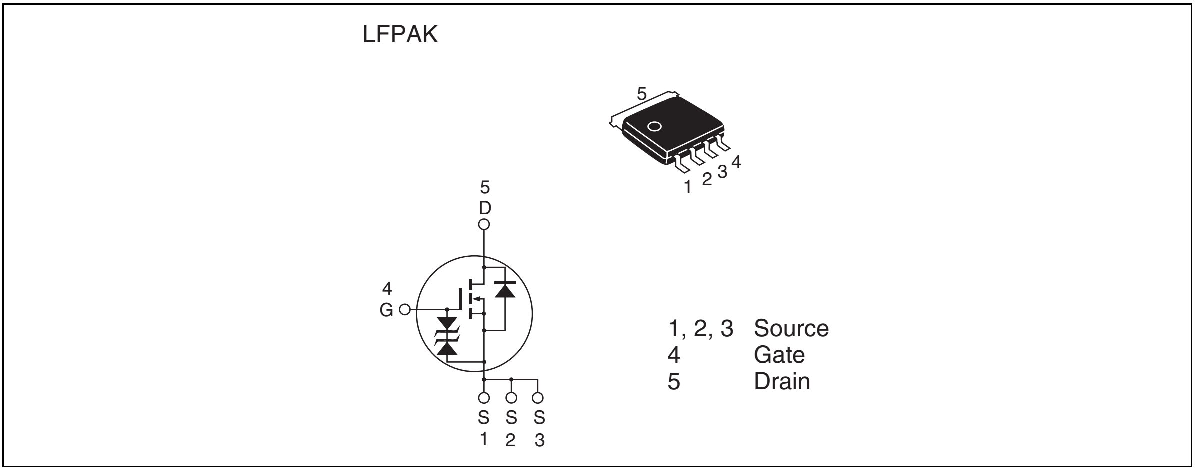
ADE-208-1582E(Z)

Preliminary
6th. Edition
Sep. 2002

Features

- Capable of 7 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 22 mΩ typ. (at V_{GS} = 10 V)

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$ Note1	60	A
Body-drain diode reverse drain current	I_{DR}	15	A
Avalanche current	I_{AP} Note 3	15	A
Avalanche energy	E_{AR} Note 3	22.5	mJ
Channel dissipation	Pch Note2	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to + 150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

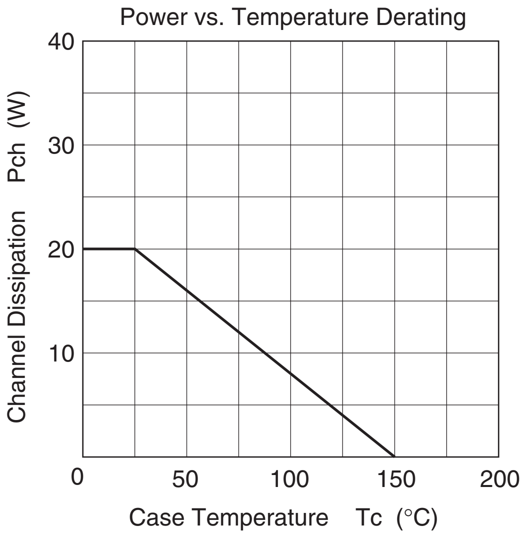
Electrical Characteristics

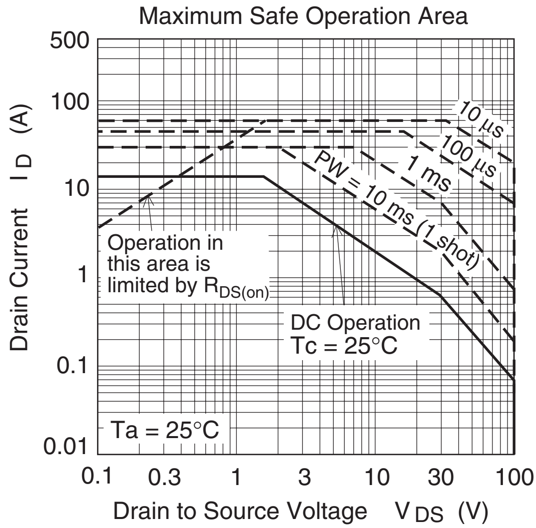
(Ta = 25°C)

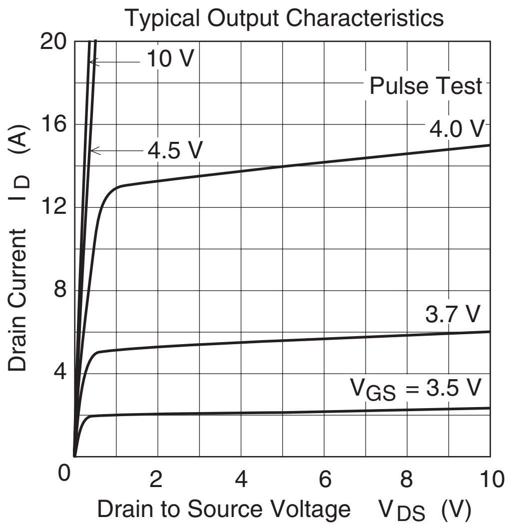
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	I_G = ±100 μA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	± 10	μA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	V_{DS} = 100 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	22	27.5	mΩ	I_D = 7.5 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	23.5	32	mΩ	I_D = 7.5 A, V_{GS} = 7 V Note4
Forward transfer admittance	$\|y_{fs}\|$	15	25	—	S	I_D = 7.5 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	3200	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	255	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	125	—	pF	f = 1 MHz
Total gate charge	Qg	—	46	—	nc	V_{DD} = 50 V
Gate to source charge	Qgs	—	11	—	nc	V_{GS} = 10 V
Gate to drain charge	Qgd	—	10	—	nc	I_D = 15 A
Turn-on delay time	$t_{d(on)}$	—	22	—	ns	V_{GS} = 10 V, I_D = 7.5 A
Rise time	t_r	—	13	—	ns	V_{DD} ≅ 30 V
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	R_L = 4 Ω
Fall time	t_f	—	10	—	ns	Rg = 4.7 Ω
Body–drain diode forward voltage	V_{DF}	—	0.82	1.07	V	IF = 15 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	50	—	ns	IF = 15 A, V_{GS} = 0 diF/ dt = 100 A/ μs

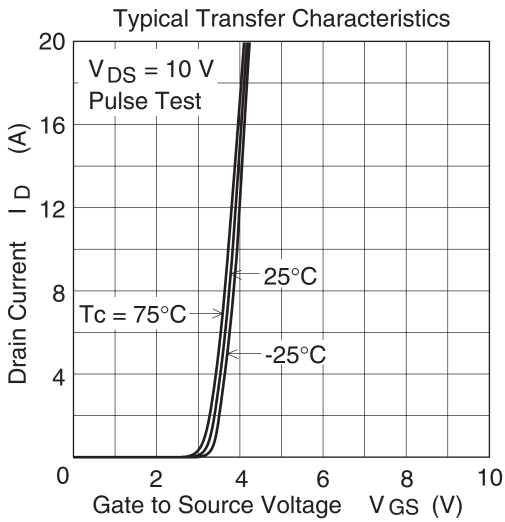
Notes: 4. Pulse test

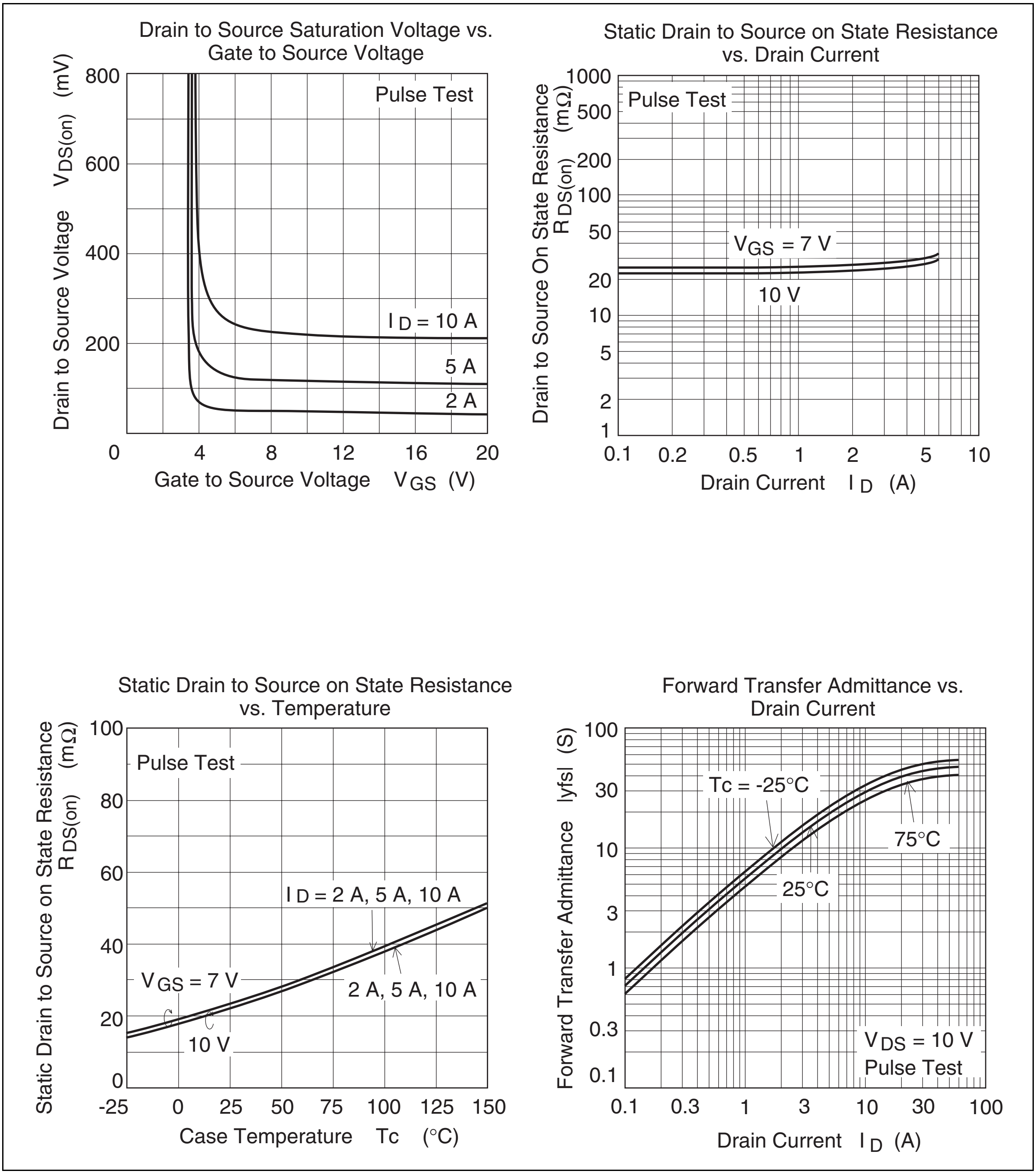
Main Characteristics



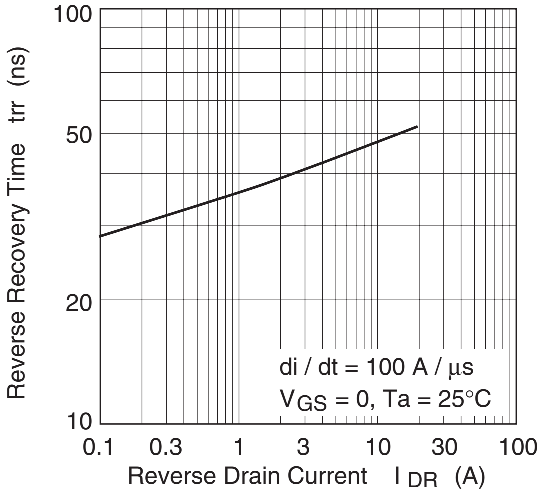




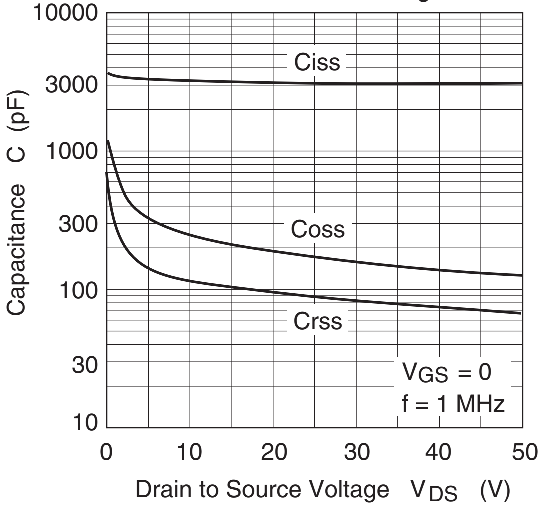



Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = 10 A
5 A
2 A
Drain to Source Voltage V DS(on) (mV)
0
200
400
600
800
4
8
12
16
20
Gate to Source Voltage V GS (V)
Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = 7 V
10 V
Drain to Source On State Resistance R DS(on) (mΩ)
1000
500
200
100
50
20
10
5
2
1
0.1
0.2
0.5
1
2
5
10
Drain Current I D (A)
Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = 2 A, 5 A, 10 A
V GS = 7 V
2 A, 5 A, 10 A
10 V
Static Drain to Source on State Resistance R DS(on) (mΩ)
100
80
60
40
20
0
-25
0
25
50
75
100
125
150
Case Temperature Tc (°C)
Forward Transfer Admittance vs.
Drain Current
Tc = -25°C
75°C
25°C
V DS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
100
30
10
3
1
0.3
0.1
0.1
0.3
1
3
10
30
100
Drain Current I D (A)

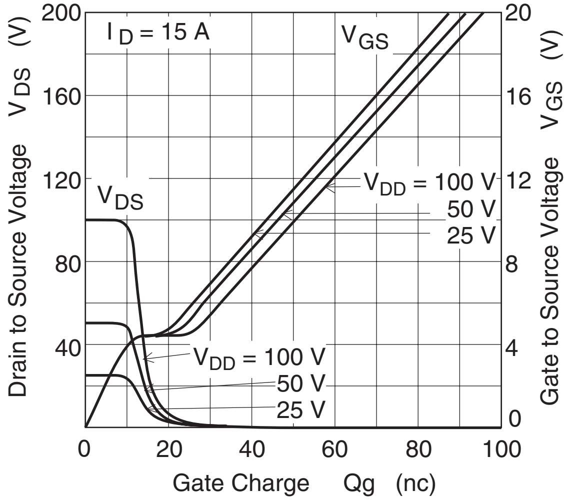
Body-Drain Diode Reverse Recovery Time



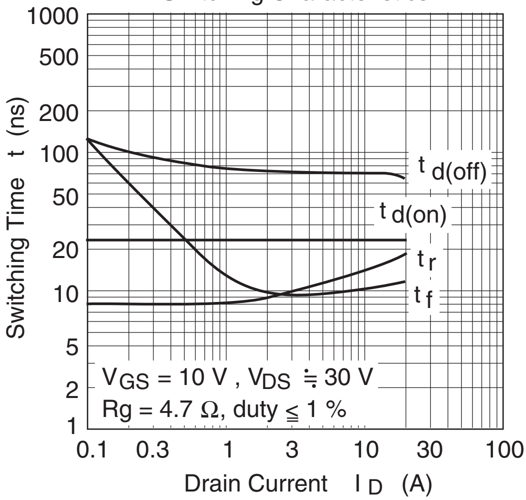
Typical Capacitance vs. Drain to Source Voltage



Dynamic Input Characteristics



Switching Characteristics



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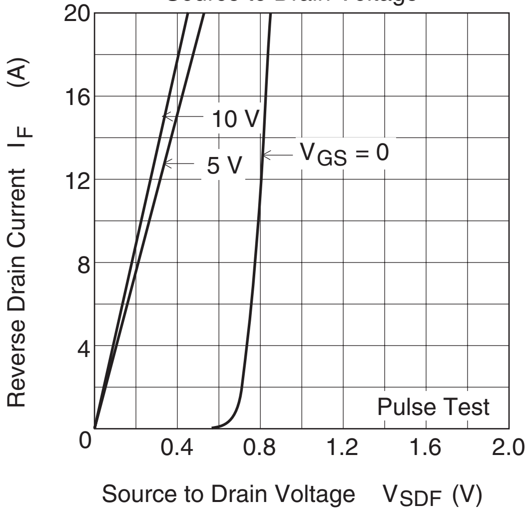
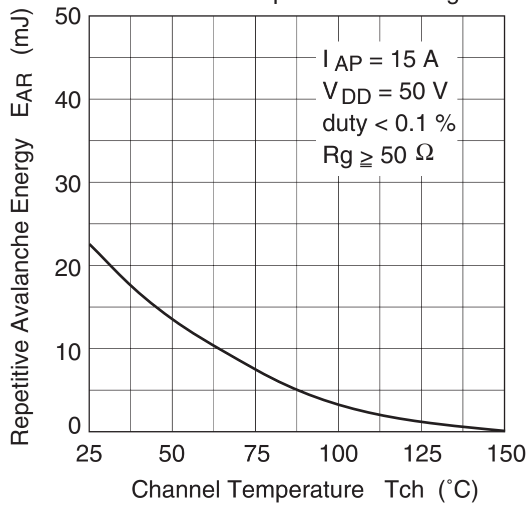
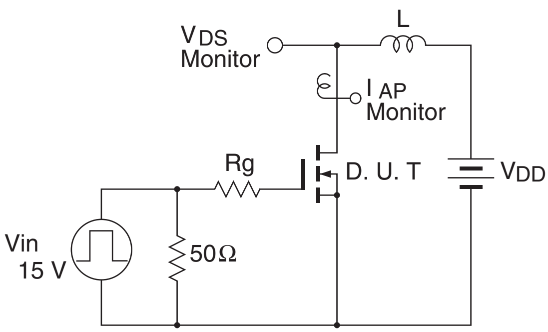
Reverse Drain Current vs. Source to Drain Voltage



Maximum Avalanche Energy vs. Channel Temperature Derating

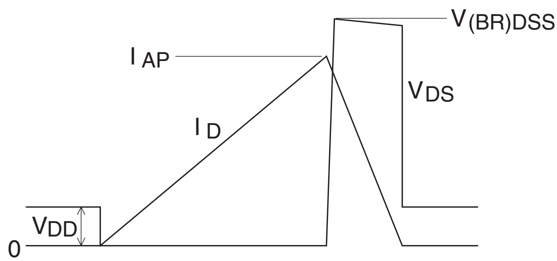


Avalanche Test Circuit

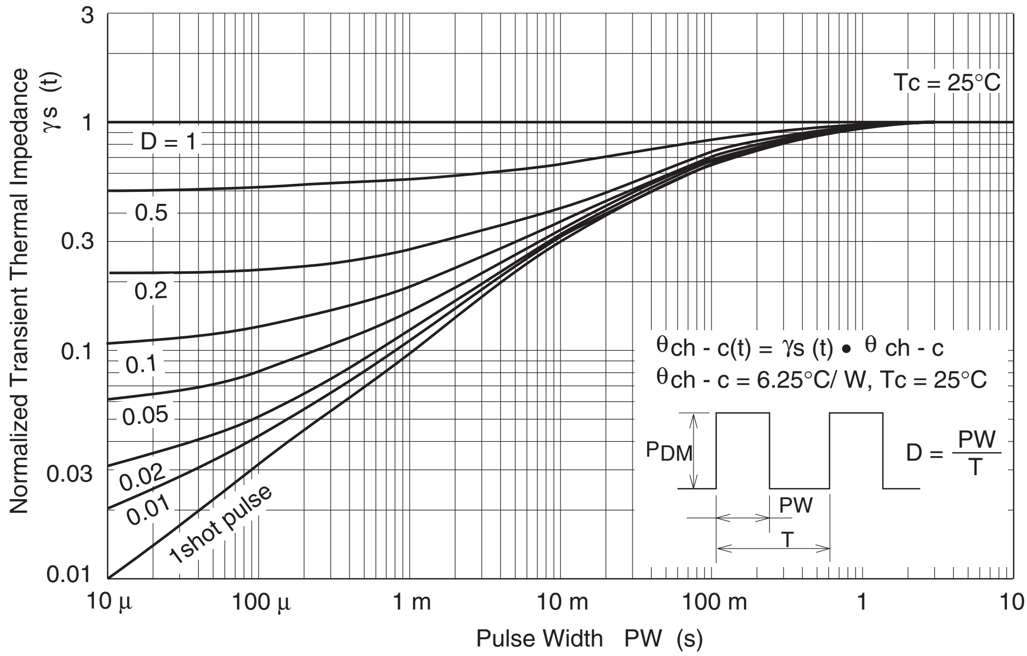


Avalanche Waveform

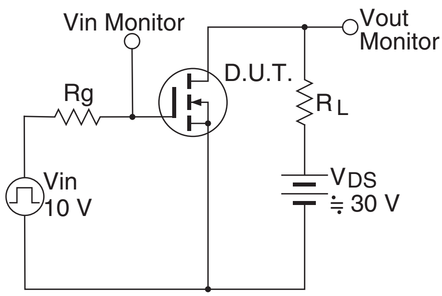
$$E_{AR} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



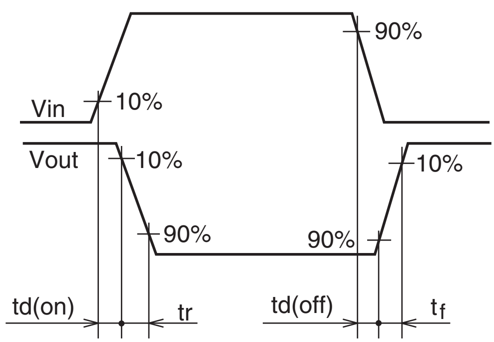
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

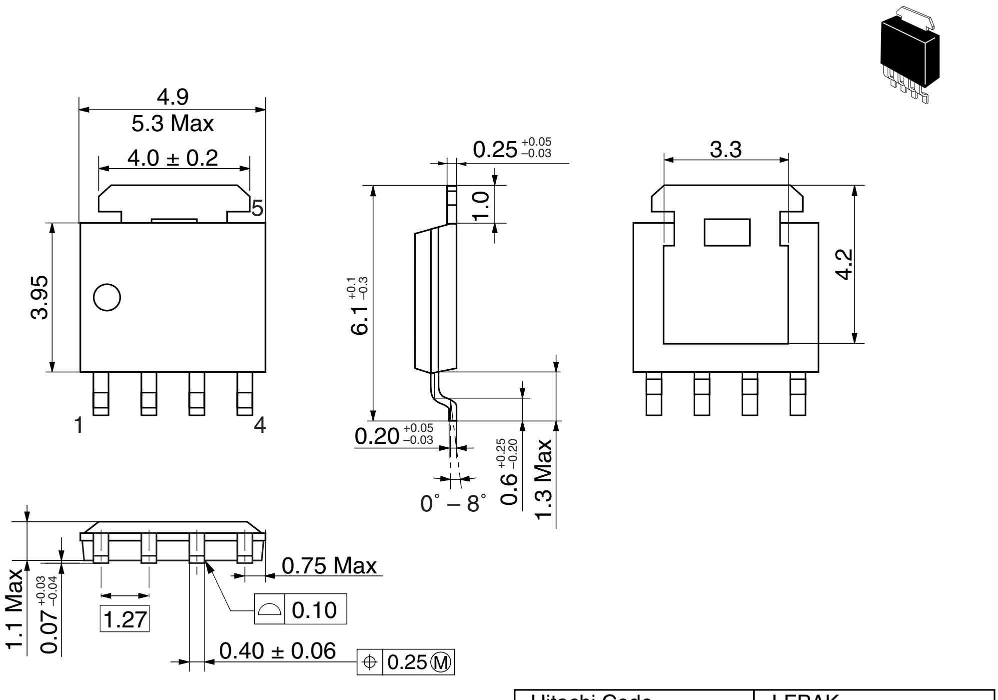


Switching Time Waveform



Package Dimensions

As of July, 2002
Unit: mm



Hitachi Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

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