

## HAT2175H

### Silicon N Channel Power MOS FET Power Switching

REJ03G0006-0300Z

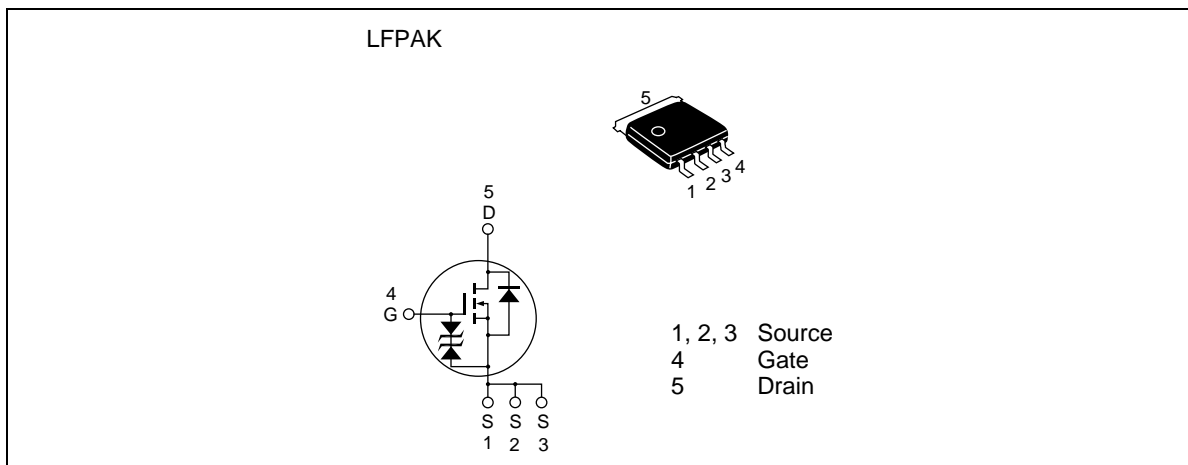
Rev.3.00

Apr.14.2003

#### Features

- Capable of 8 V gate drive
- Low drive current
- High density mounting
- Low on-resistance  
 $R_{DS(on)} = 33 \text{ m}\Omega$  typ. (at  $V_{GS} = 10 \text{ V}$ )

#### Outline



**Absolute Maximum Ratings**

(Ta = 25°C)

<b>Item</b>	<b>Symbol</b>	<b>Ratings</b>	<b>Unit</b>
Drain to source voltage	V <sub>DSS</sub>	100	V
Gate to source voltage	V <sub>GSS</sub>	± 20	V
Drain current	I <sub>D</sub>	15	A
Drain peak current	I <sub>D(pulse)</sub> <sup>Note1</sup>	60	A
Body-drain diode reverse drain current	I <sub>DR</sub>	15	A
Avalanche current	I <sub>AP</sub> <sup>Note 2</sup>	15	A
Avalanche energy	E <sub>AR</sub> <sup>Note 2</sup>	22.5	mJ
Channel dissipation	P <sub>ch</sub> <sup>Note3</sup>	15	W
Channel to Case Thermal Resistance	θ <sub>ch-C</sub>	8.34	°C/W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
2. Value at T<sub>ch</sub> = 25°C, R<sub>g</sub> ≥ 50 Ω  
3. T<sub>c</sub> = 25°C

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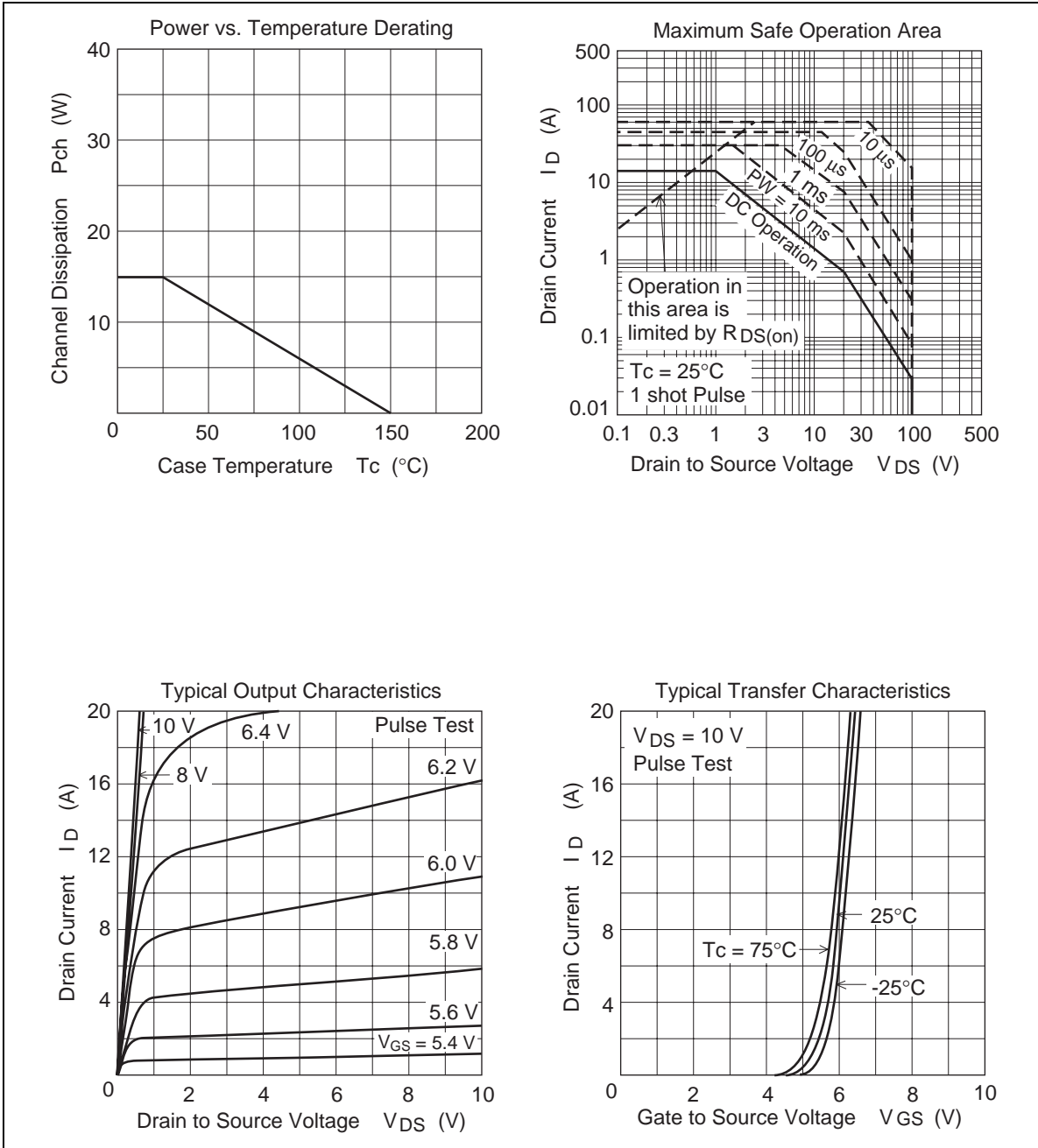
### Electrical Characteristics

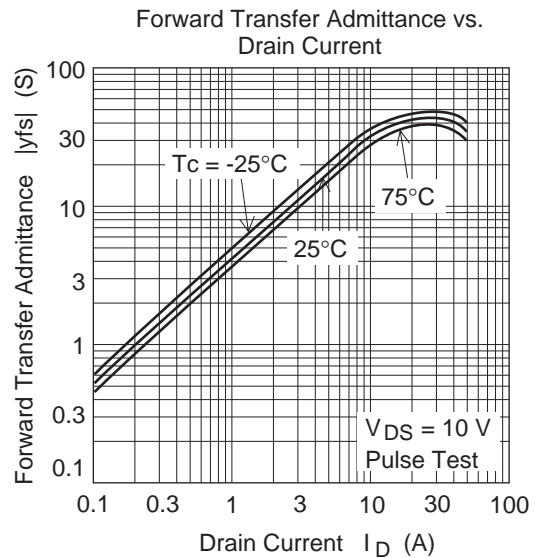
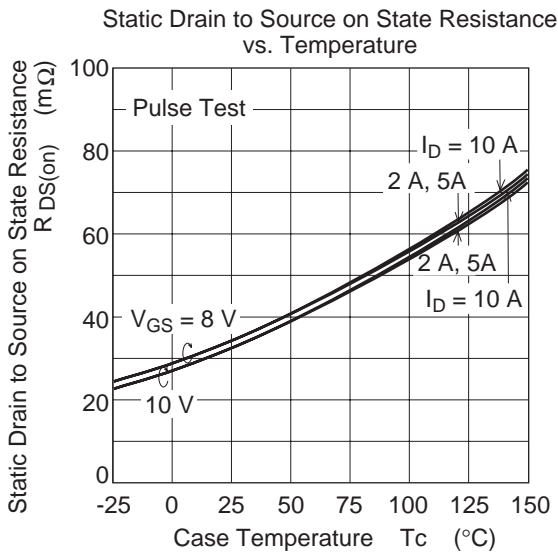
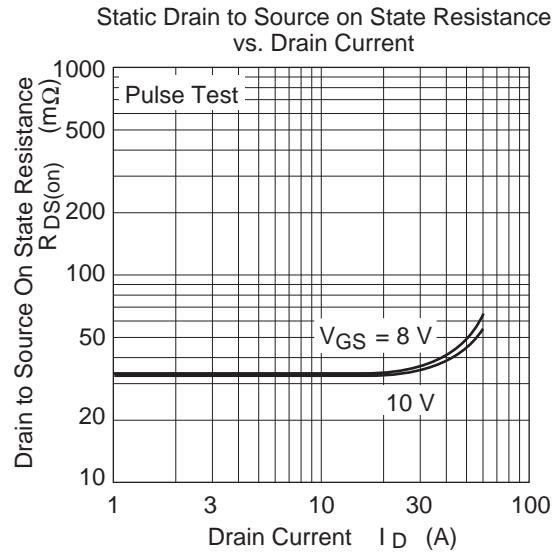
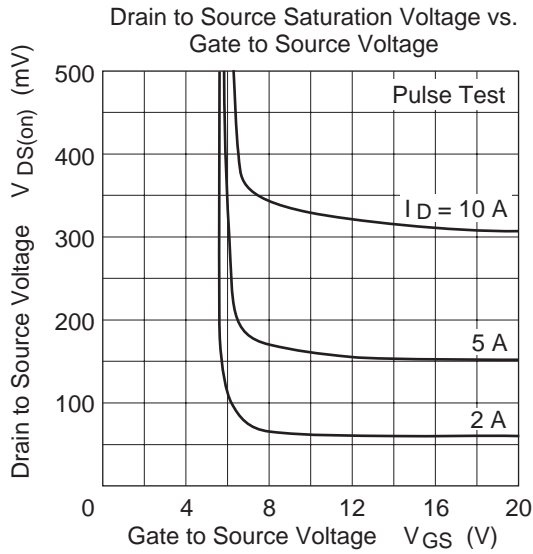
(T<sub>a</sub> = 25°C)

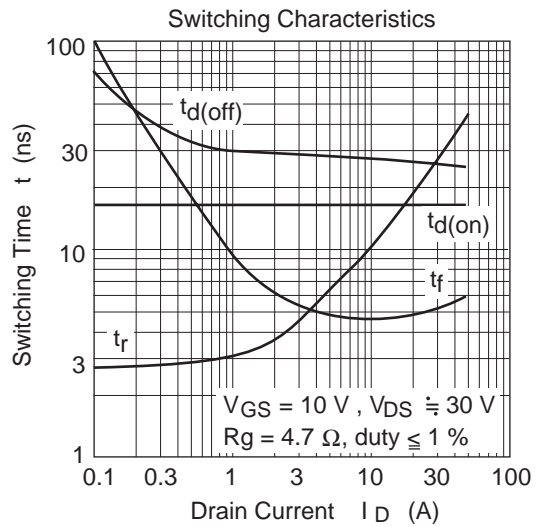
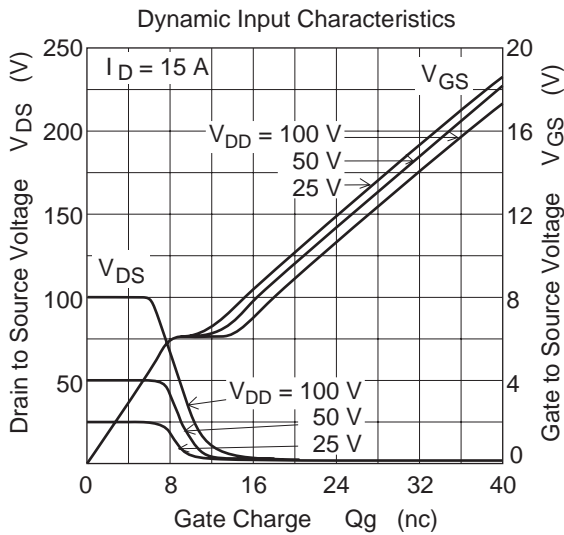
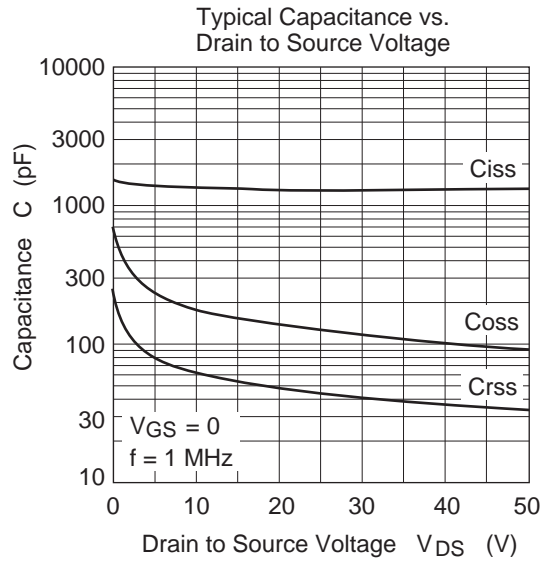
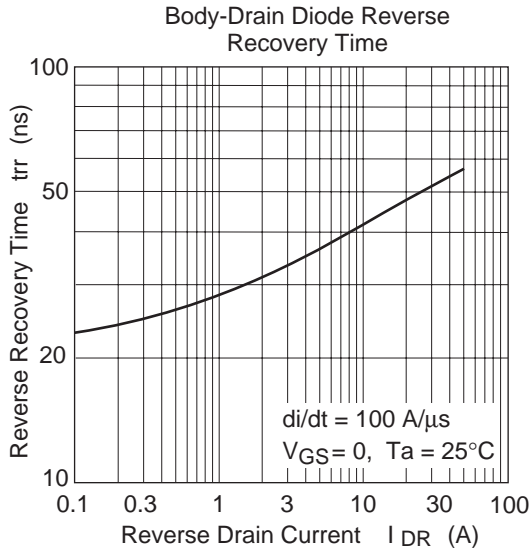
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	100	—	—	V	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0
Gate to source breakdown voltage	V <sub>(BR)GSS</sub>	± 20	—	—	V	I <sub>G</sub> = ±100 μA, V <sub>DS</sub> = 0
Gate to source leak current	I <sub>GSS</sub>	—	—	± 10	μA	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0
Gate to source cutoff voltage	V <sub>GS(off)</sub>	4.0	—	6.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 20mA
Static drain to source on state resistance	R <sub>DS(on)</sub>	—	33	42	mΩ	I <sub>D</sub> = 7.5 A, V <sub>GS</sub> = 10 V <sup>Note4</sup>
	R <sub>DS(on)</sub>	—	34	46	mΩ	I <sub>D</sub> = 7.5 A, V <sub>GS</sub> = 8 V <sup>Note4</sup>
Forward transfer admittance	y <sub>fs</sub>	15	25	—	S	I <sub>D</sub> = 7.5 A, V <sub>DS</sub> = 10 V <sup>Note4</sup>
Input capacitance	C <sub>iss</sub>	—	1445	—	pF	V <sub>DS</sub> = 10 V
Output capacitance	C <sub>oss</sub>	—	185	—	pF	V <sub>GS</sub> = 0
Reverse transfer capacitance	C <sub>rss</sub>	—	61	—	pF	f = 1 MHz
Gate Resistance	R <sub>g</sub>	—	0.55	—	Ω	
Total gate charge	Q <sub>g</sub>	—	21	—	nc	V <sub>DD</sub> = 50 V
Gate to source charge	Q <sub>gs</sub>	—	8	—	nc	V <sub>GS</sub> = 10 V
Gate to drain charge	Q <sub>gd</sub>	—	4.5	—	nc	I <sub>D</sub> = 15 A
Turn-on delay time	t <sub>d(on)</sub>	—	17	—	ns	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.5 A
Rise time	t <sub>r</sub>	—	8.2	—	ns	V <sub>DD</sub> ≅ 30 V
Turn-off delay time	t <sub>d(off)</sub>	—	28	—	ns	R <sub>L</sub> = 4 Ω
Fall time	t <sub>f</sub>	—	4.7	—	ns	R <sub>g</sub> = 4.7 Ω
Body–drain diode forward voltage	V <sub>DF</sub>	—	0.84	1.10	V	I <sub>F</sub> = 15 A, V <sub>GS</sub> = 0 <sup>Note4</sup>
Body–drain diode reverse recovery time	t <sub>rr</sub>	—	45	—	ns	I <sub>F</sub> = 15 A, V <sub>GS</sub> = 0 diF/ dt = 100 A/ μs

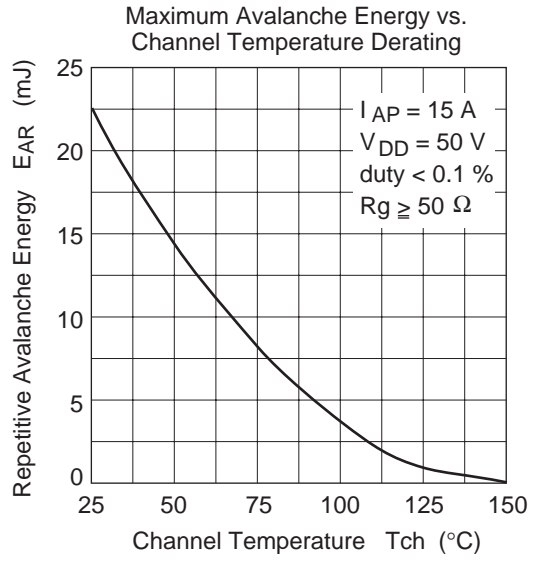
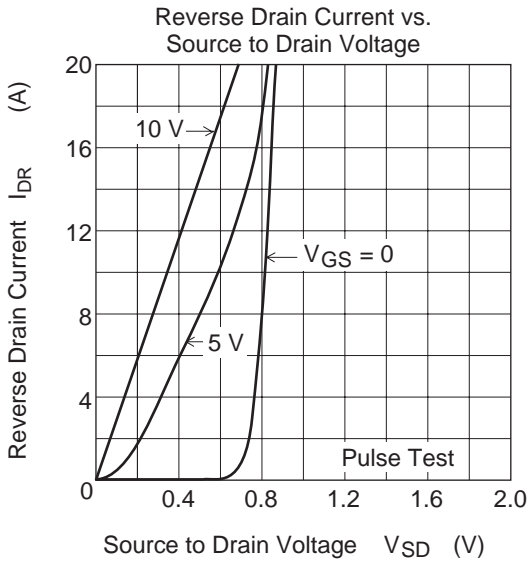
Notes: 4. Pulse test

Main Characteristics

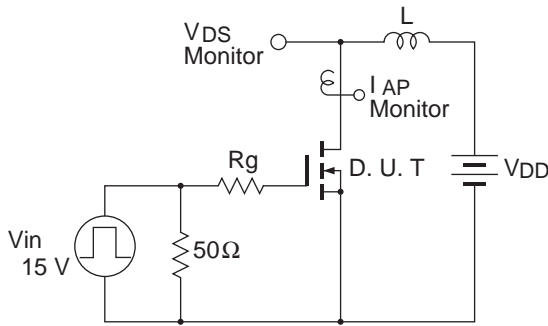






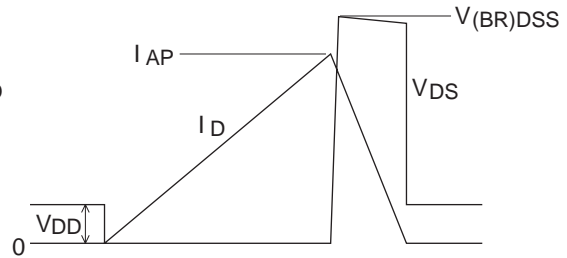


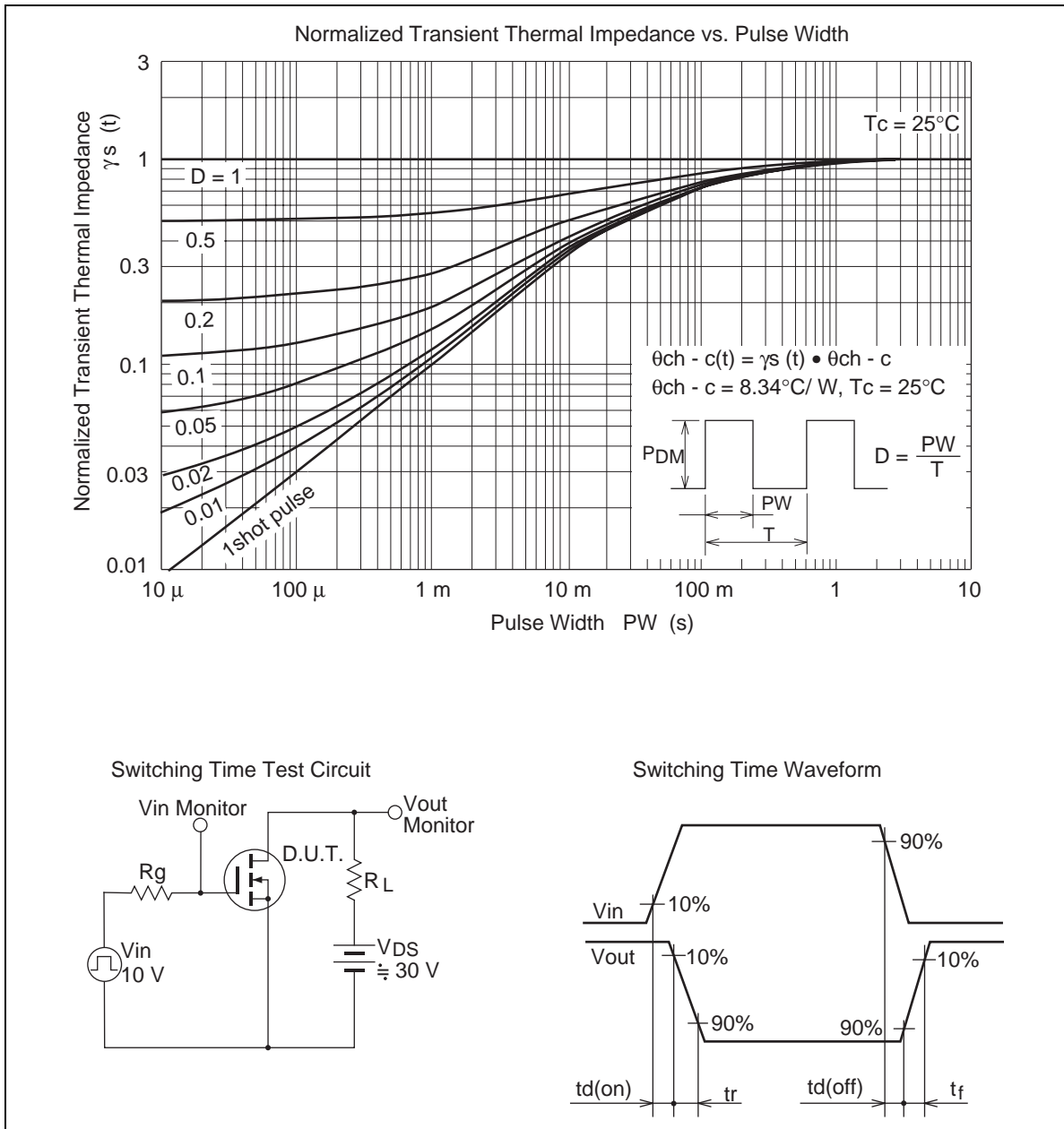
Avalanche Test Circuit



Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

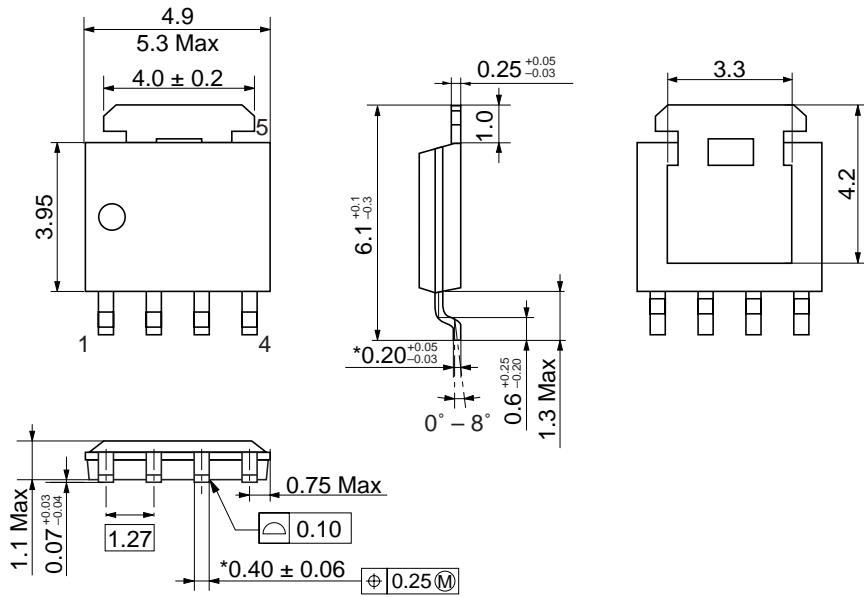
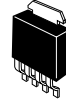




Package Dimensions

As of January, 2003

Unit: mm



\*Ni/Pd/Au plating

Package Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

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**Keep safety first in your circuit designs!**

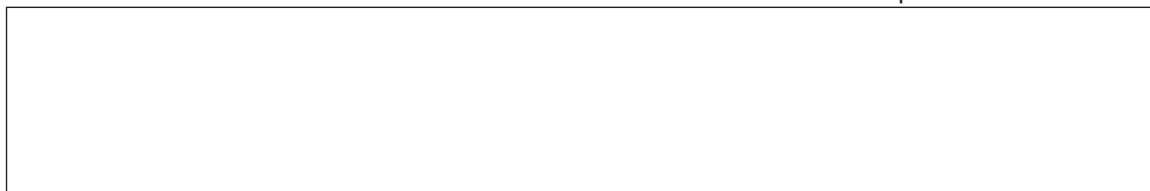
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