# HAT2200R

## Silicon N Channel Power MOS FET
## Power Switching

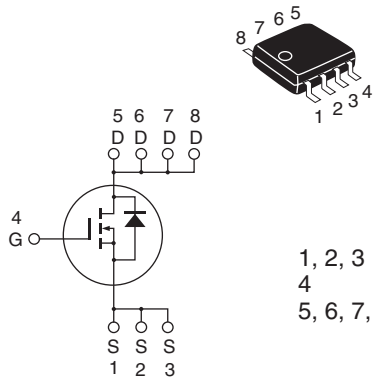
REJ03G0232-0200Z
Rev.2.00
Apr.05.2004

### Features

- Capable of 8 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 22 mΩ typ. (at $V_{GS}$ = 10 V)

### Outline

SOP-8




| | |
|---|---|
| 1, 2, 3 | Source |
| 4 | Gate |
| 5, 6, 7, 8 | Drain |

## Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain to source voltage | $V_{DSS}$ | 100 | V |
| Gate to source voltage | $V_{GSS}$ | ±20 | V |
| Drain current | $I_D$ | 8 | A |
| Drain peak current | $I_{D(pulse)}$ Note1 | 64 | A |
| Body-drain diode reverse drain current | $I_{DR}$ | 8 | A |
| Avalanche current | $I_{AP}$ Note 2 | 8 | A |
| Avalanche energy | $E_{AR}$ Note 2 | 6.4 | mJ |
| Channel dissipation | Pch Note3 | 2.5 | W |
| Channel to Ambient Thermal Impedance | θch-a Note3 | 50 | °C/W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | –55 to +150 | °C |

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

## Electrical Characteristics

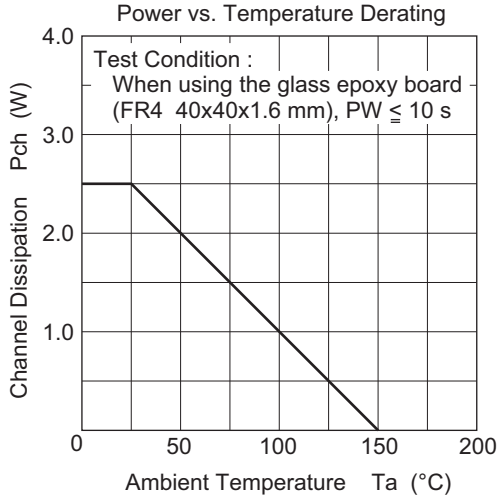
(Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 100 | — | — | V | $I_D$ = 10 mA, $V_{GS}$ = 0 |
| Gate to source leak current | $I_{GSS}$ | — | — | ± 0.1 | µA | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 |
| Zero gate voltage drain current | $I_{DSS}$ | — | — | 1 | µA | $V_{DS}$ = 100 V, $V_{GS}$ = 0 |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 3.5 | — | 5.0 | V | $V_{DS}$ = 10 V, $I_D$ = 1 mA |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 22 | 28 | mΩ | $I_D$ = 4 A, $V_{GS}$ = 10 V Note4 |
| | $R_{DS(on)}$ | — | 23 | 33 | mΩ | $I_D$ = 4 A, $V_{GS}$ = 8 V Note4 |
| Forward transfer admittance | $\|y_{fs}\|$ | 8 | 14 | — | S | $I_D$ = 4 A, $V_{DS}$ = 10 V Note4 |
| Input capacitance | Ciss | — | 2300 | — | pF | $V_{DS}$ = 10 V |
| Output capacitance | Coss | — | 280 | — | pF | $V_{GS}$ = 0 |
| Reverse transfer capacitance | Crss | — | 90 | — | pF | f = 1 MHz |
| Gate Resistance | Rg | — | 1.3 | — | Ω | |
| Total gate charge | Qg | — | 32 | — | nC | $V_{DD}$ = 50 V |
| Gate to source charge | Qgs | — | 12 | — | nC | $V_{GS}$ = 10 V |
| Gate to drain charge | Qgd | — | 8 | — | nC | $I_D$ = 8 A |
| Turn-on delay time | $t_{d(on)}$ | — | 16 | — | ns | $V_{GS}$ = 10 V, $I_D$ = 4 A |
| Rise time | $t_r$ | — | 4 | — | ns | $V_{DD}$ ≅ 30 V |
| Turn-off delay time | $t_{d(off)}$ | — | 32 | — | ns | $R_L$ = 7.5 Ω |
| Fall time | $t_f$ | — | 4.5 | — | ns | Rg = 4.7 Ω |
| Body–drain diode forward voltage | $V_{DF}$ | — | 0.79 | 1.03 | V | IF = 8 A, $V_{GS}$ = 0 Note4 |
| Body–drain diode reverse recovery time | $t_{rr}$ | — | 45 | — | ns | IF = 8 A, $V_{GS}$ = 0<br>diF/ dt = 100 A/ µs |

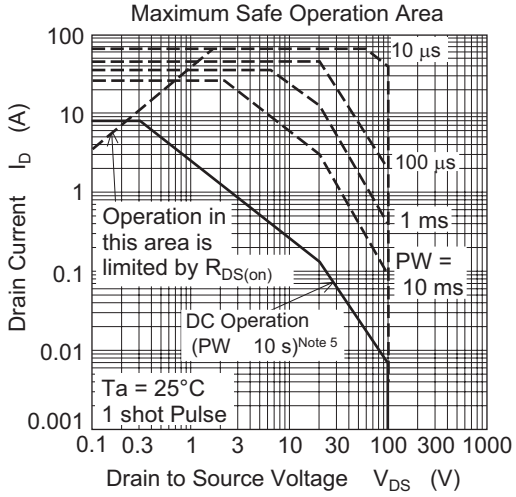
Notes: 4. Pulse test

## Main Characteristics

Power vs. Temperature Derating

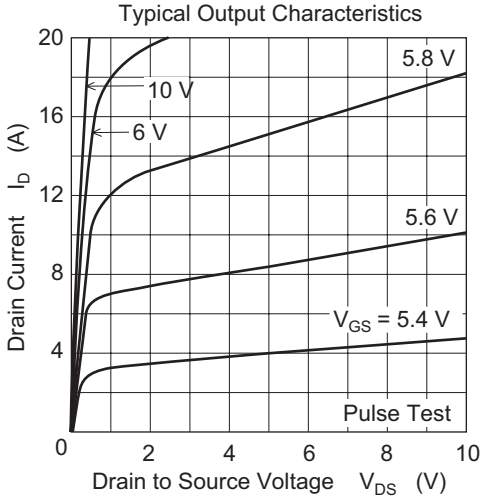



Maximum Safe Operation Area

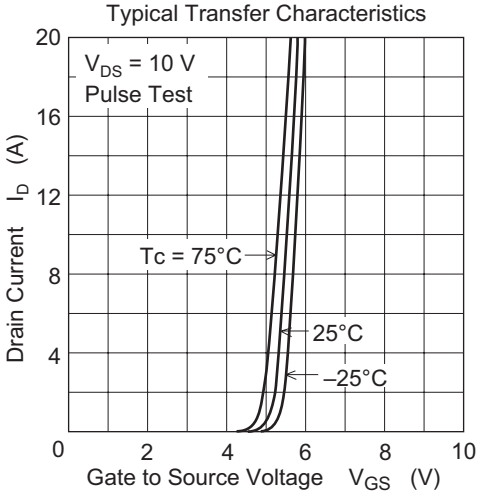



Note 5 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)

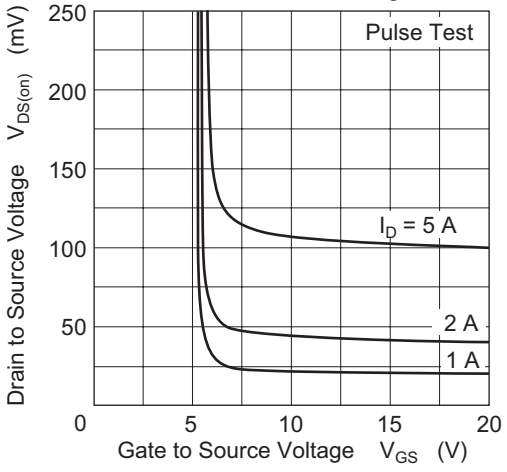
Typical Output Characteristics



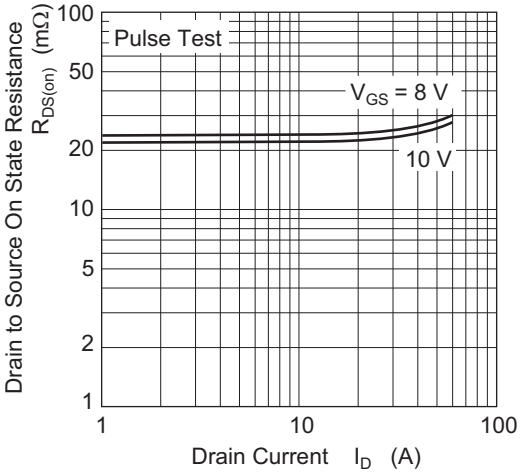

Typical Transfer Characteristics



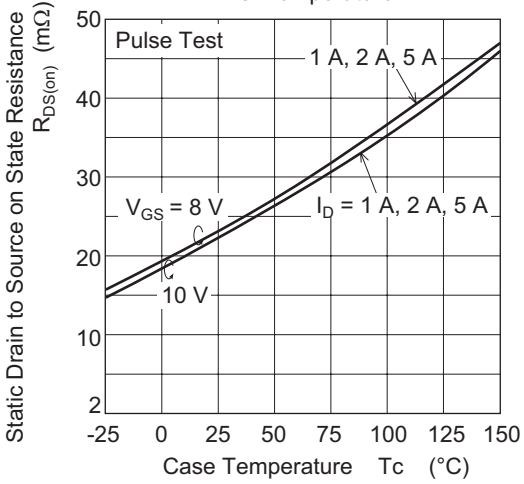

Drain to Source Saturation Voltage vs.
Gate to Source Voltage



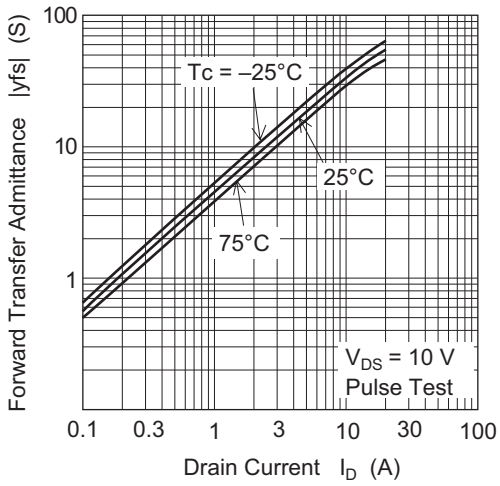

Static Drain to Source on State Resistance
vs. Drain Current



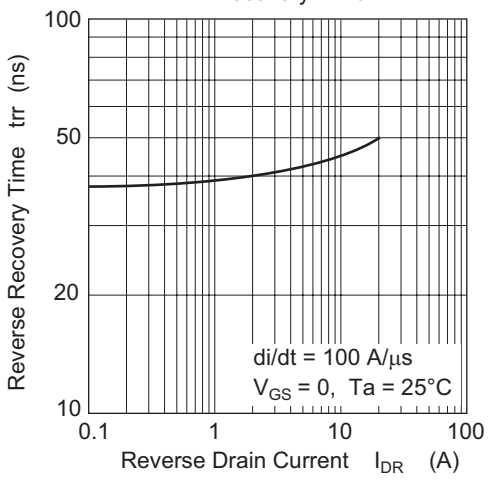
Static Drain to Source on State Resistance vs. Temperature



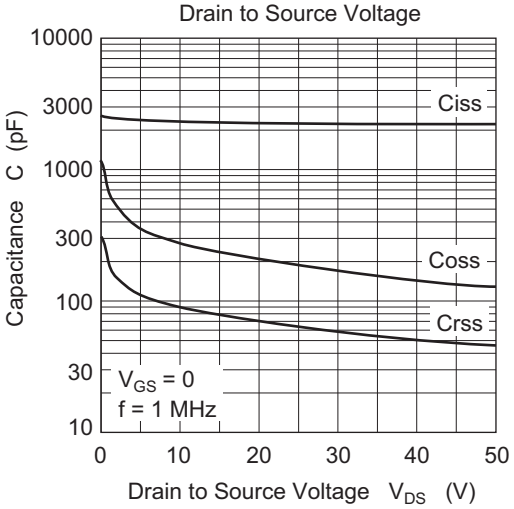

Forward Transfer Admittance vs. Drain Current



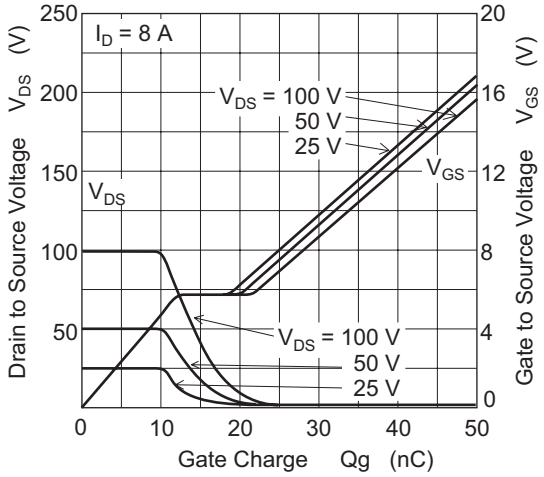

Body–Drain Diode Reverse Recovery Time



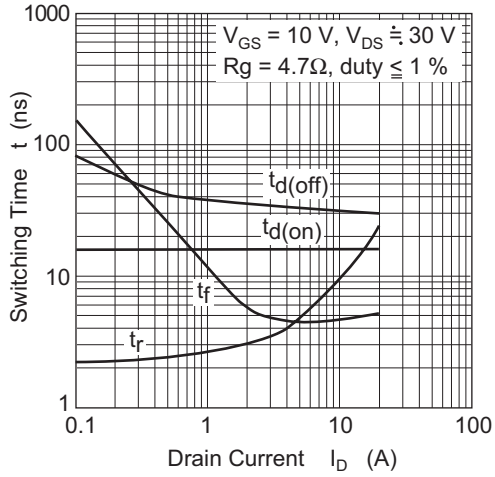

Typical Capacitance vs. Drain to Source Voltage



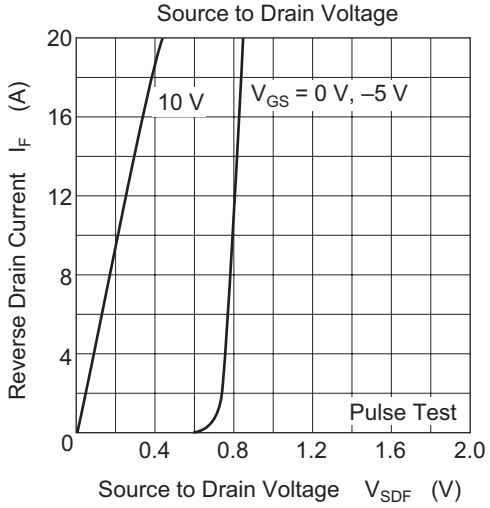

Dynamic Input Characteristics



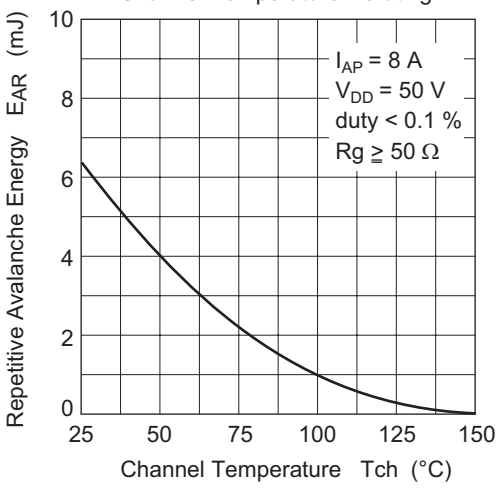

Switching Characteristics



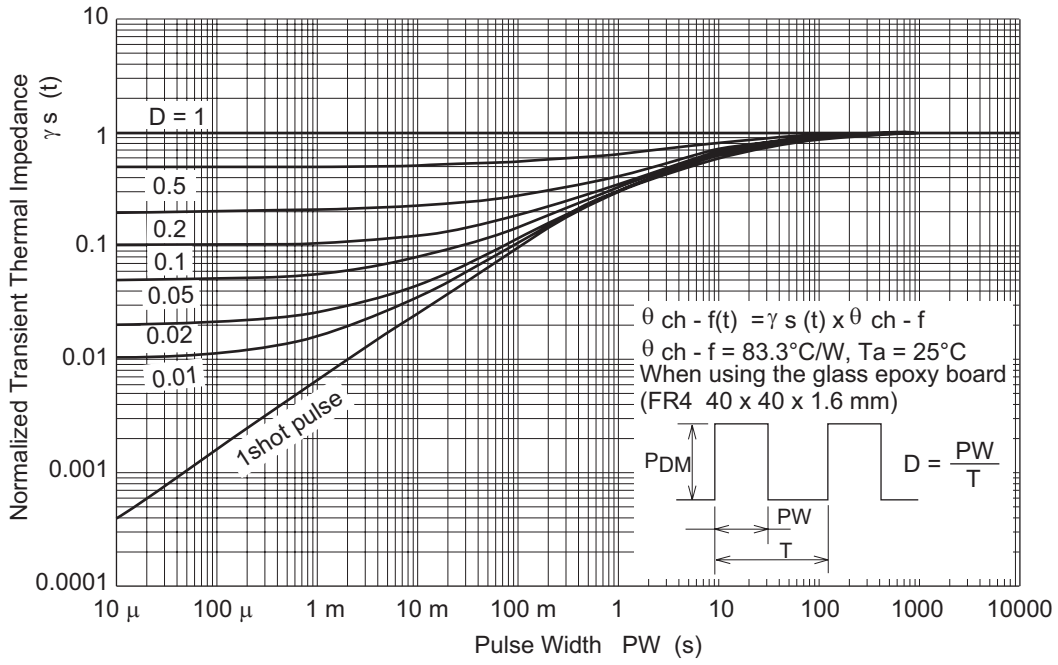
Reverse Drain Current vs. Source to Drain Voltage



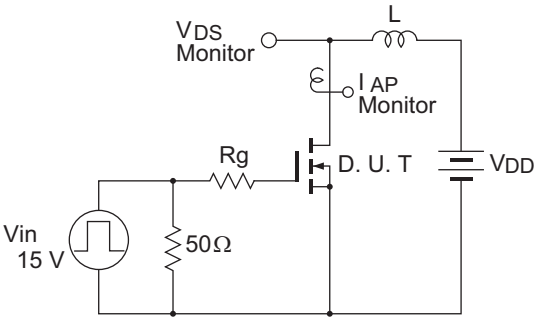

Maximum Avalanche Energy vs. Channel Temperature Derating




Normalized Transient Thermal Impedance vs. Pulse Width

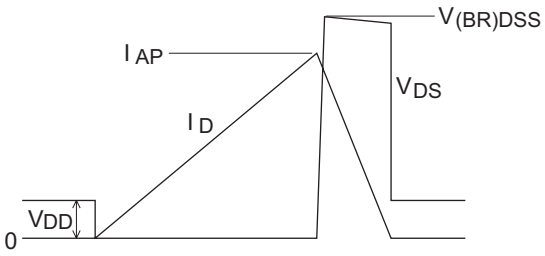


Avalanche Test Circuit

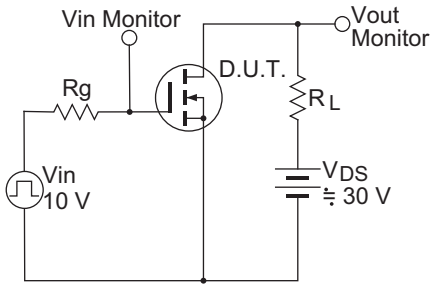



Avalanche Waveform

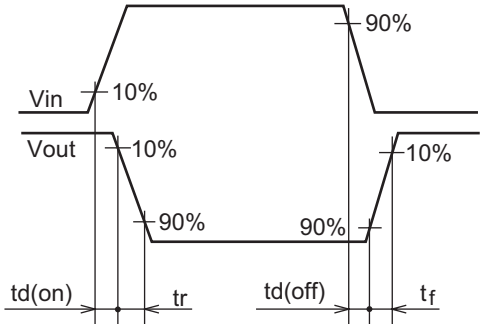
$$E_{AR} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$




Switching Time Test Circuit

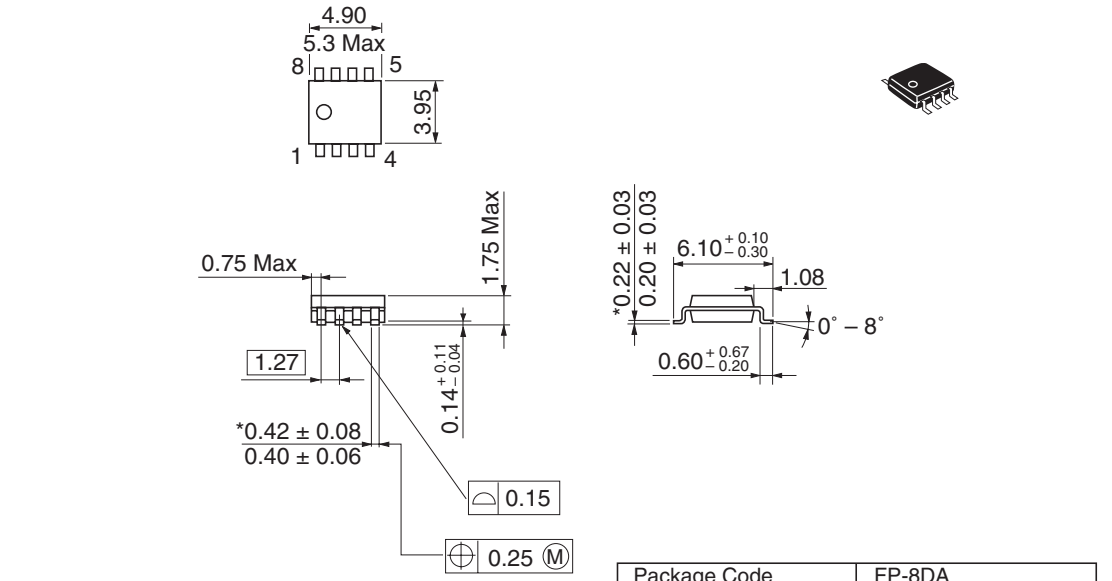



Switching Time Waveform



## Package Dimensions

As of January, 2003
Unit: mm




*Dimension including the plating thickness
Base material dimension

| | |
|---|---|
| Package Code | FP-8DA |
| JEDEC | Conforms |
| JEITA | — |
| Mass (reference value) | 0.085 g |

## Ordering Information

| Part Name | Quantity | Shipping Container |
|---|---|---|
| HAT2200R-EL-E | 2500pcs | Taping |

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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