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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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H5N5001FM

Silicon N Channel MOS FET
High Speed Power Switching

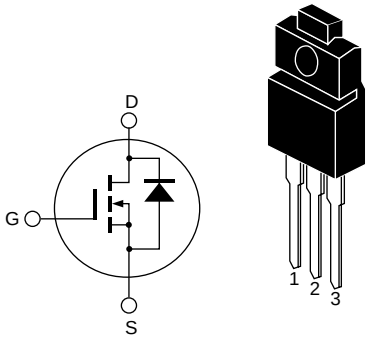
ADE-208-1380 (Z)
1st. Edition
Mar. 2001

Features

- Low on-resistance : $R_{DS(on)}$ =1.1Ω typ.
- Low leakage current : I_{DSS} =1μA max (at V_{DS} = 500 V)
- High speed switching : tf = 15ns typ (at V_{GS} = 10 V, V_{DD} = 250 V, I_D = 2.5 A)
- Low gate charge : Qg = 15nC typ (at V_{DD} = 400 V, V_{GS} = 10 V, I_D = 5 A)
- Avalanche ratings

Outline

TO–220FM



1. Gate
2. Drain
3. Source

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}$ Note1	20	A
Body-drain diode reverse drain current	I_{DR}	5	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ Note1	20	A
Avalanche current	I_{AP} Note3	5	A
Channel dissipation	Pch Note2	30	W
Channel to case Thermal Impedance	θch-c	4.17	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

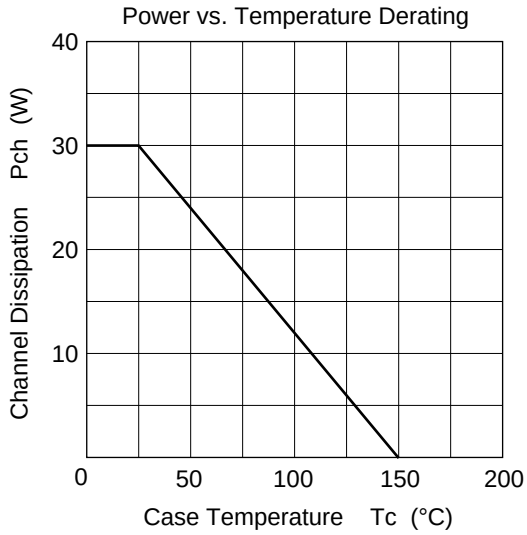
Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Tch ≤150°C

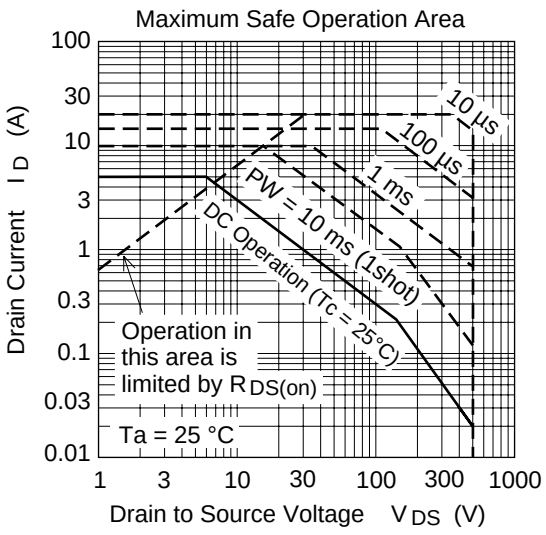
Electrical Characteristics (Ta = 25°C)

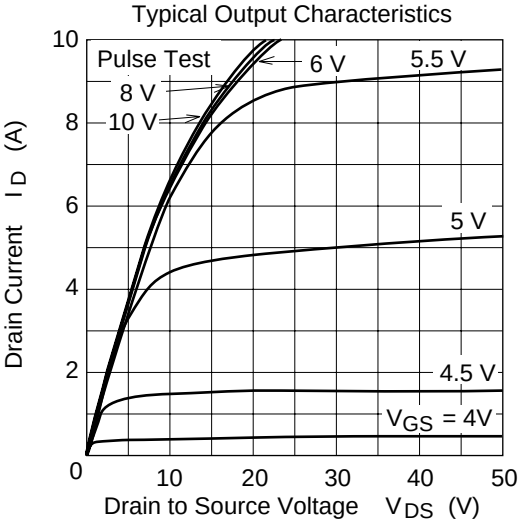
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±30V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	1	μA	V_{DS} = 500 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.0	V	I_D = 1mA, V_{DS} = 10V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.1	1.5	Ω	I_D = 2.5A, V_{GS} = 10V[Note4]
Forward transfer admittance	$\|y_{fs}\|$	3.0	4.5	—	S	I_D = 2.5A, V_{DS} = 10V [Note4]
Input capacitance	Ciss	—	580	—	pF	V_{DS} = 25V
Output capacitance	Coss	—	70	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	13	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 2.5A
Rise time	t_r	—	15	—	ns	V_{GS} = 10V
Turn-off delay time	$t_{d(off)}$	—	65	—	ns	R_L = 100Ω
Fall time	t_f	—	15	—	ns	R_g = 10Ω
Total gate charge	Qg	—	15	—	nC	V_{DD} = 400V
Gate to source charge	Qgs	—	3	—	nC	V_{GS} = 10V
Gate to drain charge	Qgd	—	8	—	nC	I_D = 5A
Body–drain diode forward voltage	V_{DF}	—	0.85	1.3	V	I_F = 5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	400	—	ns	I_F = 5A, V_{GS} = 0 diF/ dt =100A/μs
Body–drain diode reverse recovery charge	Q_{rr}	—	1.5	—	μC	

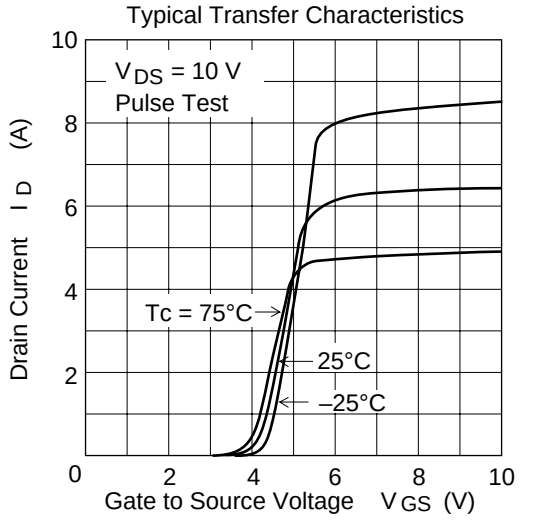
Note: 4. Pulse test

Main Characteristics

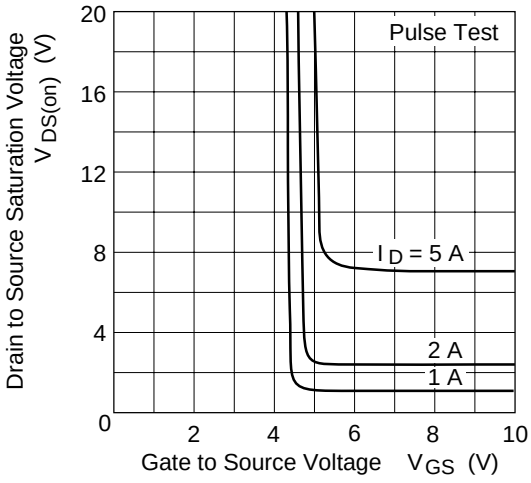




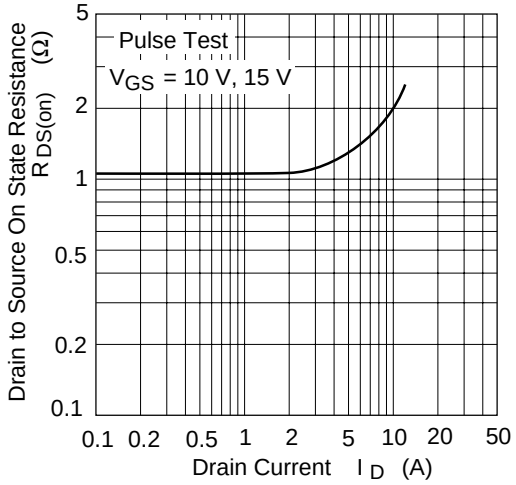




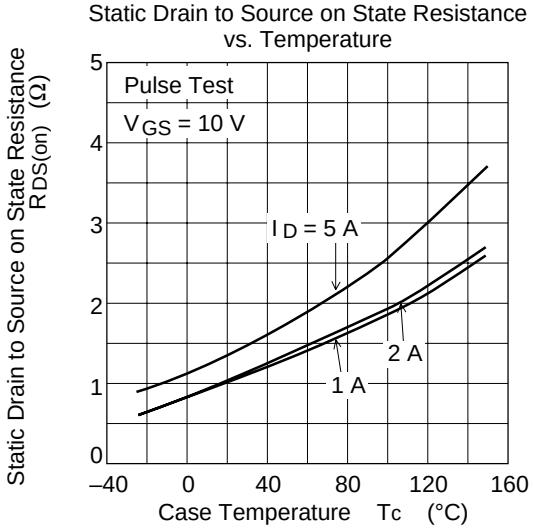
Drain to Source Saturation Voltage vs. Gate to Source Voltage



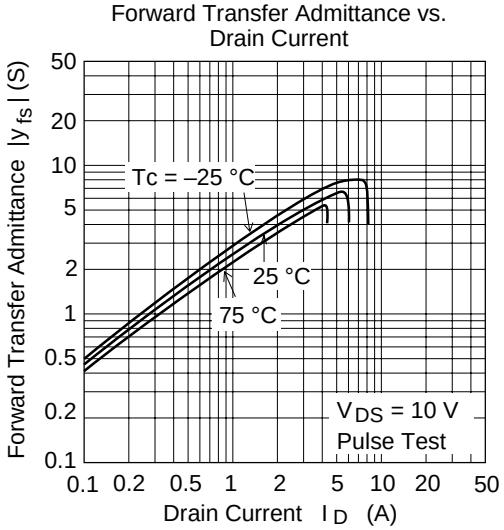
Static Drain to Source on State Resistance vs. Drain Current



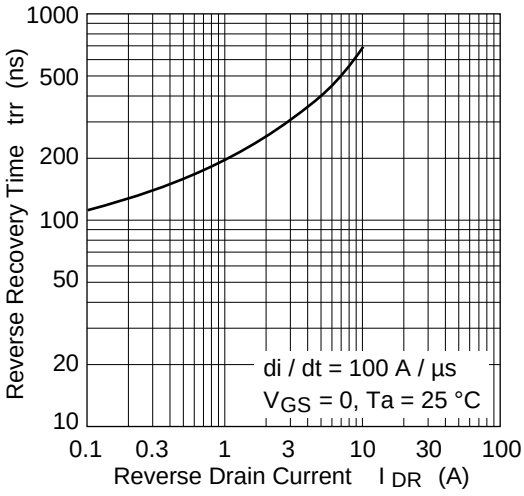
Static Drain to Source on State Resistance vs. Temperature



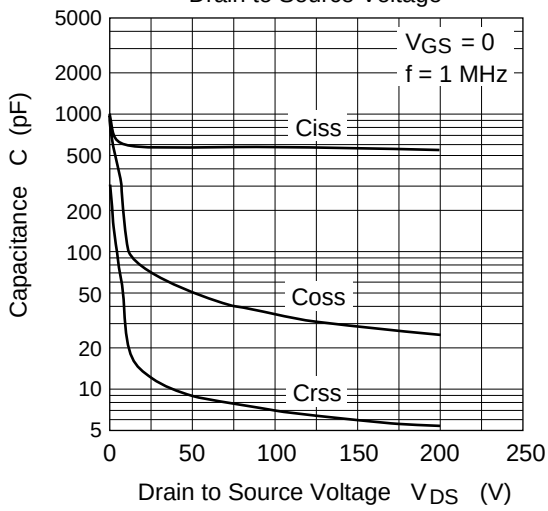
Forward Transfer Admittance vs. Drain Current



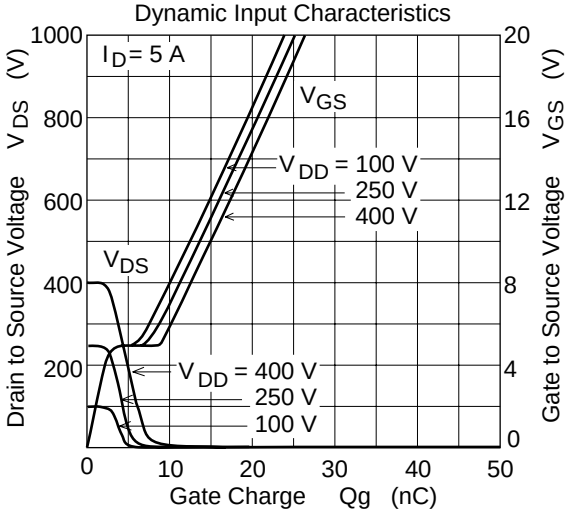
Body–Drain Diode Reverse Recovery Time



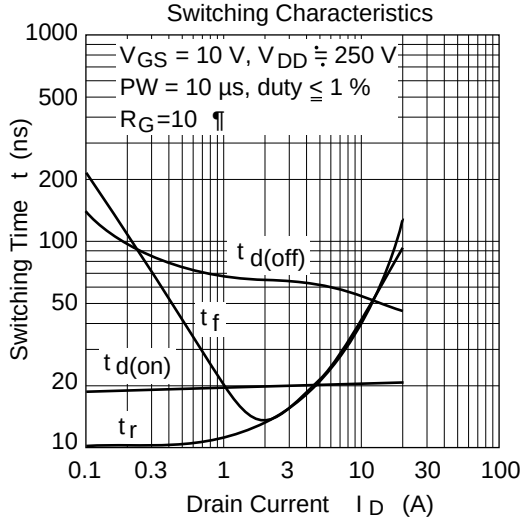
Typical Capacitance vs. Drain to Source Voltage



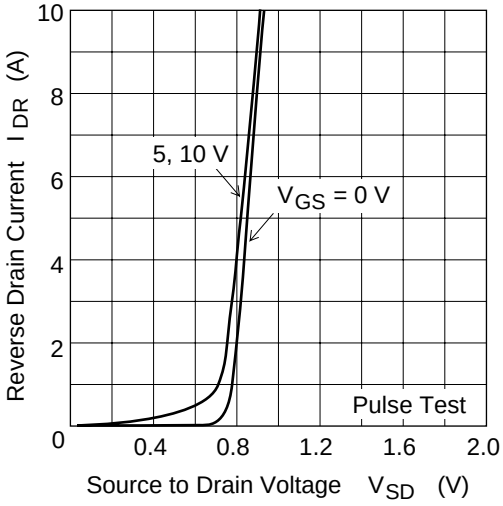
Dynamic Input Characteristics



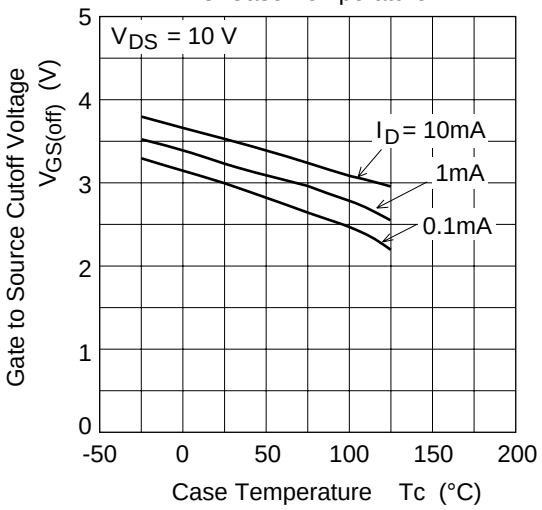
Switching Characteristics



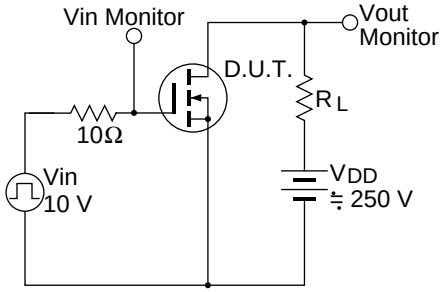
Reverse Drain Current vs.
Source to Drain Voltage



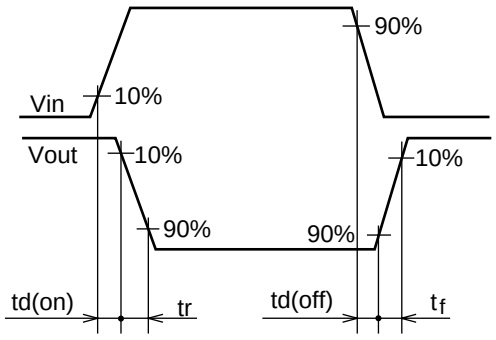
Gate to Source Cutoff Voltage
vs. Case Temperature

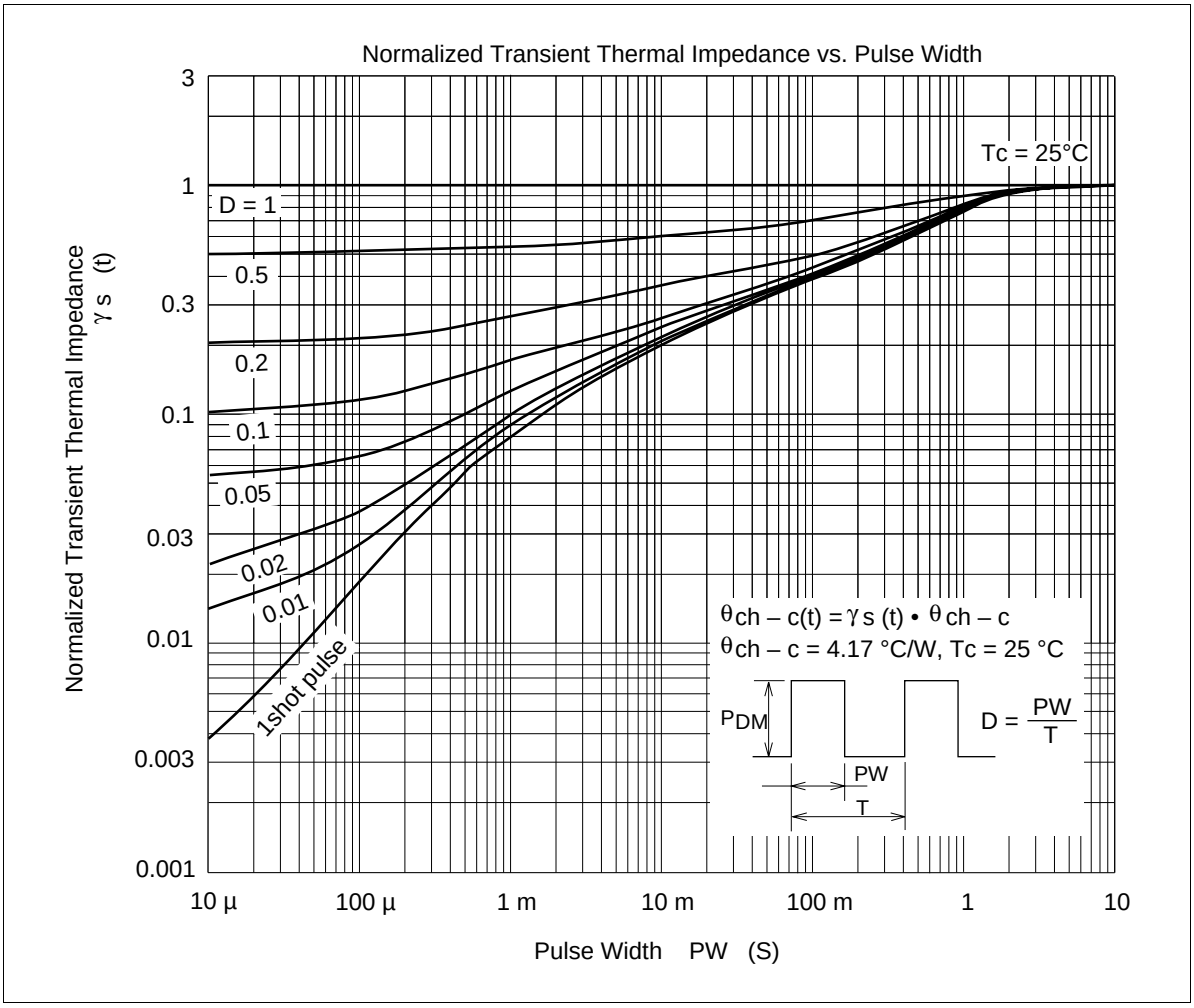


Switching Time Test Circuit



Waveform

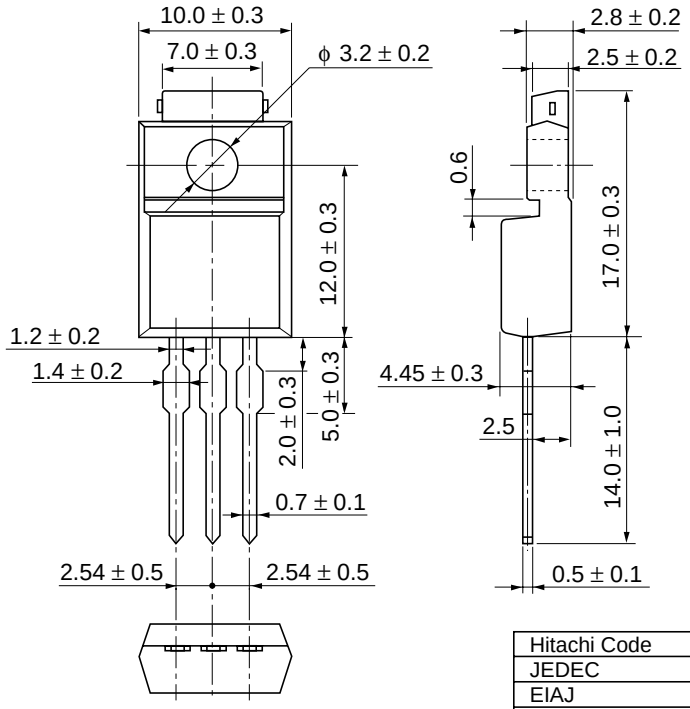


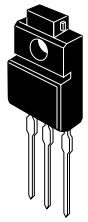

Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
0.003
0.001
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 4.17 °C/W, Tc = 25 °C
PDM
D = PW / T
PW
T
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

Package Dimensions

As of January, 2001

Unit: mm





Hitachi Code	TO-220FM
JEDEC	—
EIAJ	Conforms
Mass (reference value)	1.8 g

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