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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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H5N5006LD, H5N5006LS, H5N5006LM

Silicon N Channel MOS FET
High Speed Power Switching

ADE-208-1549 (Z)

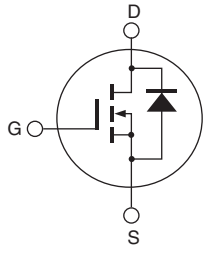
Rev.0
Aug.2002

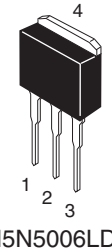
Features

- Low on-resistance
- Low leakage current
- High speed switching
- Low gate charge
- Avalanche ratings

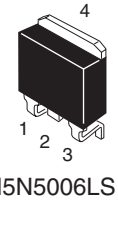
Outline

LDPAK

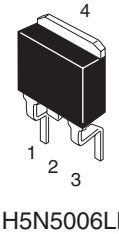




H5N5006LD



H5N5006LS



H5N5006LM

1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	3.5	A
Drain peak current	I_D (pulse) Note 1	14	A
Body-drain diode reverse drain current	I_{DR}	3.5	A
Avalanche current	I_{AP} Note 3	3.5	A
Channel dissipation	Pch Note 2	50	W
Channel to case thermal impedance	θch-c	2.5	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. Tch ≤ 150°C

Electrical Characteristics

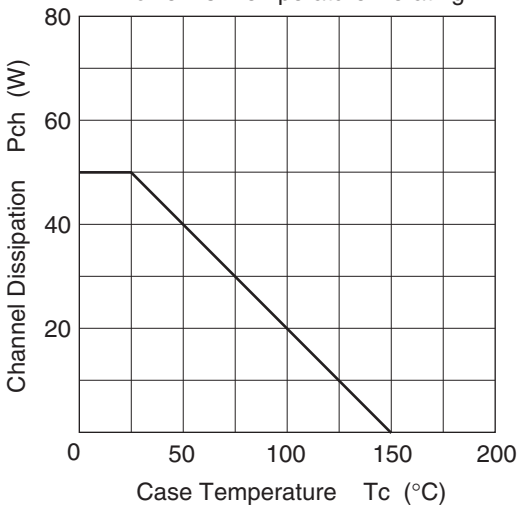
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{DSS}	—	—	1	µA	V_{DS} = 500 V, V_{GS} = 0
Zero gate voltage drain current	I_{GSS}	—	—	±0.1	µA	V_{GS} = ±30 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward transfer admittance	$\|y_{fs}\|$	1.8	3.0	—	S	I_D = 1.75 A, V_{DS} = 10 V [Note 4]
Static drain to source on state resistance	$R_{DS(on)}$	—	2.5	3.0	Ω	I_D = 1.75 A, V_{GS} = 10 V [Note 4]
Input capacitance	Ciss	—	365	—	pF	V_{DS} = 25 V
Output capacitance	Coss	—	35	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	8	—	pF	f = 1 MHz
Turn-on delay time	td(on)	—	20	—	ns	V_{DD} ≅ 250 V, I_D = 1.75 A
Rise time	tr	—	13	—	ns	V_{GS} = 10 V
Turn-off delay time	td(off)	—	48	—	ns	R_L = 143 Ω
Fall time	tf	—	14	—	ns	Rg = 10 Ω
Total gate charge	Qg	—	14	—	nC	V_{DD} = 400 V
Gate to source charge	Qgs	—	2	—	nC	V_{GS} = 10 V
Gate to drain charge	Qgd	—	8	—	nC	I_D = 3.5 A
Body-drain diode forward voltage	V_{DF}	—	0.85	1.3	V	I_F = 3.5 A, V_{GS} = 0
Body-drain diode reverse recovery time	trr	—	280	—	ns	I_F = 3.5 A, V_{GS} = 0 diF/dt = 100 A/µs
Body-drain diode reverse recovery charge	Qrr	—	0.8	—	µC	

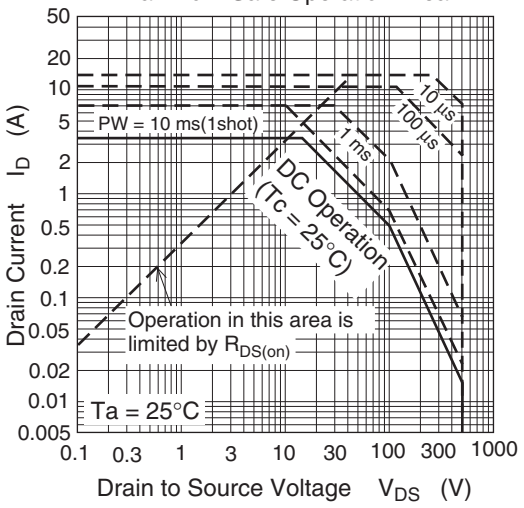
Notes: 4. Pulse test

Main Characteristics

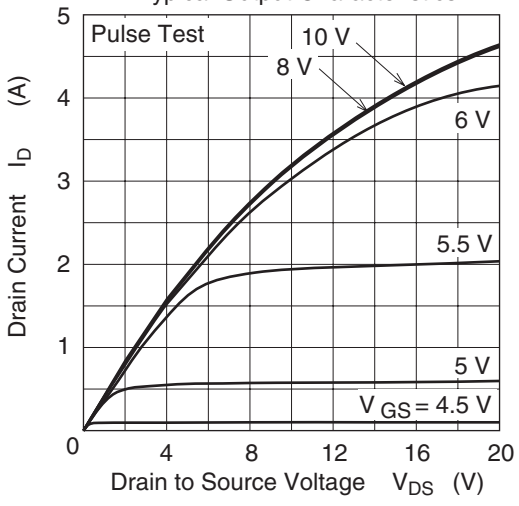
Power vs. Temperature Derating



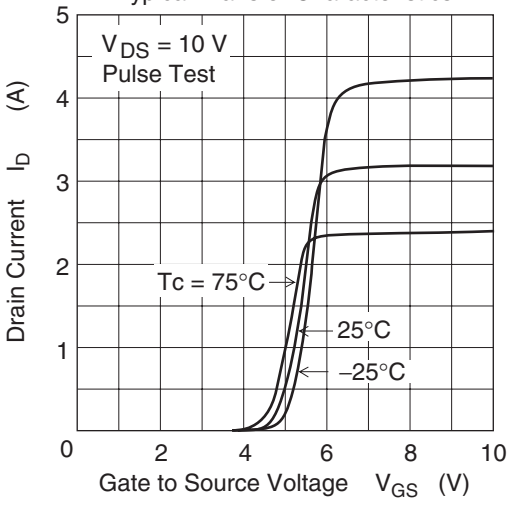
Maximum Safe Operation Area



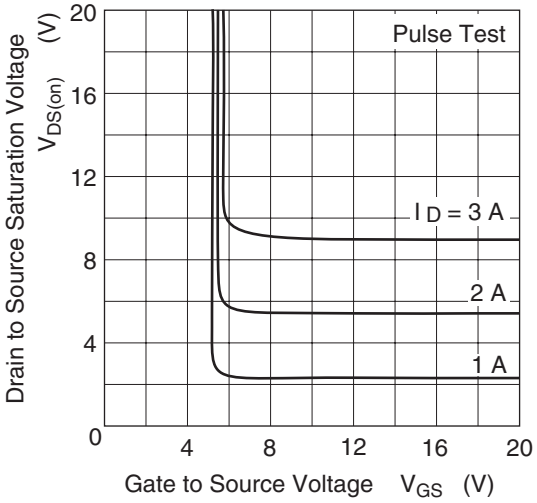
Typical Output Characteristics



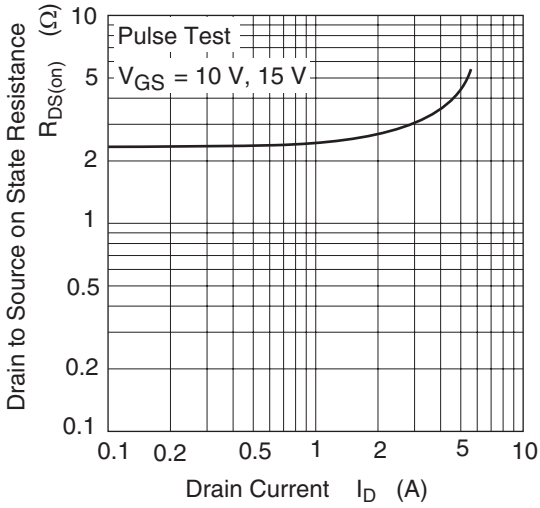
Typical Transfer Characteristics



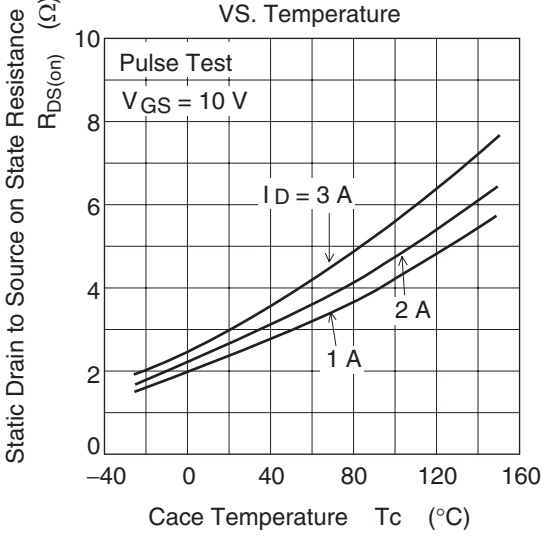
Drain to Source Saturation Voltage vs. Gate to Source Voltage



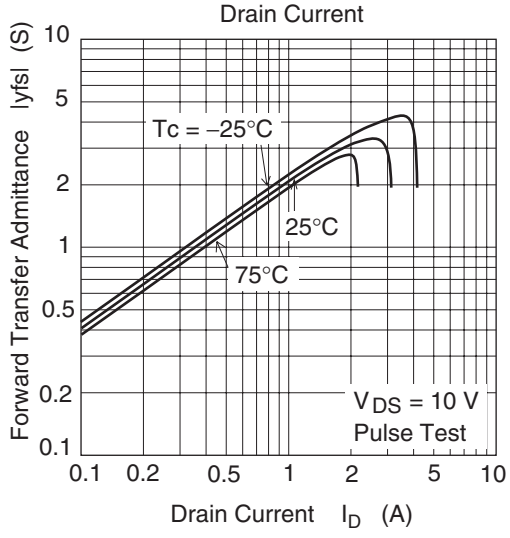
Static Drain to Source on State Resistance vs. Drain Current



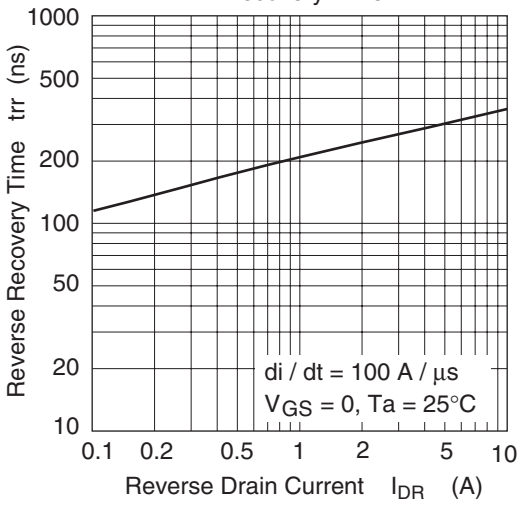
Static Drain to Source on State Resistance VS. Temperature



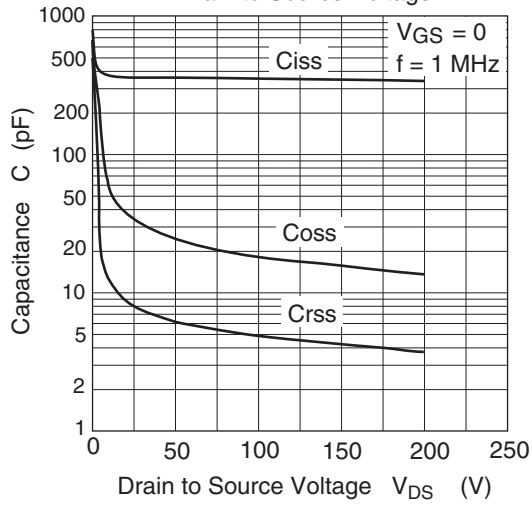
Forward Transfer Admittance vs. Drain Current



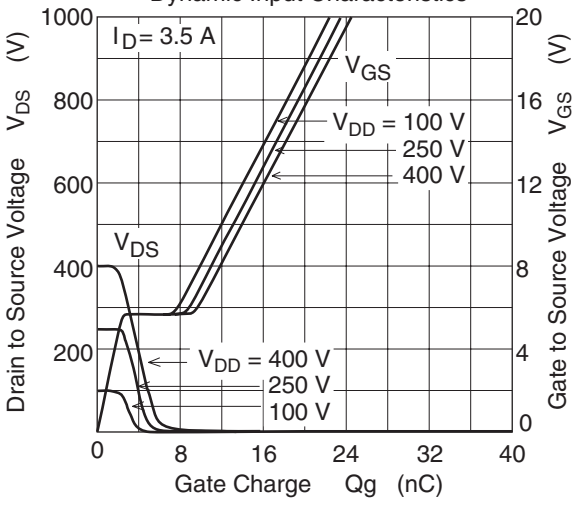
Body-Drain Diode Reverse Recovery Time



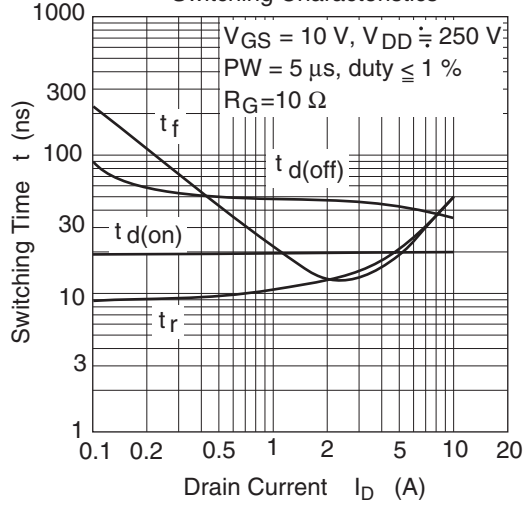
Typical Capacitance vs. Drain to Source Voltage



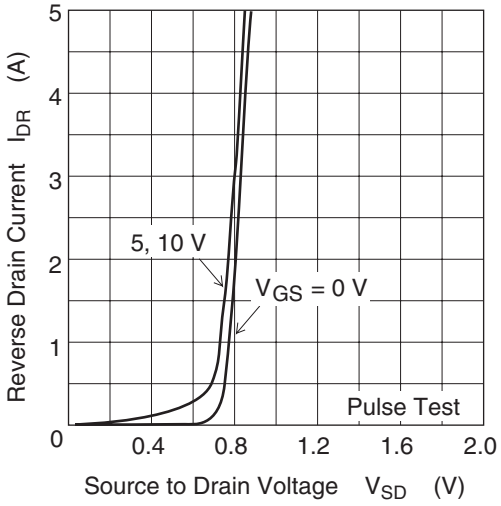
Dynamic Input Characteristics



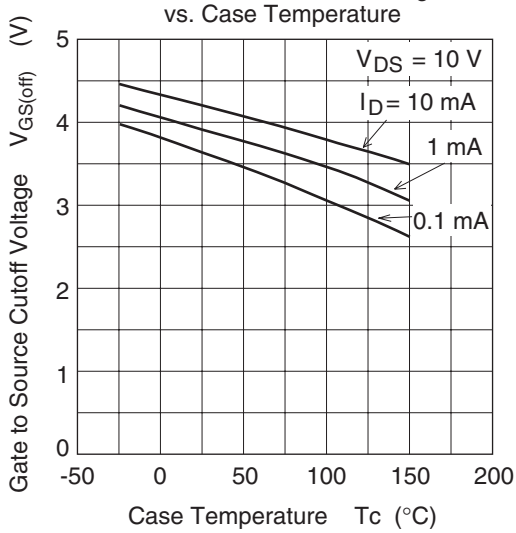
Switching Characteristics



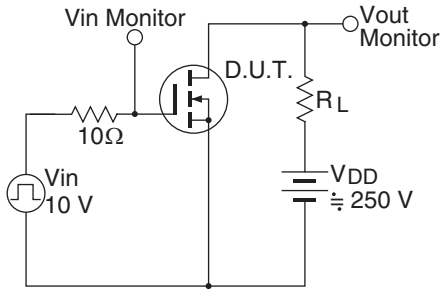
Reverse Drain Current vs. Source to Drain Voltage



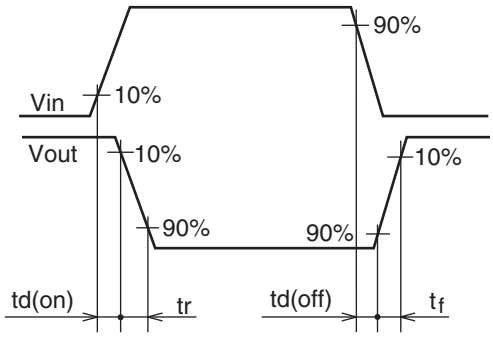
Gate to Source Cutoff Voltage vs. Case Temperature

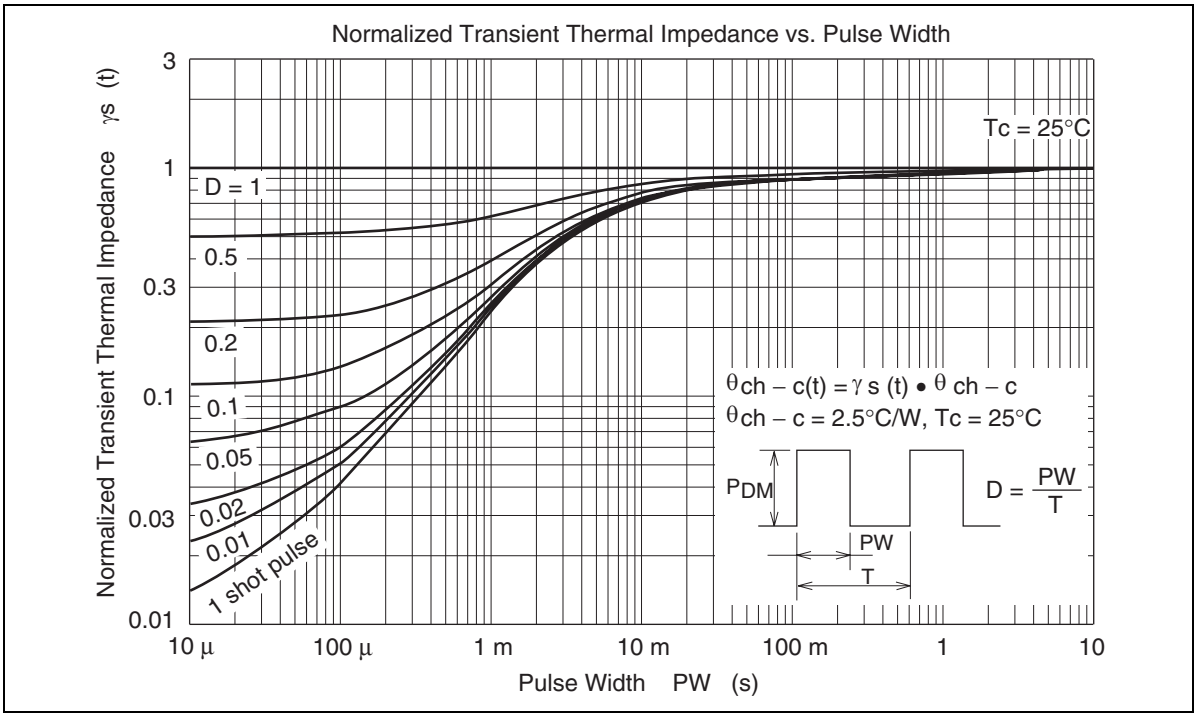


Switching Time Test Circuit



Waveform

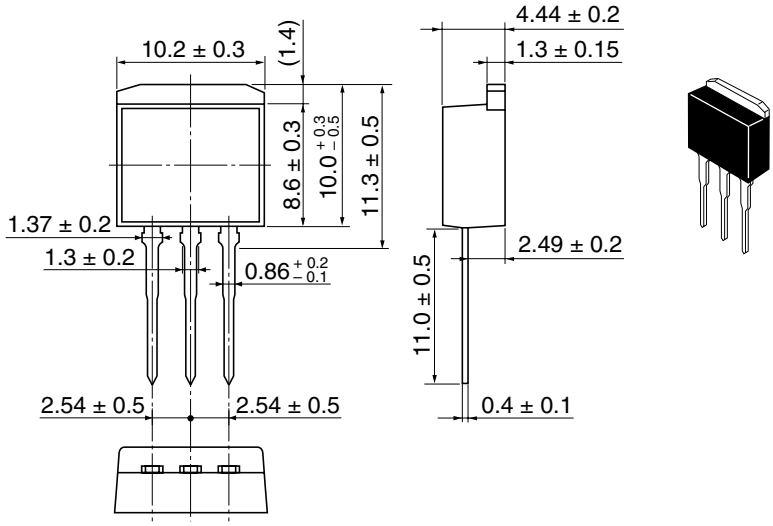



Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 2.5°C/W, Tc = 25°C
PDM
D = PW / T
PW
T
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

Package Dimensions

• H5N5006LD

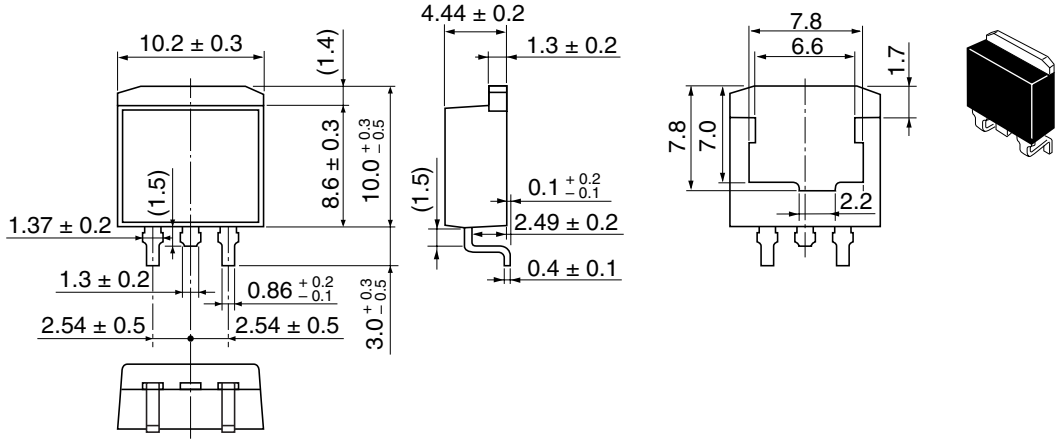
Unit: mm



Hitachi Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.4 g

• H5N5006LS

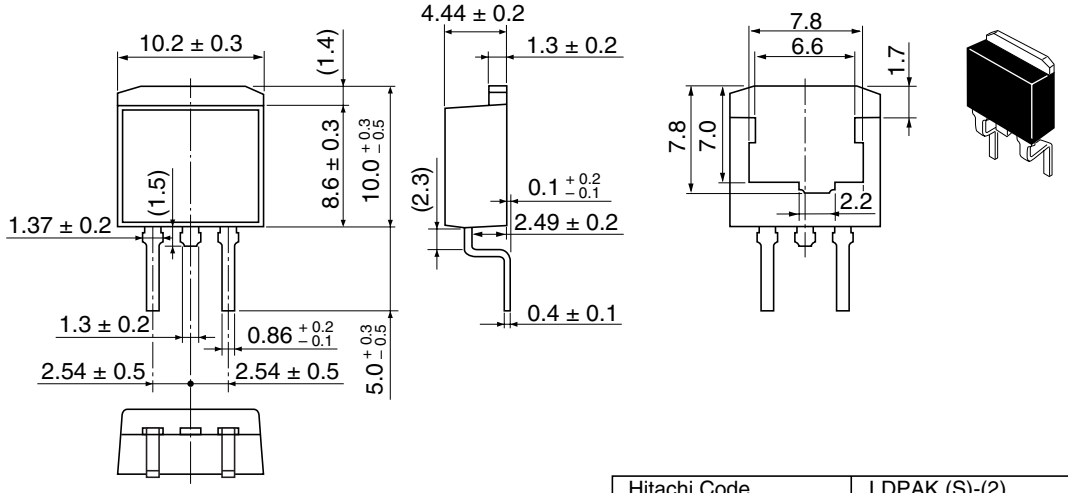
Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.3 g

• H5N5006LM

Unit: mm



Hitachi Code	LDPAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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