To all our customers

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The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Renesas Technology Corp.

Cautions

H7N1002LD, H7N1002LS, H7N1002LM

Silicon N Channel MOS FET
High Speed Power Switching

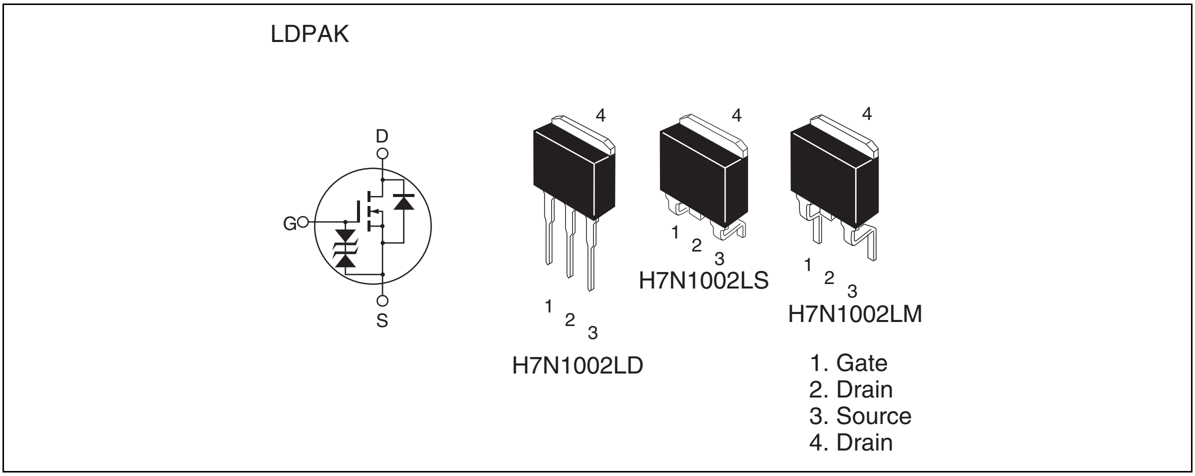
ADE-208-1573E (Z)

6th. Edition
Aug. 2002

Features

- Low on-resistance
- $R_{DS(on)}$ = 8 mΩ typ.
- Low drive current
- Available for 4.5 V gate drive

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	75	A
Drain peak current	$I_{D(pulse)}^{Note1}$	300	A
Body-drain diode reverse drain current	I_{DR}	75	A
Avalanche current	I_{AP}^{Note3}	50	A
Avalanche energy	E_{AR}^{Note3}	166	mJ
Channel dissipation	Pch^{Note2}	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown Voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	10	µA	V_{DS} = 100 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	I_D = 1 mA, V_{DS} = 10 V*[1]
Static drain to source on state resistance	$R_{DS(on)}$	—	8	10	mΩ	I_D = 37.5 A, V_{GS} = 10 V*[1]
		—	10	15	mΩ	I_D = 37.5 A, V_{GS} = 4.5 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	57	95	—	S	I_D = 37.5 A, V_{DS} = 10 V*[1]
Input capacitance	Ciss	—	9700	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	740	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	330	—	pF	f = 1 MHz
Total gate charge	Qg	—	155	—	nc	V_{DD} = 50 V
Gate to source charge	Qgs	—	35	—	nc	V_{GS} = 10 V
Gate to drain charge	Qgd	—	33	—	nc	I_D = 75 A
Turn-on delay time	$t_{d(on)}$	—	43	—	ns	V_{GS} = 10 V, I_D = 37.5 A
Rise time	t_r	—	245	—	ns	R_L = 0.8 Ω
Turn-off delay time	$t_{d(off)}$	—	130	—	ns	R_g = 4.7 Ω
Fall time	t_f	—	25	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.93	—	V	I_F = 75 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	70	—	ns	I_F = 75 A, V_{GS} = 0 diF/ dt = 100 A/µs

Notes: 1. Pulse test

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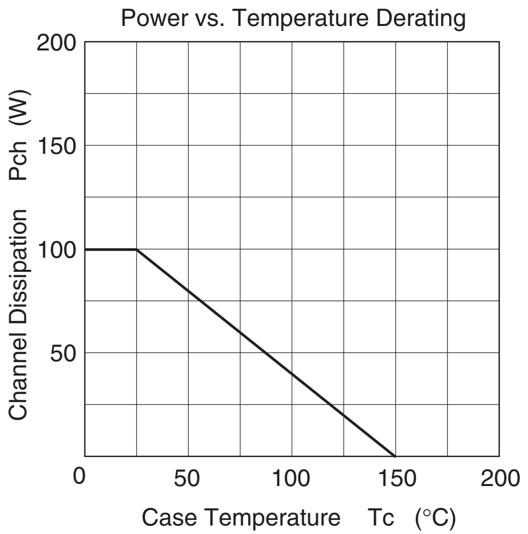
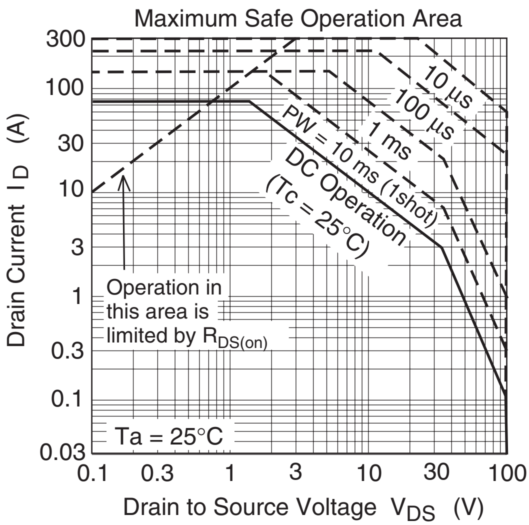
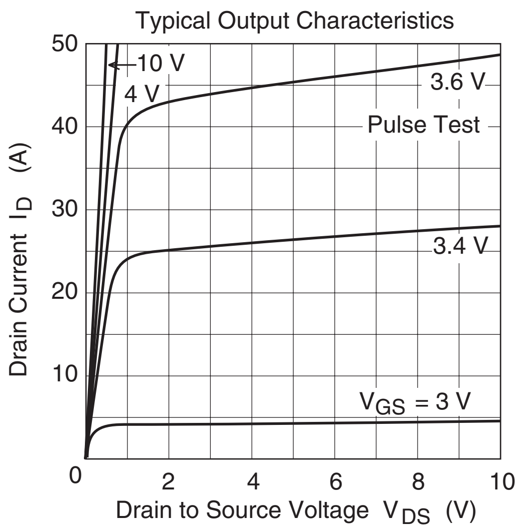
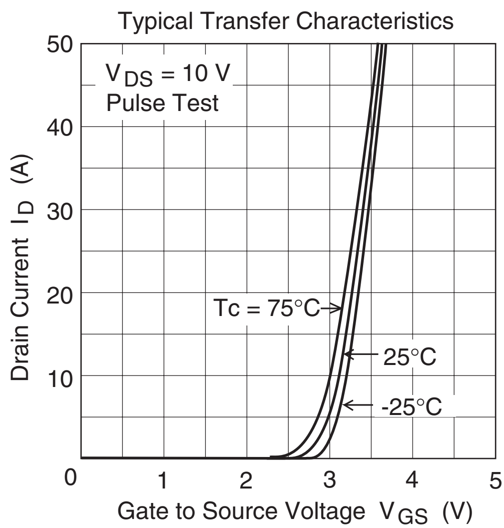
Main Characteristics









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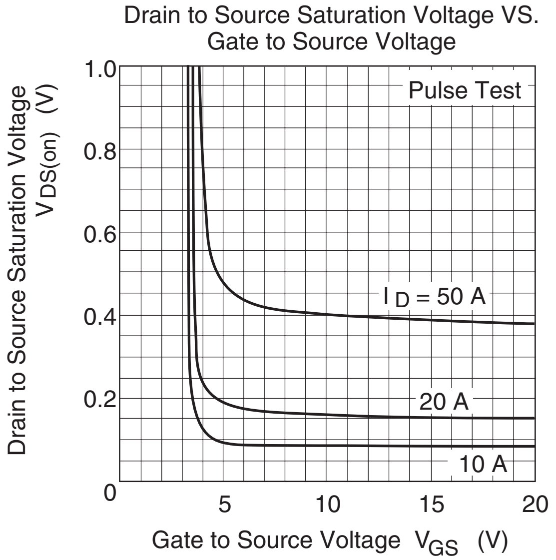
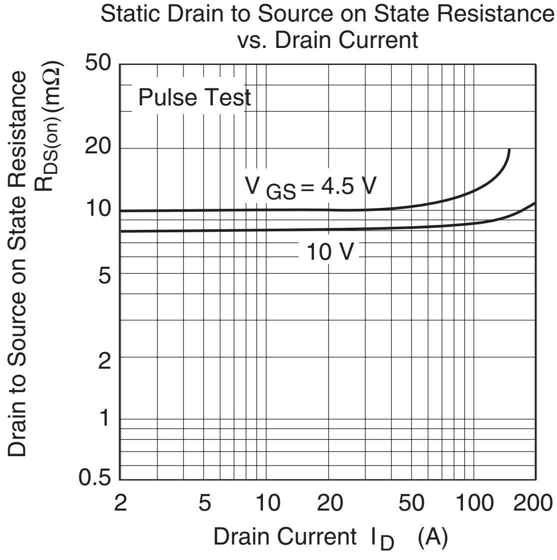
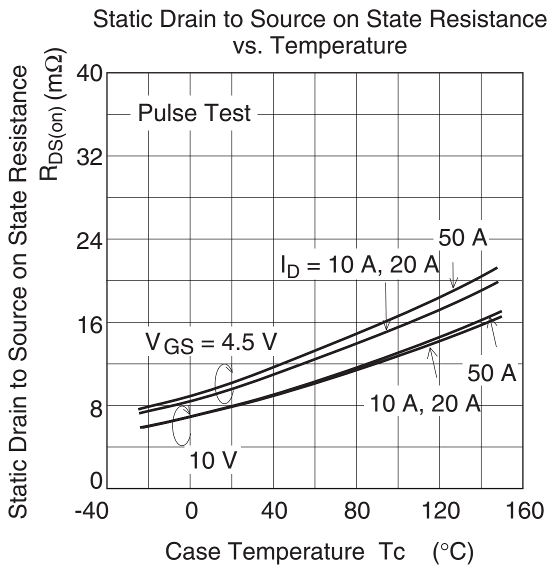
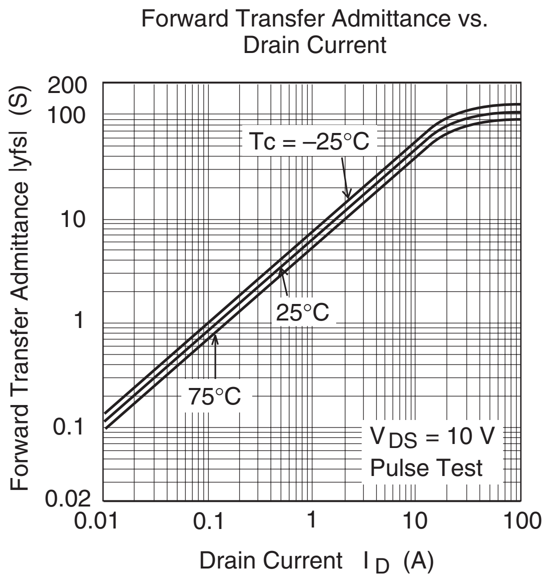
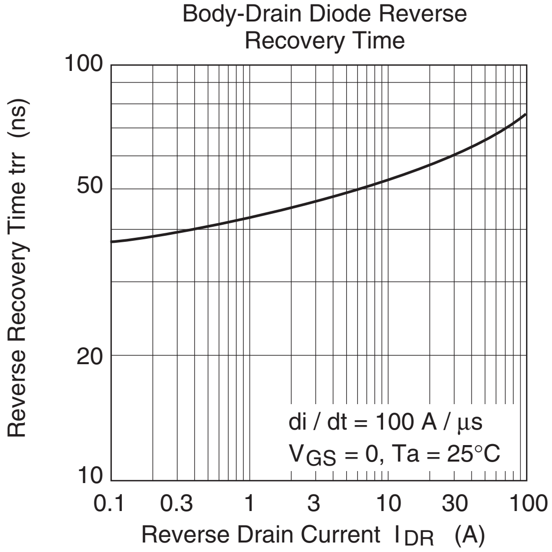

Drain to Source Saturation Voltage VS. Gate to Source Voltage
Pulse Test
I D = 50 A
20 A
10 A
Drain to Source Saturation Voltage VDS(on) (V)
1.0
0.8
0.6
0.4
0.2
0
5
10
15
20
Gate to Source Voltage VGS (V)

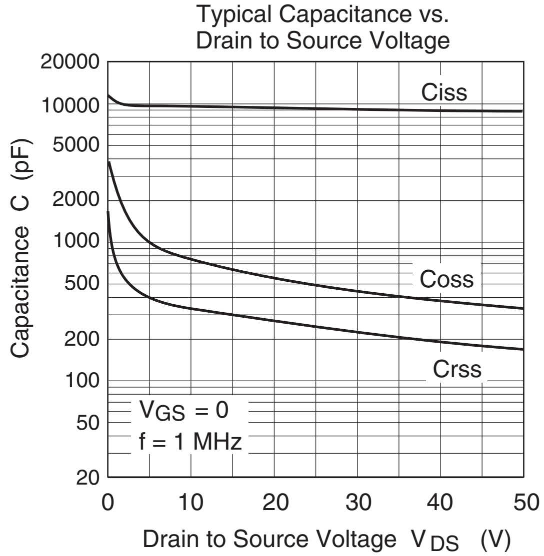

Static Drain to Source on State Resistance vs. Drain Current
Pulse Test
V GS = 4.5 V
10 V
Drain to Source on State Resistance RDS(on) (mΩ)
50
20
10
5
2
1
0.5
2
5
10
20
50
100
200
Drain Current I D (A)


Static Drain to Source on State Resistance vs. Temperature
Pulse Test
50 A
ID = 10 A, 20 A
VGS = 4.5 V
50 A
10 A, 20 A
10 V
Static Drain to Source on State Resistance RDS(on) (mΩ)
40
32
24
16
8
0
-40
0
40
80
120
160
Case Temperature Tc (°C)

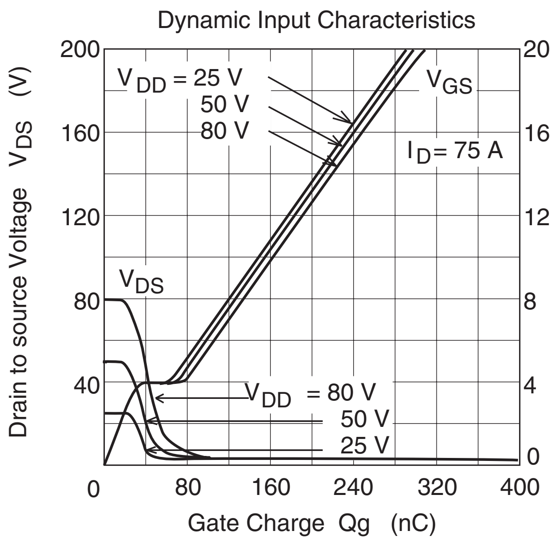

Forward Transfer Admittance vs. Drain Current
Tc = –25°C
25°C
75°C
VDS = 10 V
Pulse Test
Forward Transfer Admittance lyfsl (S)
200
100
10
1
0.1
0.02
0.01
0.1
1
10
100
Drain Current I D (A)



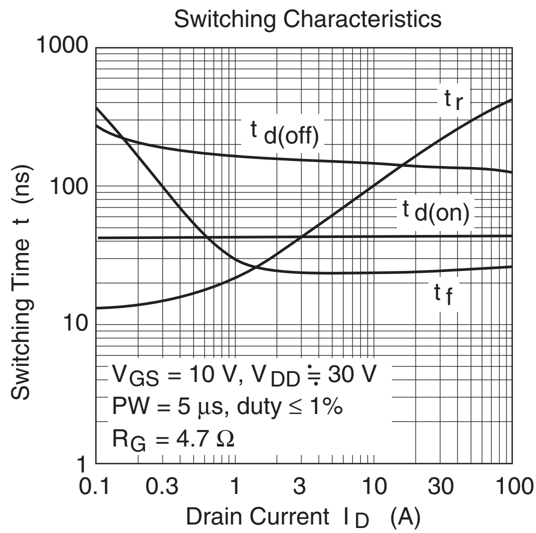
Body-Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
Reverse Drain Current I DR (A)
di / dt = 100 A / µs
V GS = 0, Ta = 25°C



Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
Drain to Source Voltage V DS (V)
Ciss
Coss
Crss
V GS = 0
f = 1 MHz

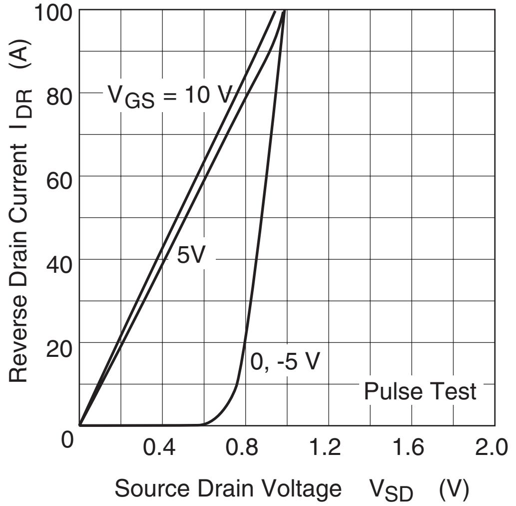


Dynamic Input Characteristics
Drain to source Voltage V DS (V)
Gate to Source Voltage V GS (V)
Gate Charge Qg (nC)
V DD = 25 V
50 V
80 V
V GS
I D = 75 A
V DS
V DD = 80 V
50 V
25 V

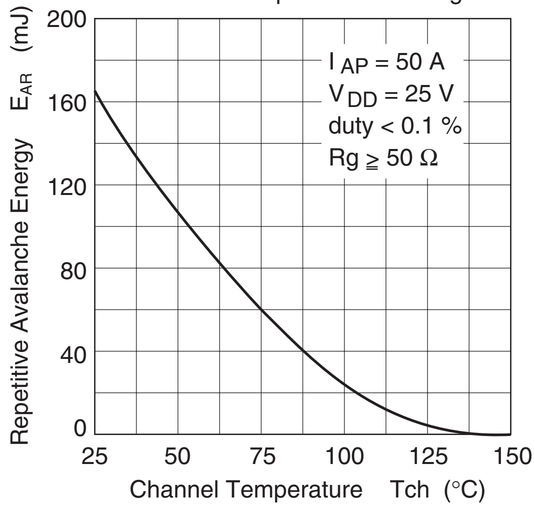


Switching Characteristics
Switching Time t (ns)
Drain Current I D (A)
t r
t d(off)
t d(on)
t f
V GS = 10 V, V DD ≒ 30 V
PW = 5 µs, duty ≤ 1%
R G = 4.7 Ω

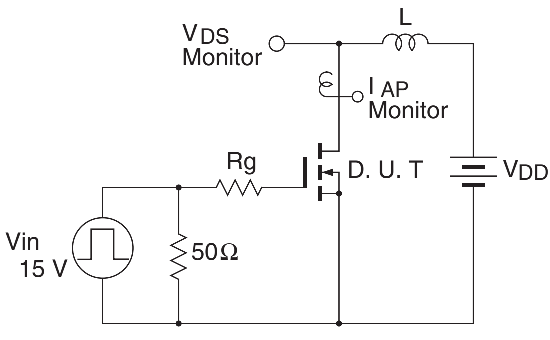
Reverses Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

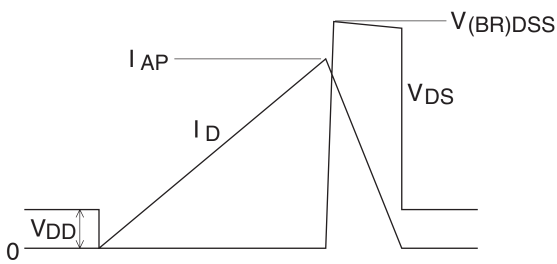


Avalanche Test Circuit



Avalanche Waveform

$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}{}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



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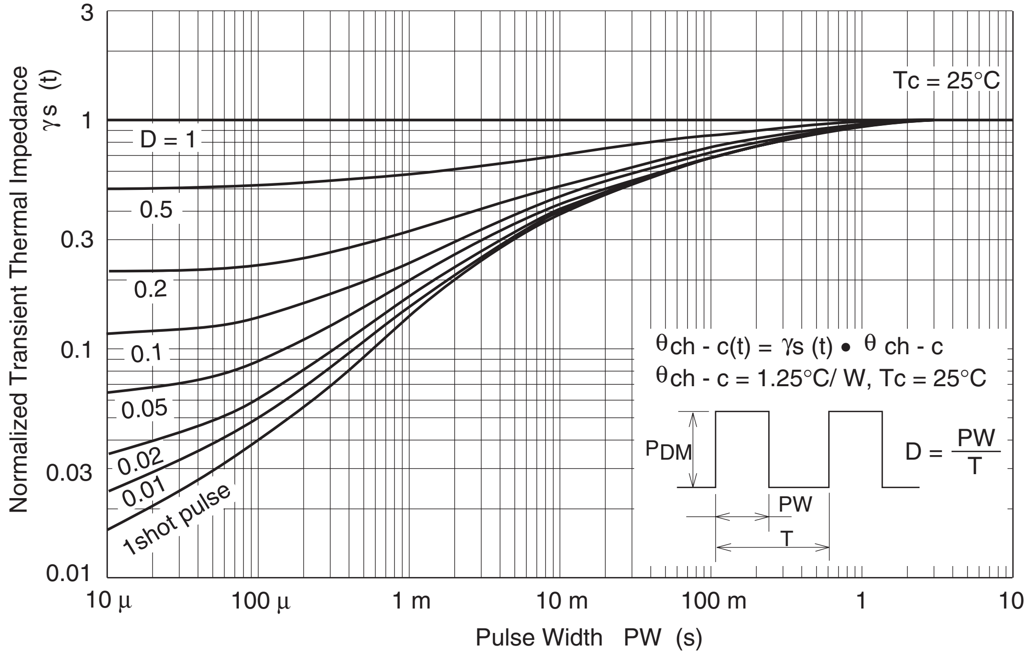
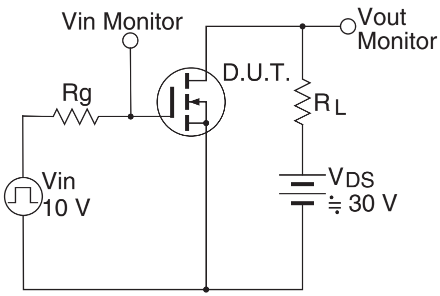
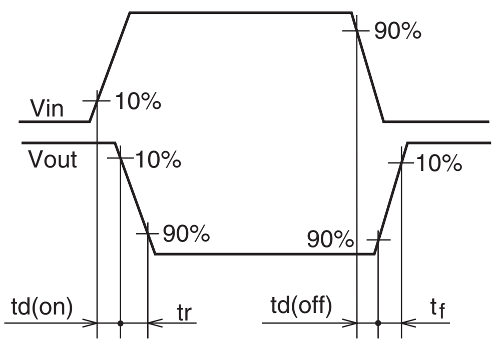
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



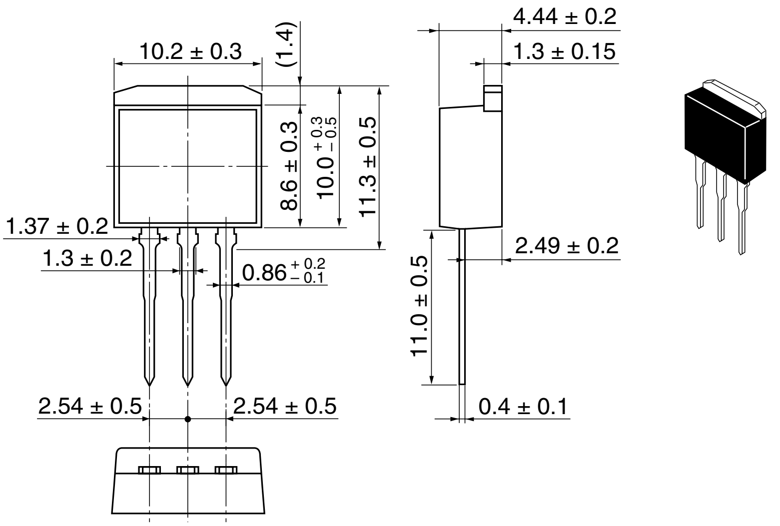
Switching Time Waveform



Package Dimensions

• H7N1002LD

Unit: mm



Hitachi Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.4 g

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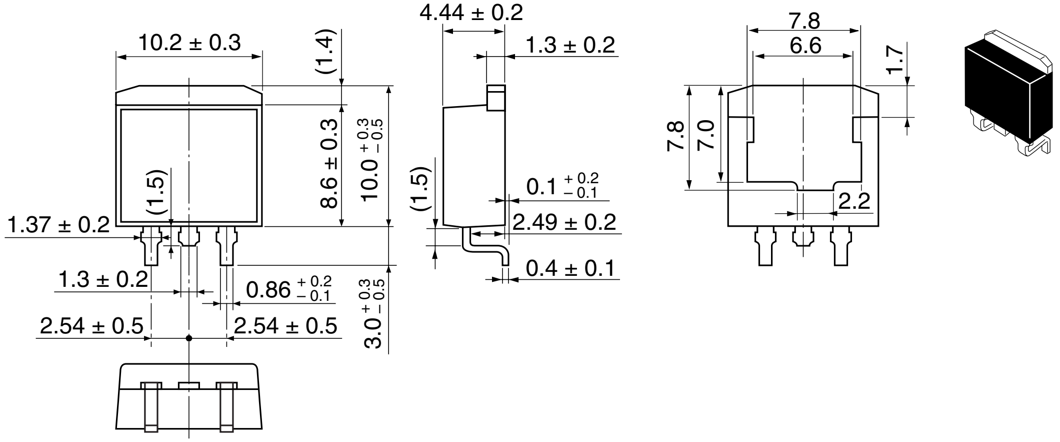
• H7N1002LS

Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.3 g

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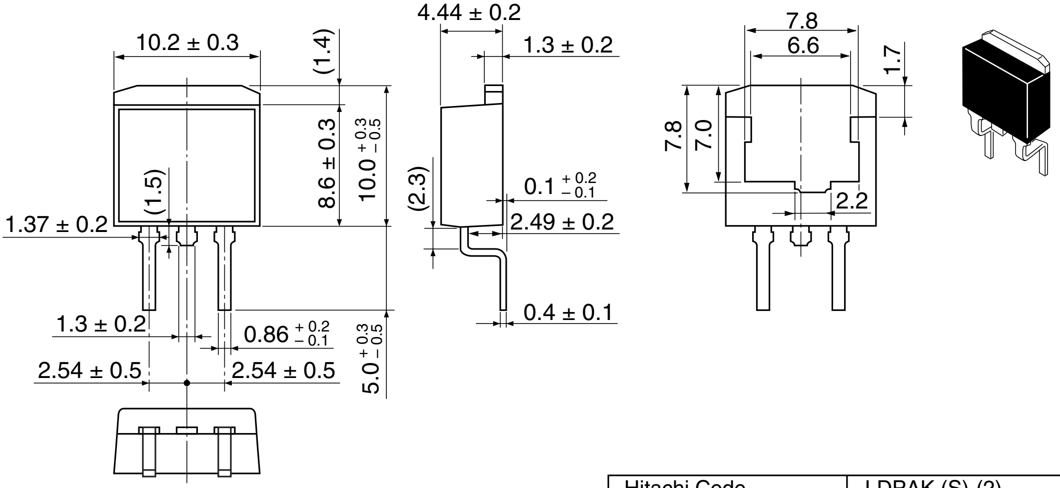
• H7N1002LM

Unit: mm



Hitachi Code	LDPAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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