

## H7N1004FM

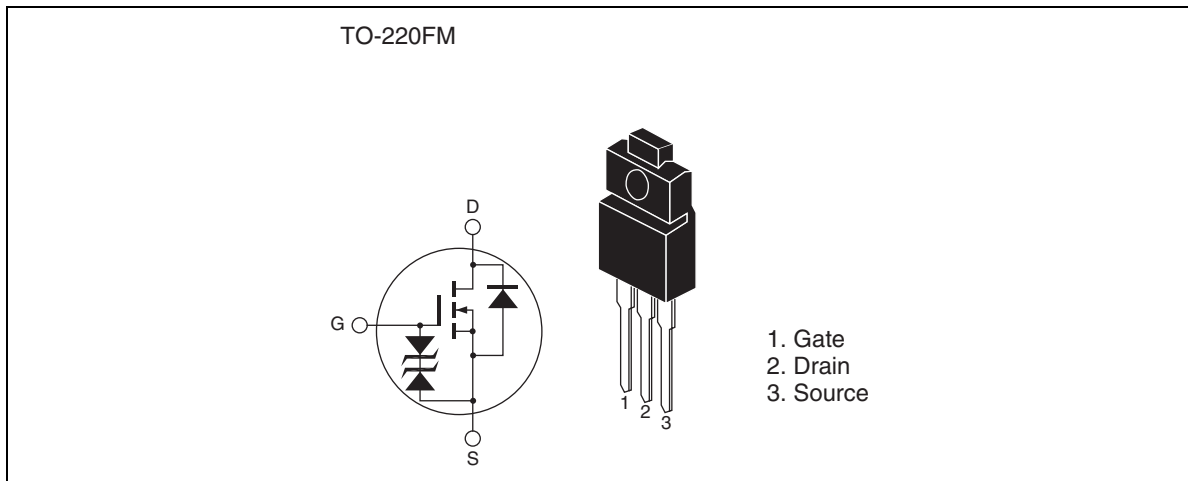
Silicon N-Channel MOSFET  
High-Speed Power Switching

REJ03G0073-0100Z  
(Previous ADE-208-1463A(Z))  
Rev.1.00  
Aug.27.2003

### Features

- Low on-resistance
- $R_{DS(on)} = 25 \text{ m}\Omega$  typ.
- Low drive current
- Available for 4.5 V gate drive

### Outline



**Absolute Maximum Ratings**

(Ta = 25°C)

<b>Item</b>	<b>Symbol</b>	<b>Value</b>	<b>Unit</b>
Drain to source voltage	V <sub>DSS</sub>	100	V
Gate to source voltage	V <sub>GSS</sub>	±20	V
Drain current	I <sub>D</sub>	25	A
Drain peak current	I <sub>D</sub> (pulse) <sup>Note1</sup>	100	A
Body-drain diode reverse drain current	I <sub>DR</sub>	100	A
Avalanche current	I <sub>AP</sub> <sup>Note 3</sup>	15	A
Avalanche energy	E <sub>AR</sub> <sup>Note 3</sup>	22.5	mJ
Channel dissipation	P <sub>ch</sub> <sup>Note 2</sup>	25	W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
2. Value at Tc = 25°C  
3. Value at Tch = 25°C, Rg ≥ 50 Ω

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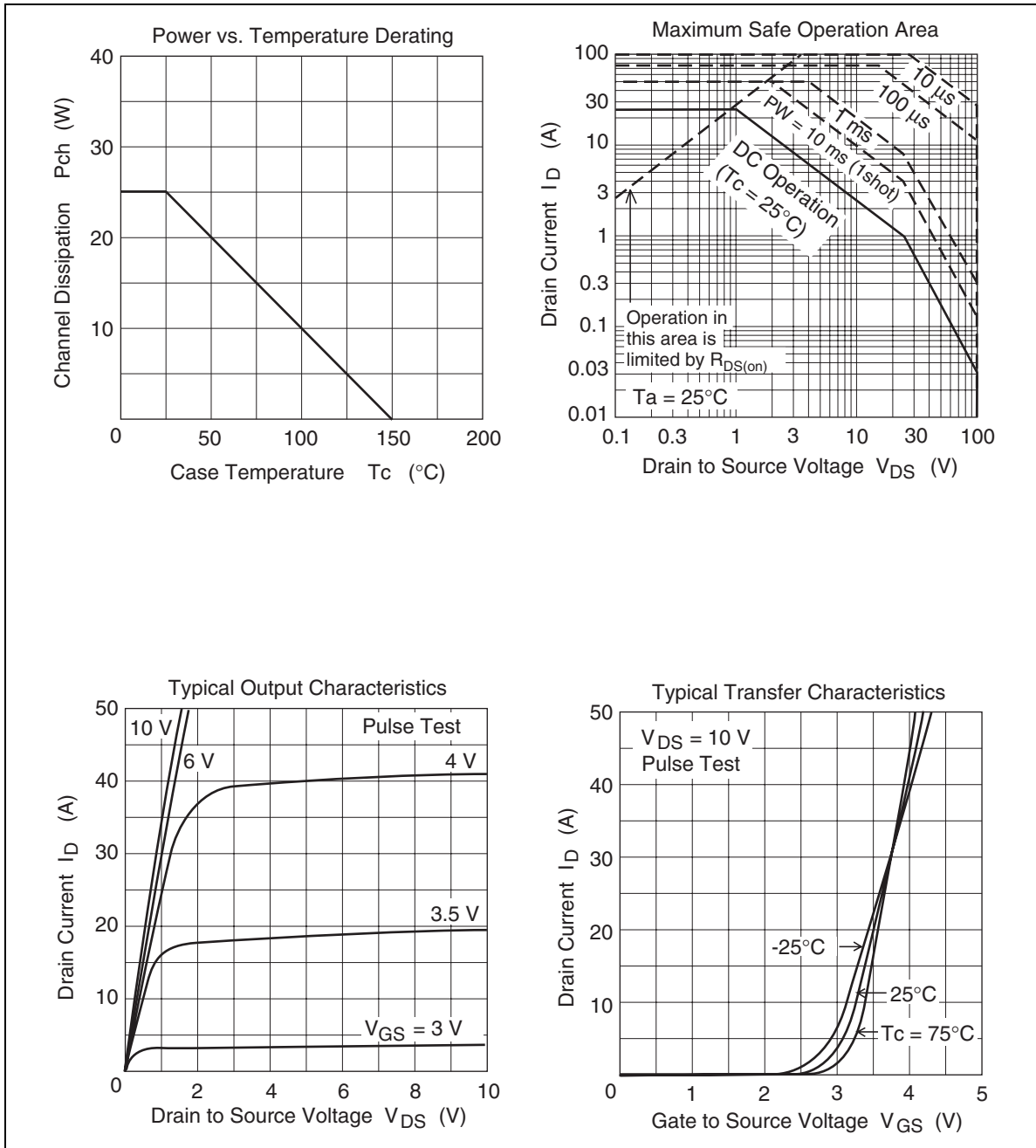
### Electrical Characteristics

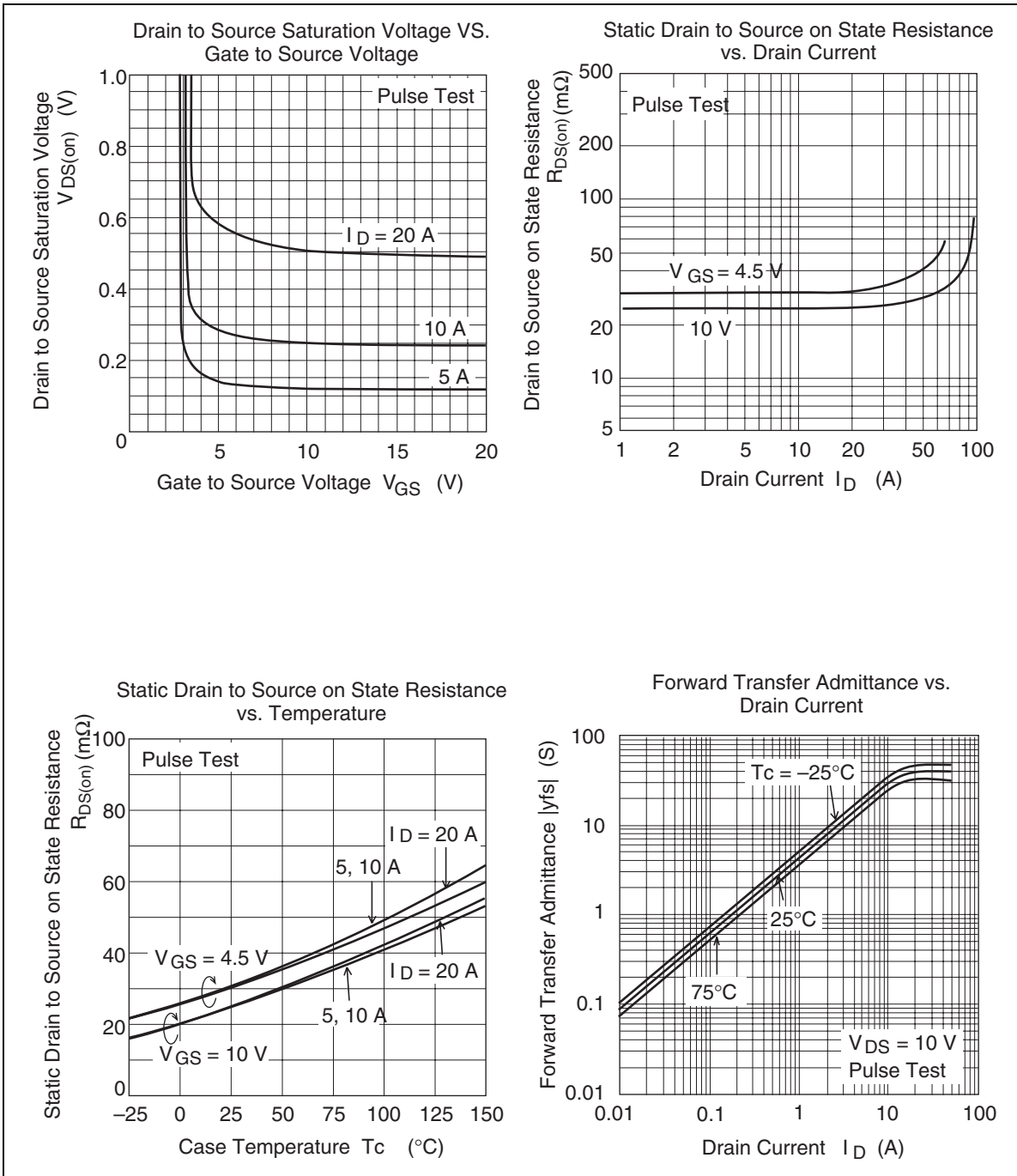
(Ta = 25°C)

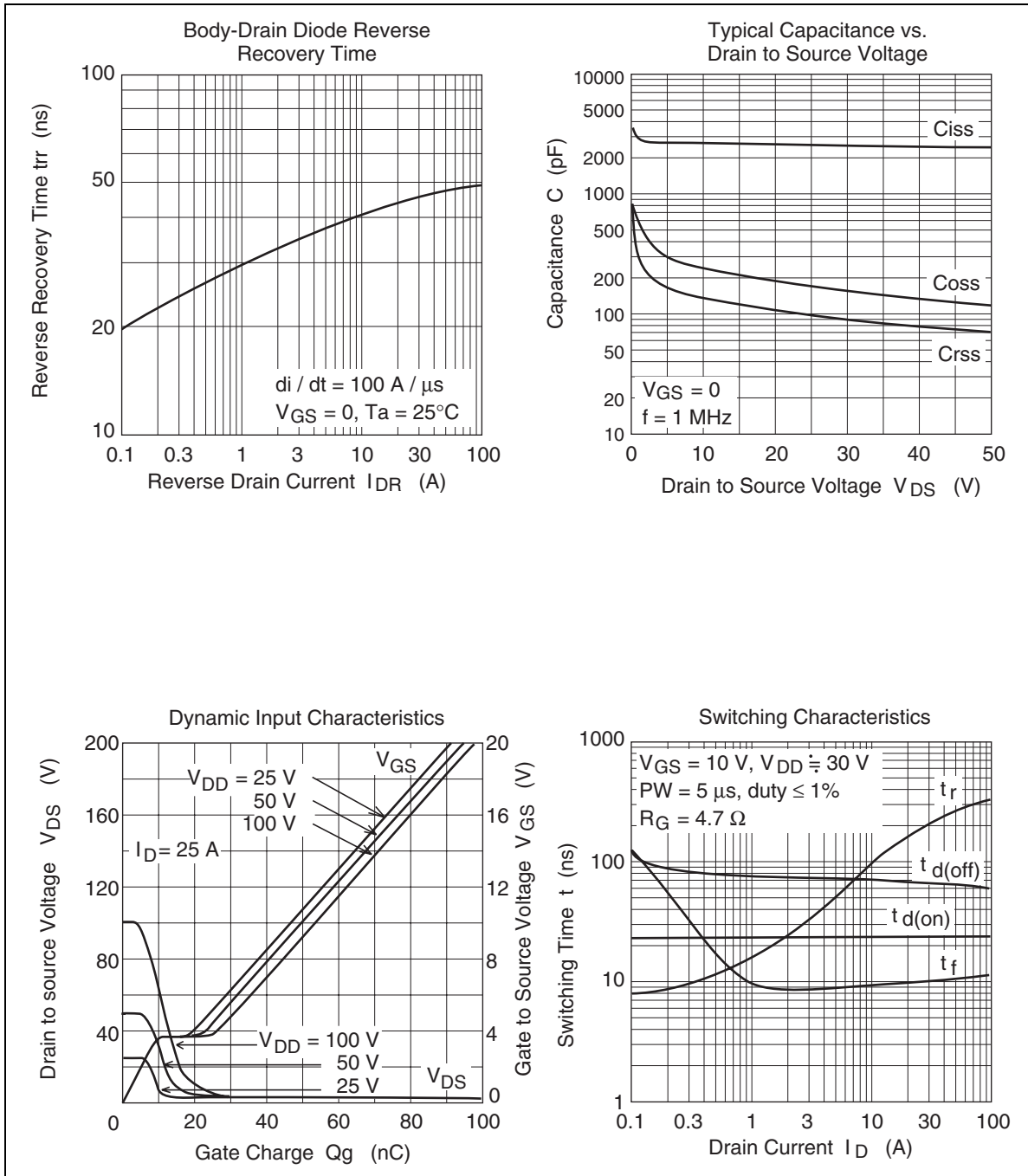
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu\text{A}$	$V_{DS} = 100 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$I_D = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}$ <sup>Note 1</sup>
Static drain to source on state resistance	$R_{DS(on)}$	—	25	35	$\text{m}\Omega$	$I_D = 12.5 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note 1</sup>
		—	30	45	$\text{m}\Omega$	$I_D = 12.5 \text{ A}$ , $V_{GS} = 4.5 \text{ V}$ <sup>Note 1</sup>
Forward transfer admittance	$ y_{fs} $	20	35	—	S	$I_D = 12.5 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note 1</sup>
Input capacitance	$C_{iss}$	—	2800	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	240	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	140	—	pF	$f = 1 \text{ MHz}$
Total gate charge	$Q_g$	—	50	—	nC	$V_{DD} = 50 \text{ V}$
Gate to source charge	$Q_{gs}$	—	9	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	11	—	nC	$I_D = 25 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	23	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 12.5 \text{ A}$
Rise time	$t_r$	—	110	—	ns	$R_L = 2.4 \text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	$R_g = 4.7 \text{ }\Omega$
Fall time	$t_f$	—	9.5	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.89	—	V	$I_F = 25 \text{ A}$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	45	—	ns	$I_F = 25 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

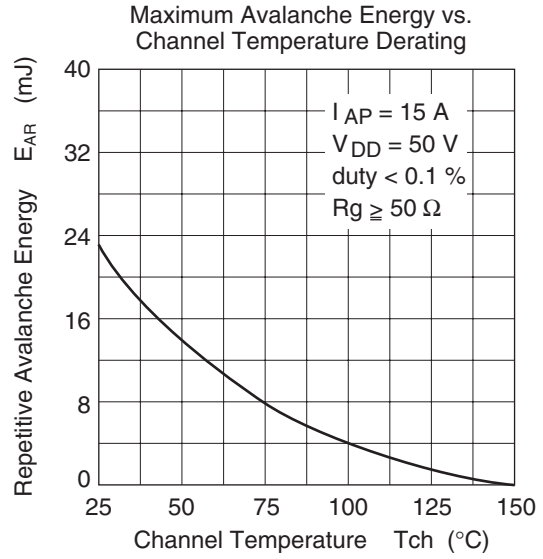
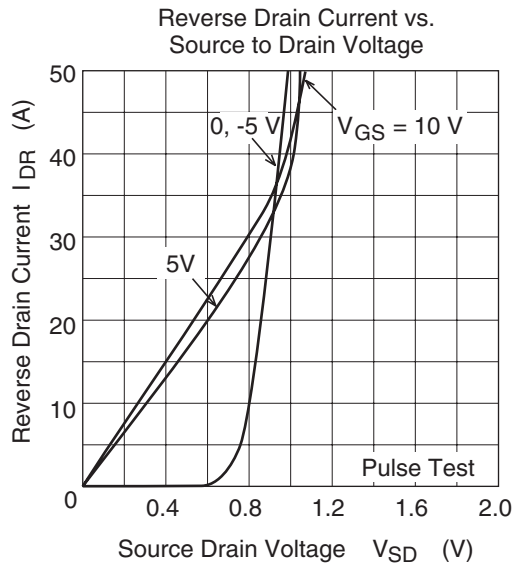
Notes: 1. Pulse test

Main Characteristics

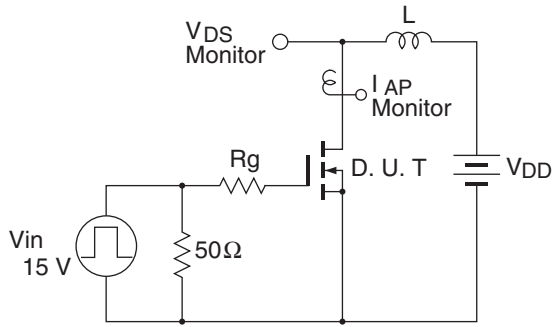




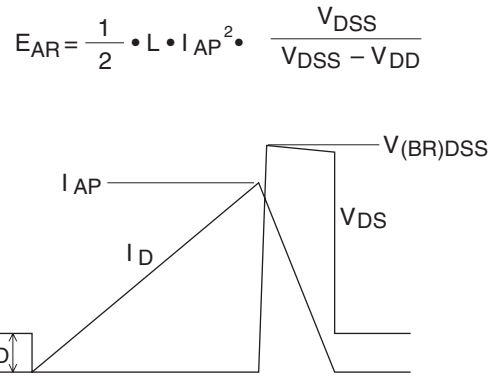


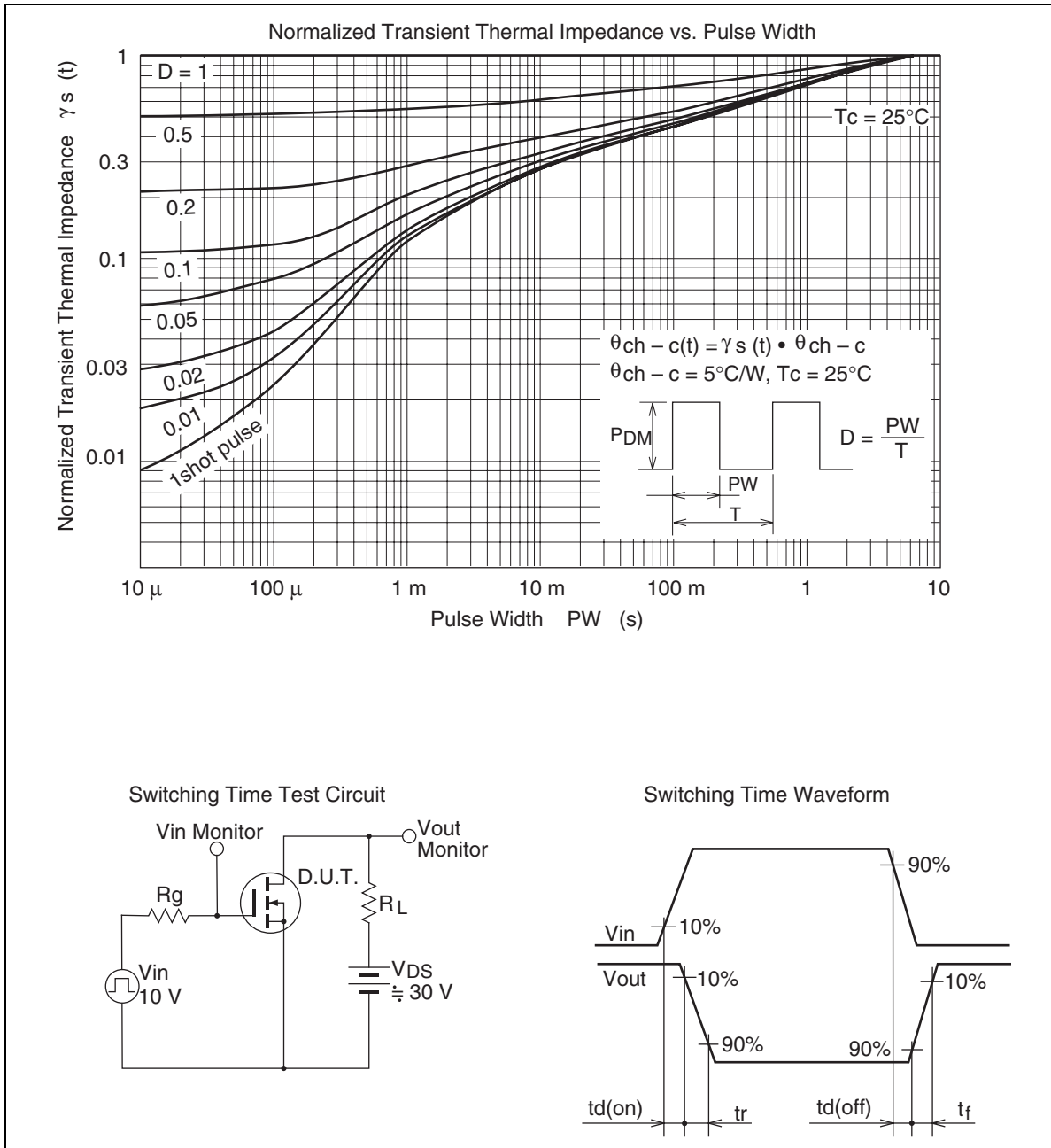


Avalanche Test Circuit

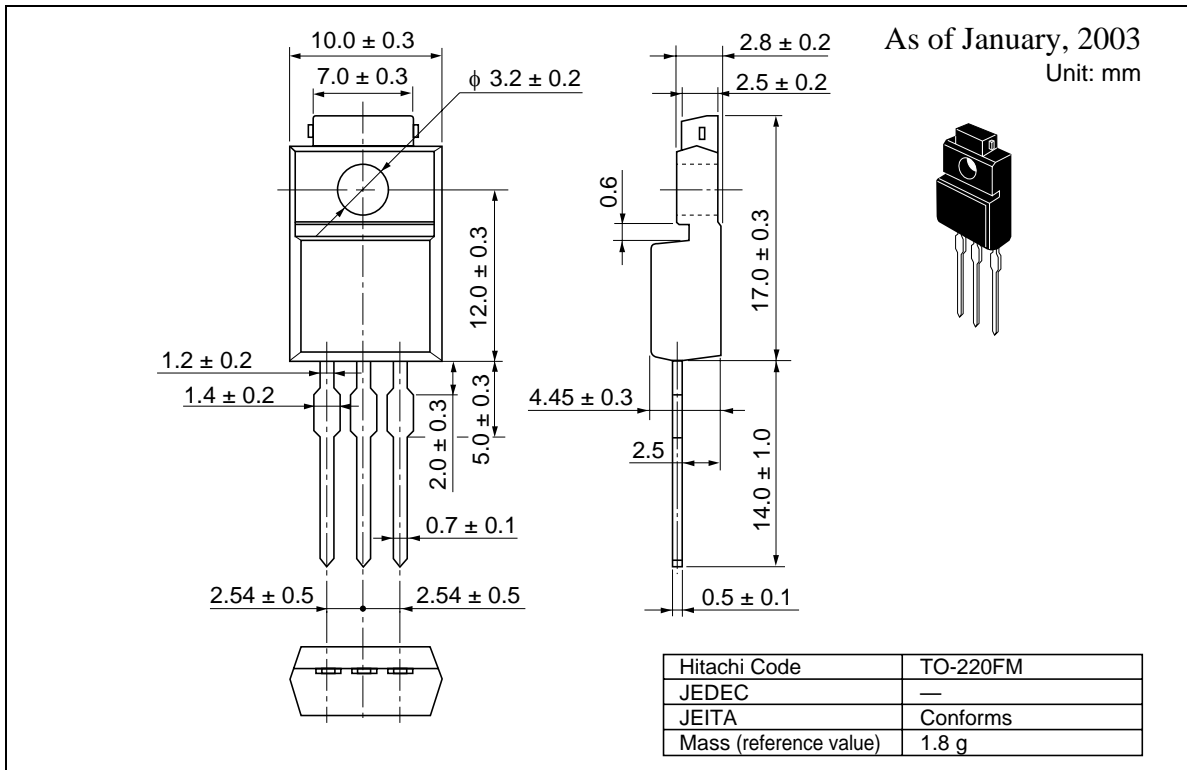


Avalanche Waveform





Package Dimensions



**Renesas Technology Corp.** Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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**Keep safety first in your circuit designs!**

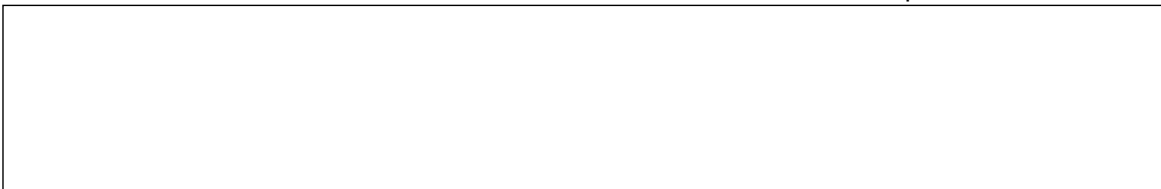
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