

## H7N1004LD, H7N1004LS, H7N1004LM

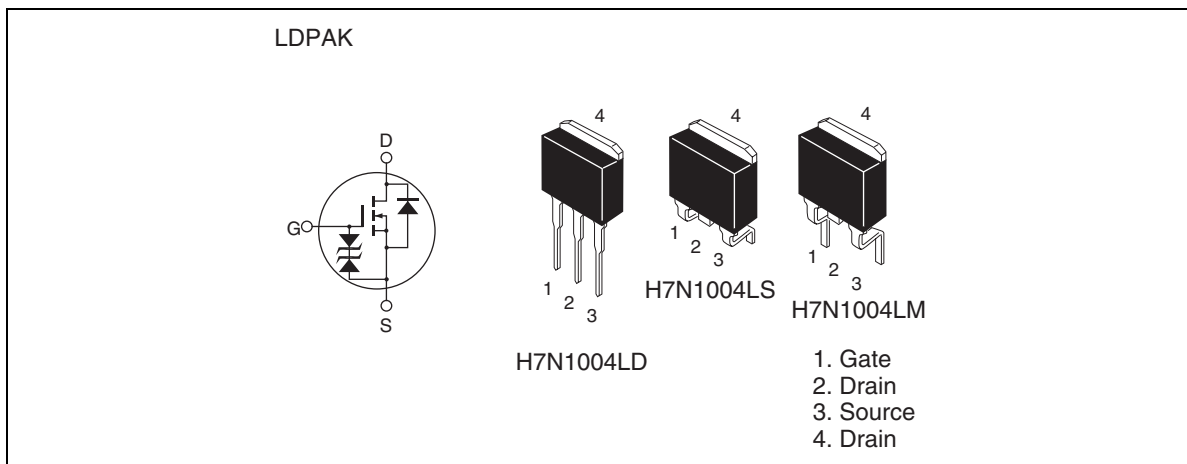
Silicon N-Channel MOSFET  
High-Speed Power Switching

REJ03G0072-0600Z  
(Previous ADE-208-1552E(Z))  
Rev.6.00  
Aug.27.2003

### Features

- Low on-resistance
- $R_{DS(on)} = 25 \text{ m}\Omega$  typ.
- Low drive current
- Available for 4.5 V gate drive

### Outline



**Absolute Maximum Ratings**

(Ta = 25°C)

<b>Item</b>	<b>Symbol</b>	<b>Value</b>	<b>Unit</b>
Drain to source voltage	V <sub>DSS</sub>	100	V
Gate to source voltage	V <sub>GSS</sub>	±20	V
Drain current	I <sub>D</sub>	30	A
Drain peak current	I <sub>D</sub> (pulse) <sup>Note 1</sup>	100	A
Body-drain diode reverse drain current	I <sub>DR</sub>	30	A
Avalanche current	I <sub>AP</sub> <sup>Note 3</sup>	15	A
Avalanche energy	E <sub>AR</sub> <sup>Note 3</sup>	22.5	mJ
Channel dissipation	P <sub>ch</sub> * <sup>Note 2</sup>	50	W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
2. Value at Tc = 25°C  
3. Value at Tch = 25°C, Rg ≥ 50 Ω

## H7N1004LD, H7N1004LS, H7N1004LM

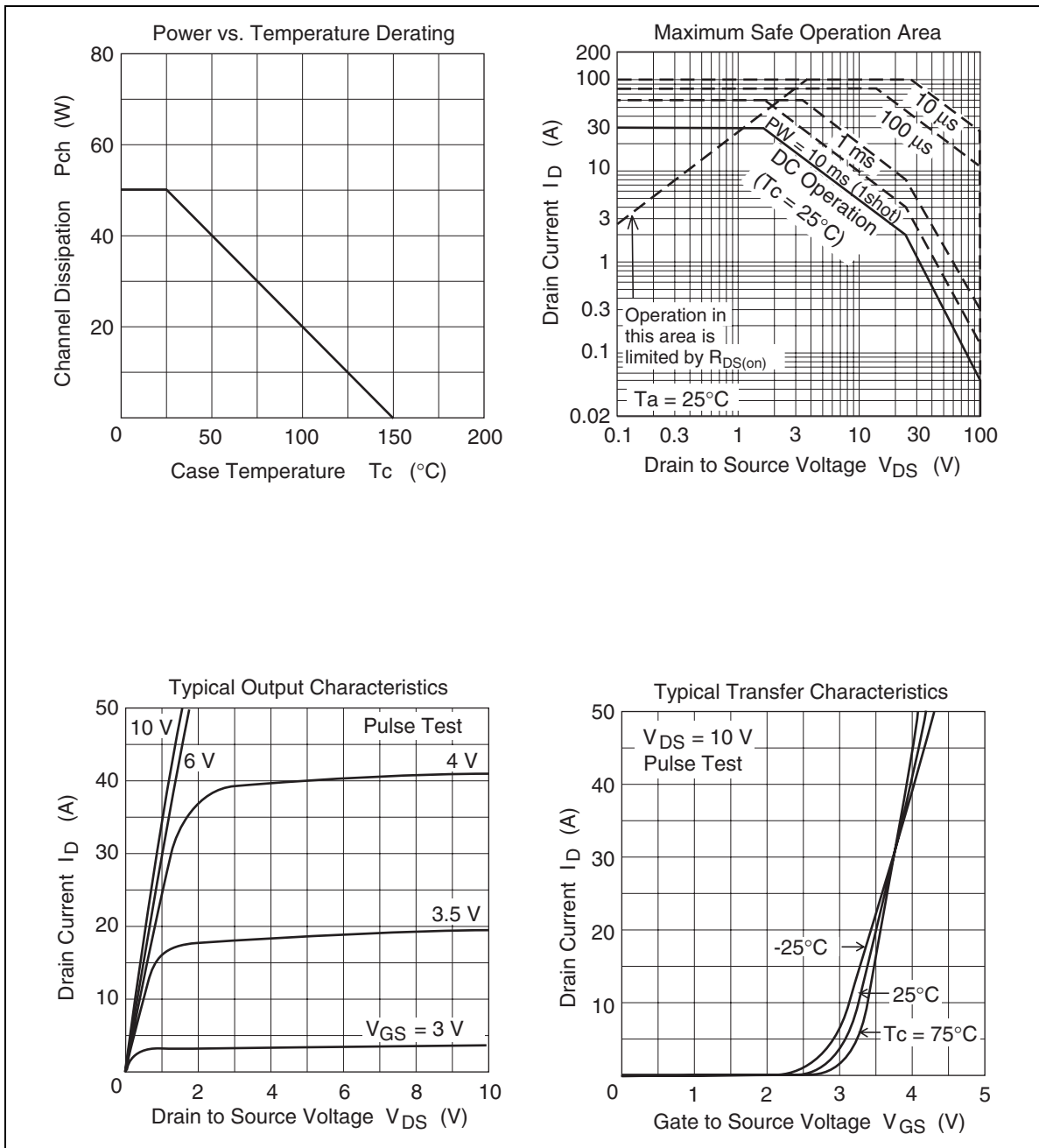
### Electrical Characteristics

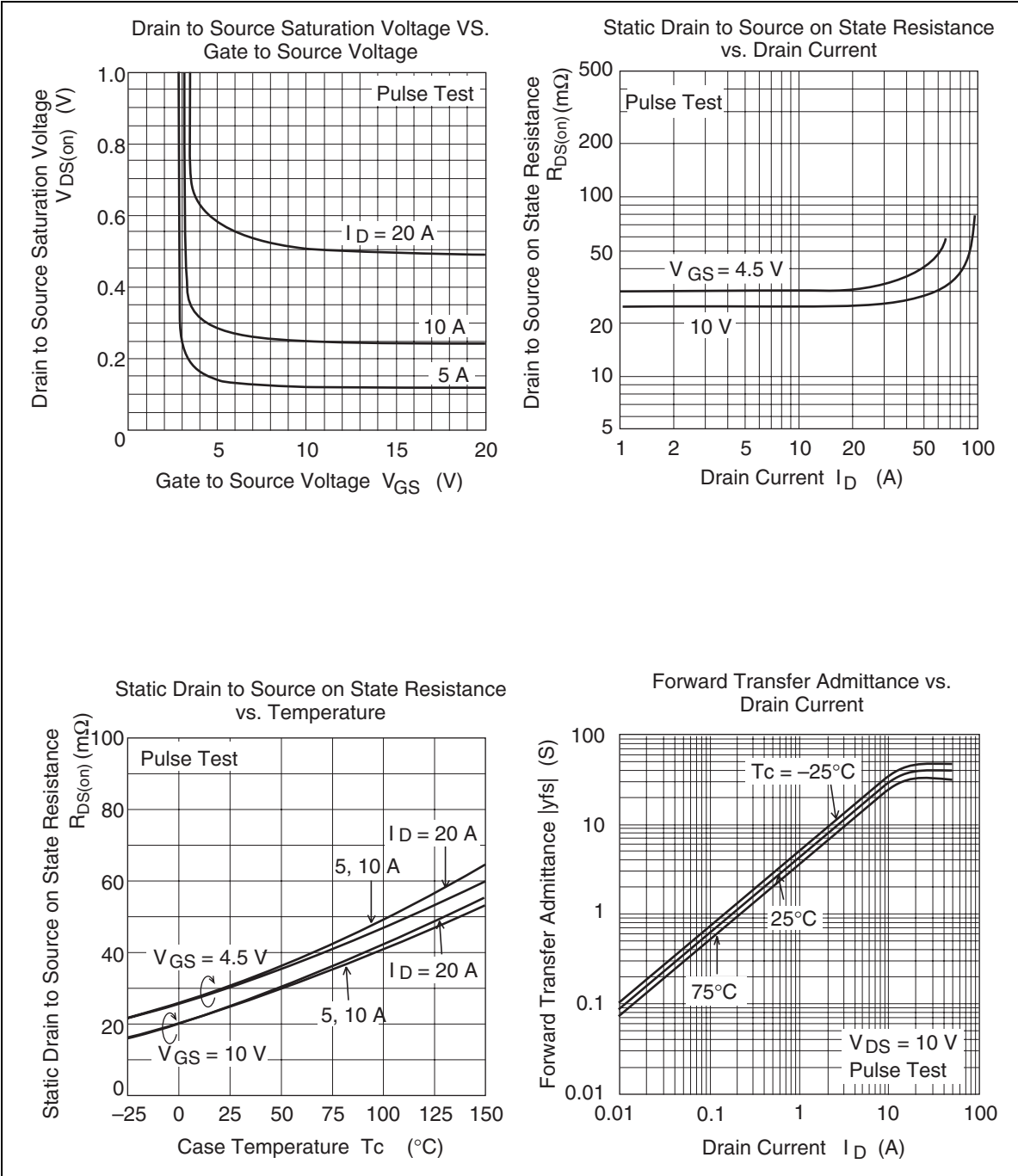
(T<sub>a</sub> = 25°C)

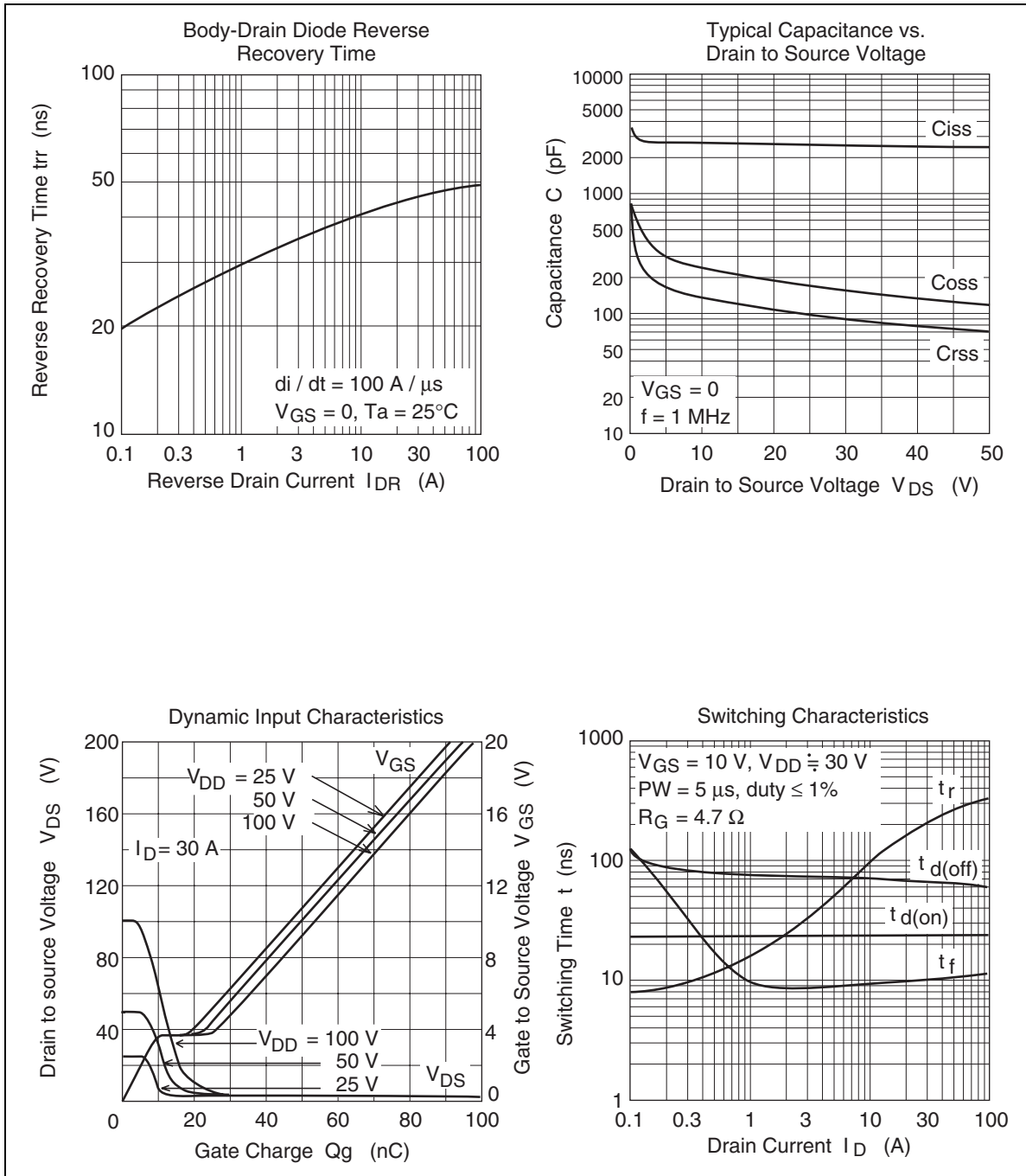
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	100	—	—	V	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0
Gate to source breakdown voltage	V <sub>(BR)GSS</sub>	±20	—	—	V	I <sub>G</sub> = ±100 μA, V <sub>DS</sub> = 0
Gate to source leak current	I <sub>GSS</sub>	—	—	±10	μA	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	10	μA	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0
Gate to source cutoff voltage	V <sub>GS(off)</sub>	1.5	—	2.5	V	I <sub>D</sub> = 1 mA, V <sub>DS</sub> = 10 V <sup>Note 1</sup>
Static drain to source on state resistance	R <sub>DS(on)</sub>	—	25	35	mΩ	I <sub>D</sub> = 15 A, V <sub>GS</sub> = 10 V <sup>Note 1</sup>
		—	30	45	mΩ	I <sub>D</sub> = 15 A, V <sub>GS</sub> = 4.5 V <sup>Note 1</sup>
Forward transfer admittance	y <sub>fs</sub>	22	37	—	S	I <sub>D</sub> = 15 A, V <sub>GS</sub> = 10 V <sup>Note 1</sup>
Input capacitance	C <sub>iss</sub>	—	2800	—	pF	V <sub>DS</sub> = 10 V
Output capacitance	C <sub>oss</sub>	—	240	—	pF	V <sub>GS</sub> = 0
Reverse transfer capacitance	C <sub>rss</sub>	—	140	—	pF	f = 1 MHz
Total gate charge	Q <sub>g</sub>	—	50	—	nC	V <sub>DD</sub> = 50 V
Gate to source charge	Q <sub>gs</sub>	—	9	—	nC	V <sub>GS</sub> = 10 V
Gate to drain charge	Q <sub>gd</sub>	—	11	—	nC	I <sub>D</sub> = 30 A
Turn-on delay time	t <sub>d(on)</sub>	—	23	—	ns	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A
Rise time	t <sub>r</sub>	—	120	—	ns	R <sub>L</sub> = 2 Ω
Turn-off delay time	t <sub>d(off)</sub>	—	70	—	ns	R <sub>g</sub> = 4.7 Ω
Fall time	t <sub>f</sub>	—	9.5	—	ns	
Body-drain diode forward voltage	V <sub>DF</sub>	—	0.9	—	V	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0
Body-drain diode reverse recovery time	t <sub>rr</sub>	—	47	—	ns	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 diF/dt = 100 A/μs

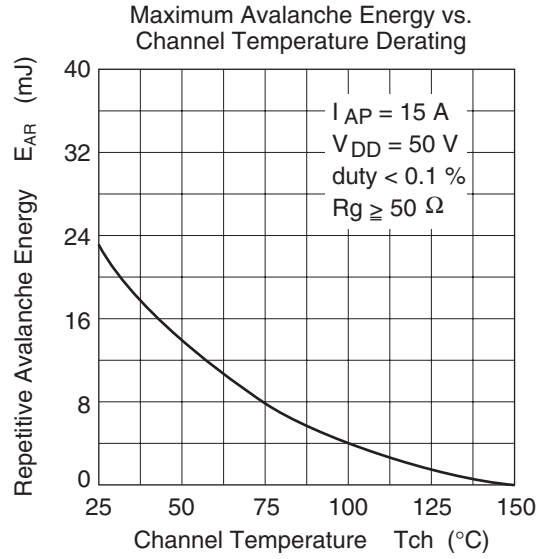
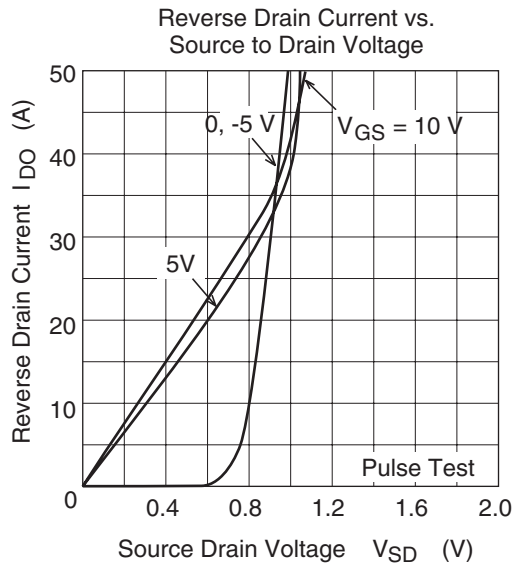
Notes: 1. Pulse test

Main Characteristics

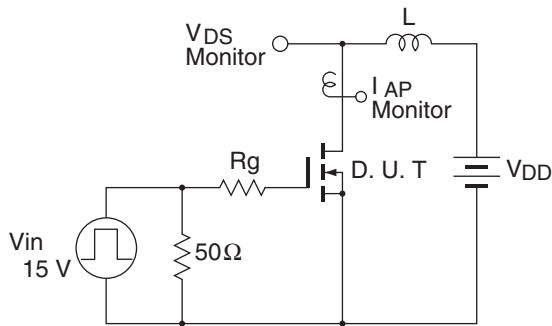




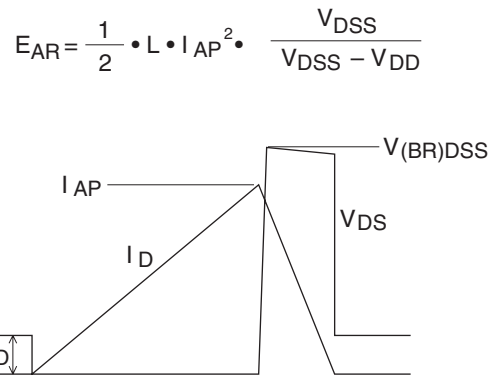


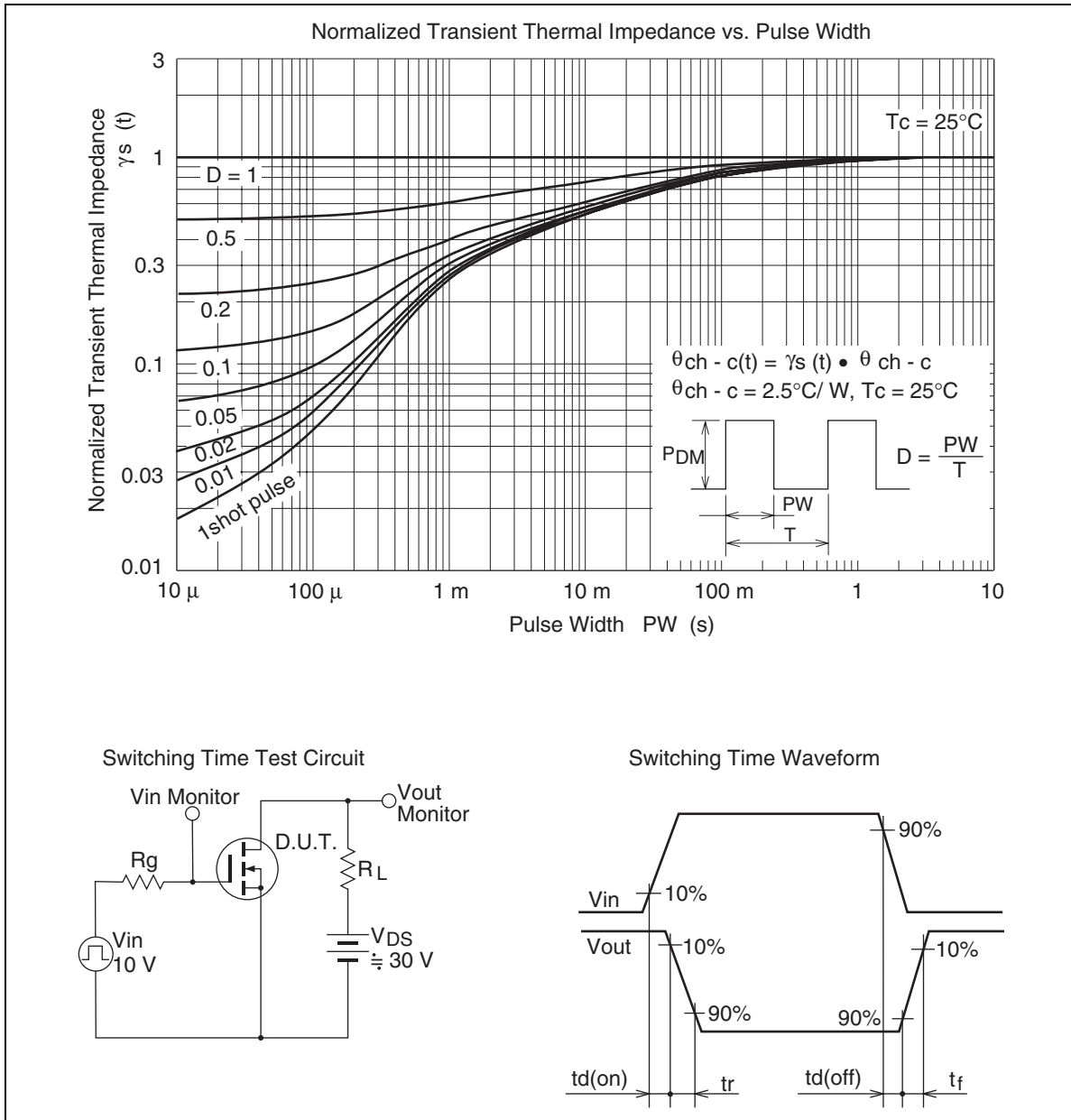


Avalanche Test Circuit



Avalanche Waveform

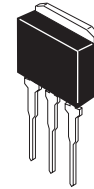
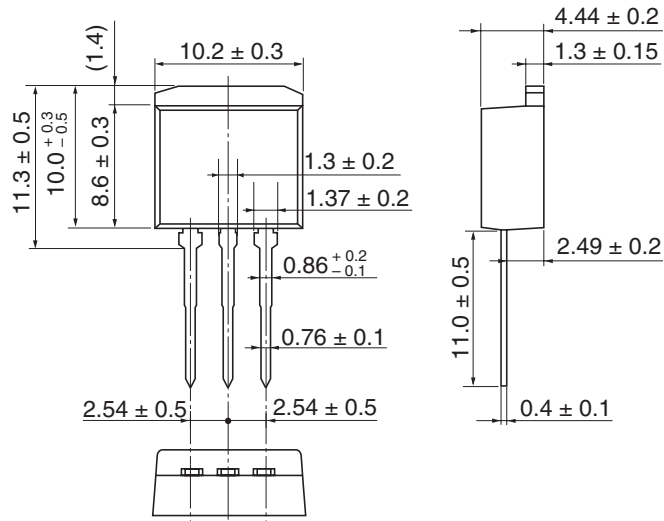




Package Dimensions

• H7N1004LD

As of January, 2003  
Unit: mm

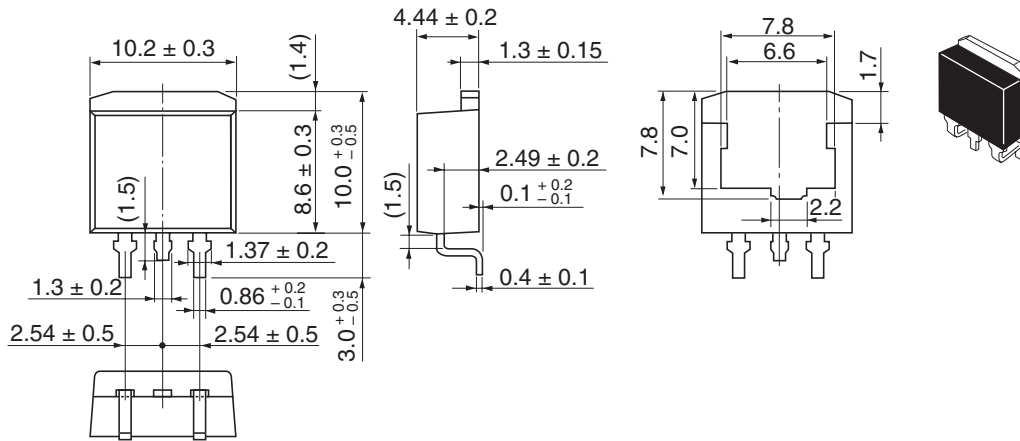


Package Code	LDBAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.40 g

H7N1004LD, H7N1004LS, H7N1004LM

• H7N1004LS

As of January, 2003  
Unit: mm

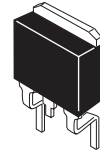
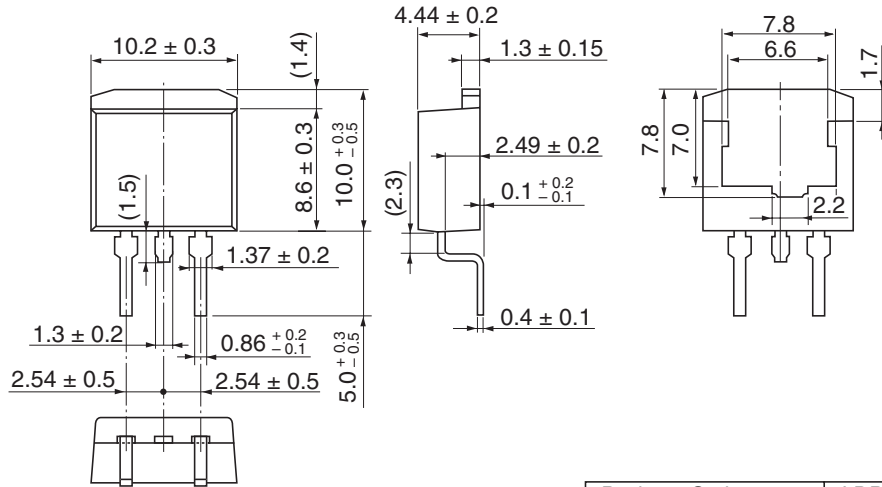


Package Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.30 g

**H7N1004LD, H7N1004LS, H7N1004LM**

• H7N1004LM

As of January, 2003  
Unit: mm



Package Code	LDPAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

**Renesas Technology Corp.** Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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**Keep safety first in your circuit designs!**

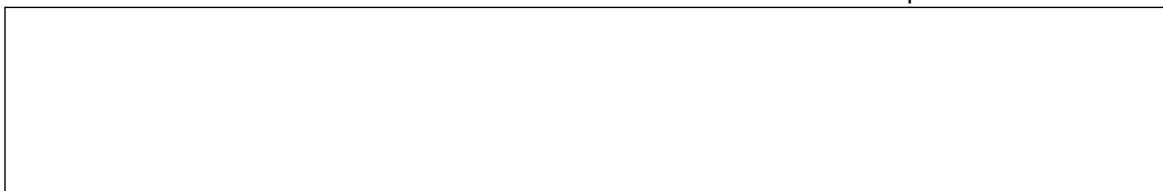
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