HAT1047R, HAT1047RJ

Silicon P Channel Power MOS FET
High Speed Power Switching

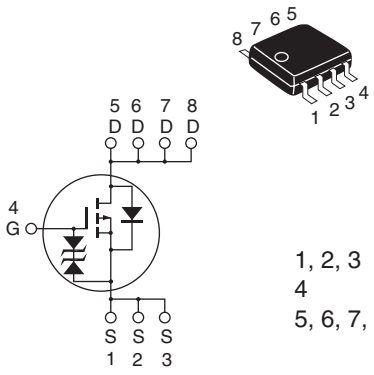
REJ03G0074-0500Z
(Previous ADE-208-1545D(Z))
Rev.5.00
Aug.27.2003

Features

- For Automotive Application (at Type Code "J")
- Low on-resistance
- Capable of –4.5 V gate drive
- High density mounting

Outline

SOP-8



1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage		V_{DSS}	–30	V
Gate to source voltage		V_{GSS}	±20	V
Drain current		I_D	–14	A
Drain peak current		$I_{D(pulse)}$ Note1	–112	A
Body-drain diode reverse drain current		I_{DR}	–14	A
Avalanche current	HAT1047R	I_{AP} Note3	—	—
	HAT1047RJ		–14	A
Avalanche energy	HAT1047R	E_{AR} Note3	—	—
	HAT1047RJ		19.6	mJ
Channel dissipation		Pch Note2	2.5	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1 %
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s
3. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics

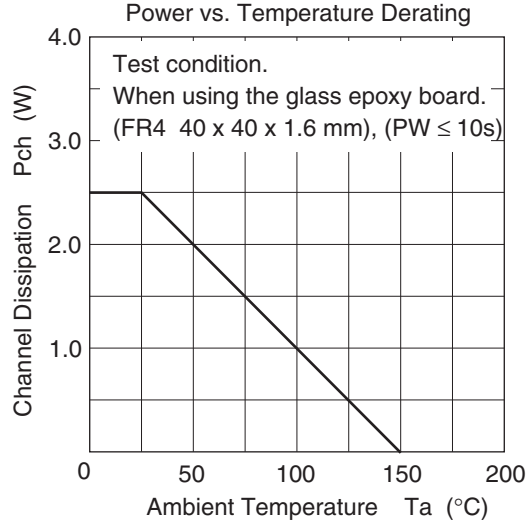
(Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage		$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage		$V_{(BR)GSS}$	±20	—	—	mV	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ± 16V, V_{DS} = 0
Zero gate voltage drain current		I_{DSS}	—	—	±1	µA	V_{DS} = –30 V, V_{GS} = 0
Zero gate voltage drain current	HAT1047R	I_{DSS}	—	—	—	µA	V_{DS} = –24 V, V_{GS} = 0
	HAT1047RJ	I_{DSS}	—	—	–20	µA	Ta = 125°C
Gate to source cutoff voltage		$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance		$R_{DS(on)}$	—	10	12	mΩ	I_D = –7 A, V_{GS} = –10 V Note4
		$R_{DS(on)}$	—	19	25	mΩ	I_D = –7 A, V_{GS} = –4.5 V Note4
Forward transfer admittance		$\|y_{fs}\|$	9.6	16	—	S	I_D = –7 A, V_{DS} = –10 V Note4
Input capacitance		Ciss	—	3500	—	pF	V_{DS} = –10 V
Output capacitance		Coss	—	750	—	pF	V_{GS} = 0
Reverse transfer capacitance		Crss	—	520	—	pF	f = 1 MHz
Total gate charge		Qg	—	64	—	nc	V_{DD} = –10 V
Gate to source charge		Qgs	—	10	—	nc	V_{GS} = –10 V
Gate to drain charge		Qgd	—	12	—	nc	I_D = –14 A
Turn-on delay time		$t_{d(on)}$	—	23	—	ns	V_{GS} = –10 V, I_D = –7A
Rise time		t_r	—	45	—	ns	V_{DD} ≅ –10 V
Turn-off delay time		$t_{d(off)}$	—	80	—	ns	R_L = 1.43 Ω
Fall time		t_f	—	25	—	ns	R_L = 4.7 Ω
Body–drain diode forward voltage		V_{DF}	—	–0.82	–1.07	V	IF = –14 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time		t_{rr}	—	45	—	ns	IF = –14 A, V_{GS} = 0 diF/ dt = 100 A/µs

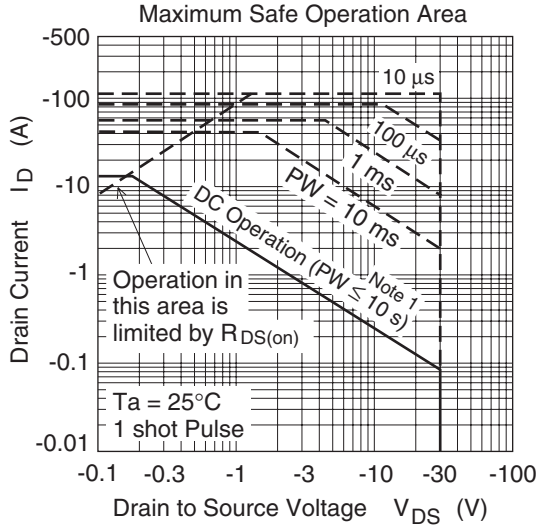
Notes: 4. Pulse test

Main Characteristics

Power vs. Temperature Derating

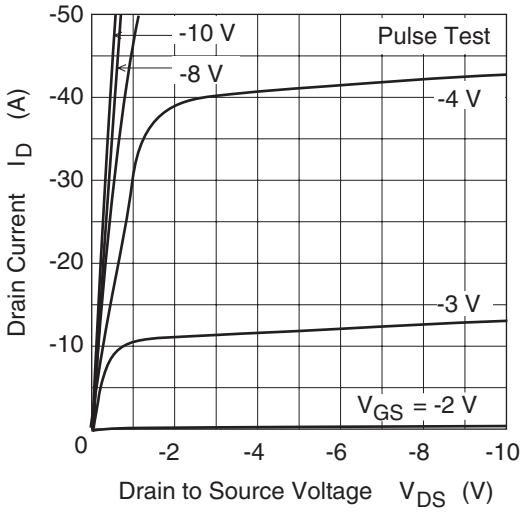


Maximum Safe Operation Area

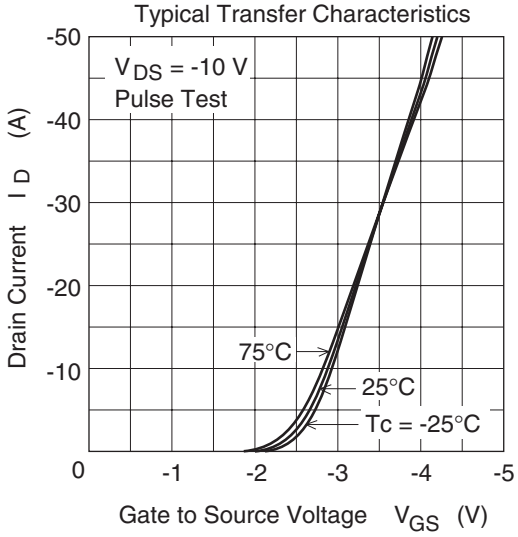


Note 1:
When using the glass epoxy board.
(FR4 40 x 40 x 1.6 mm)

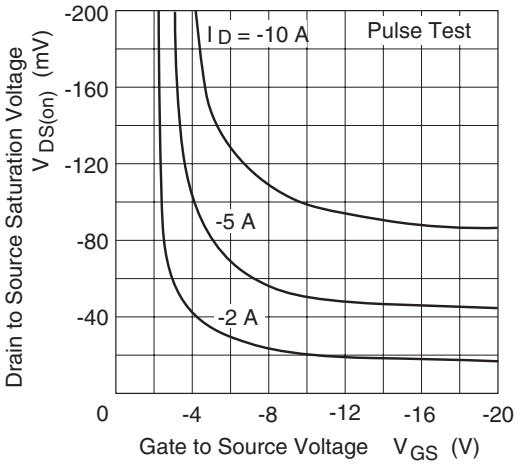
Typical Output Characteristics



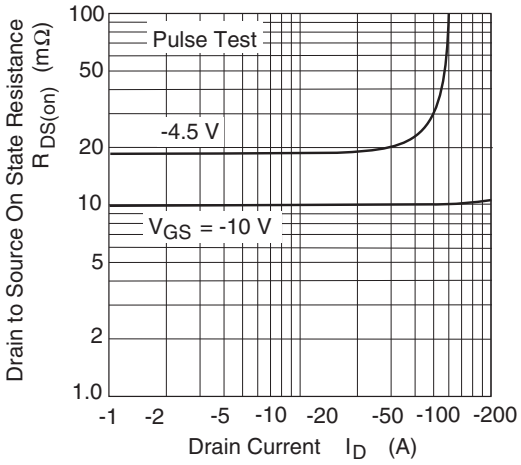
Typical Transfer Characteristics



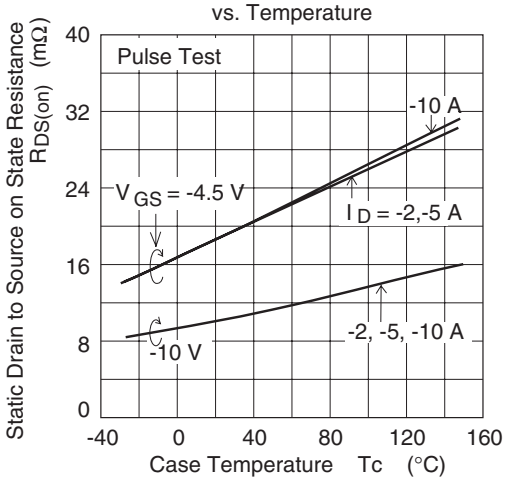
Drain to Source Saturation Voltage vs. Gate to Source Voltage



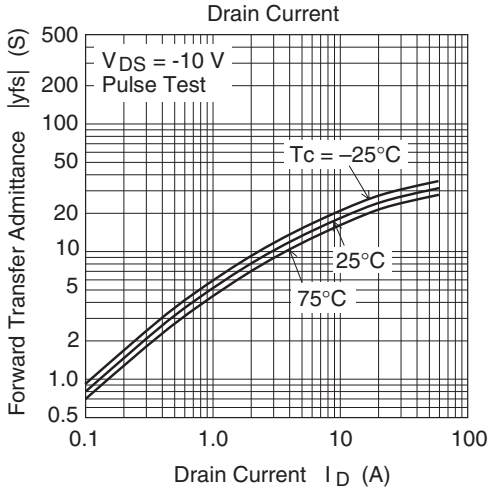
Static Drain to Source on State Resistance vs. Drain Current



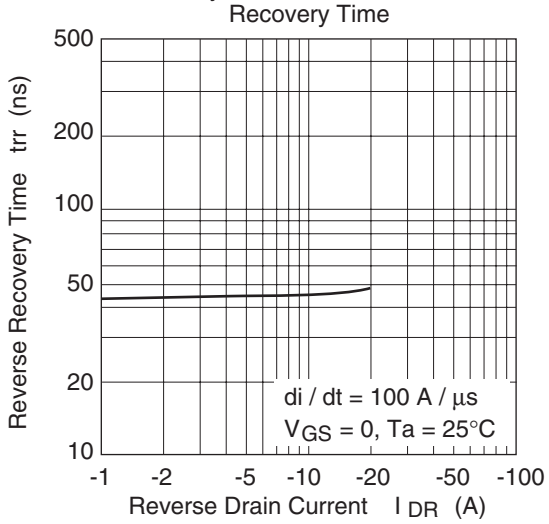
Static Drain to Source on State Resistance vs. Temperature



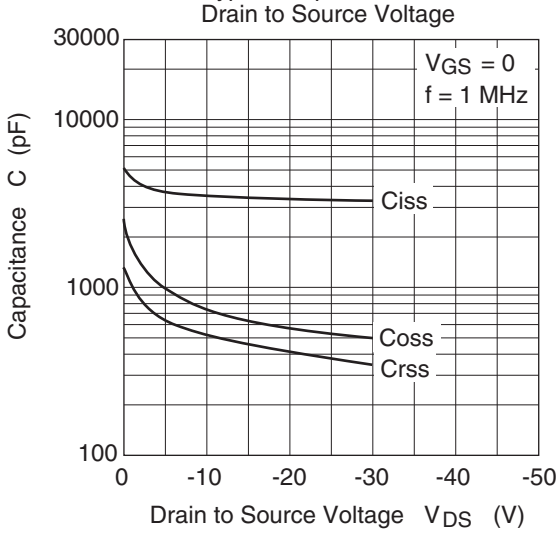
Forward Transfer Admittance vs. Drain Current



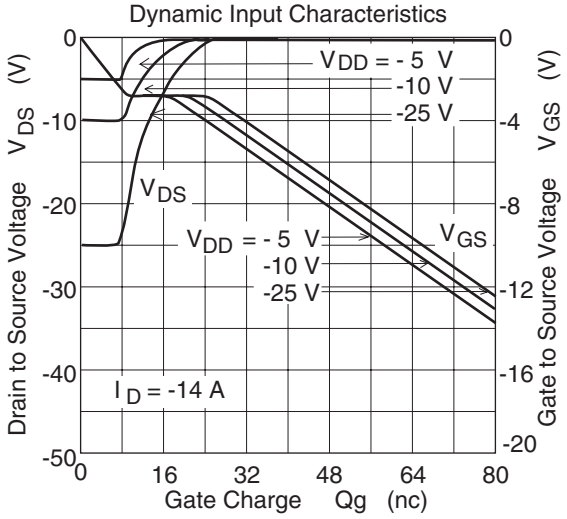
Body-Drain Diode Reverse Recovery Time



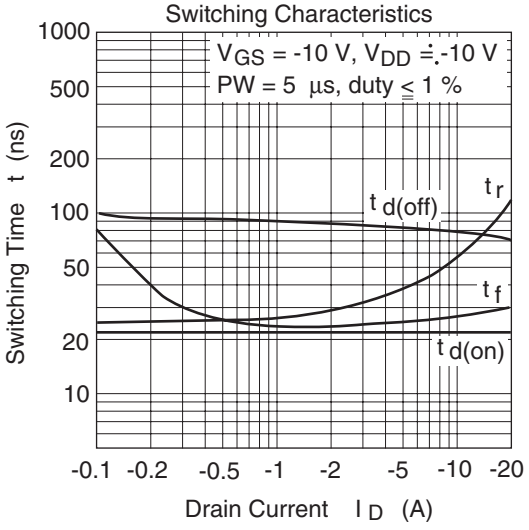
Typical Capacitance vs. Drain to Source Voltage



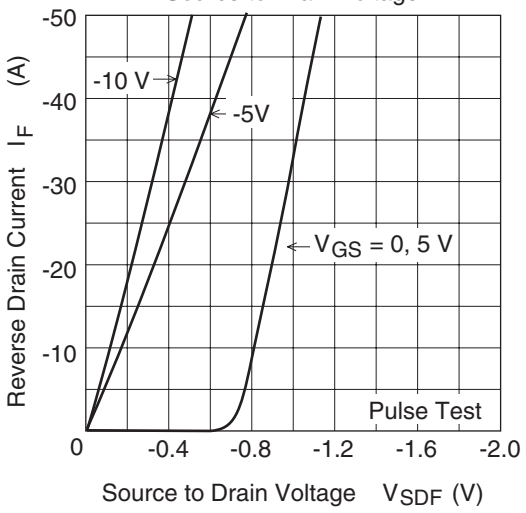
Dynamic Input Characteristics



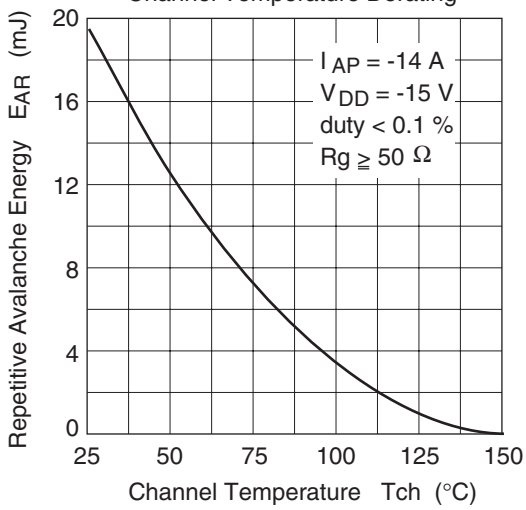
Switching Characteristics



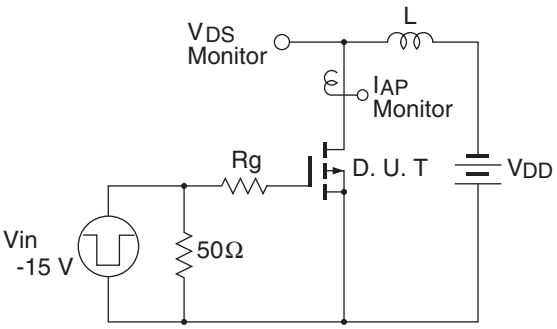
Reverse Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

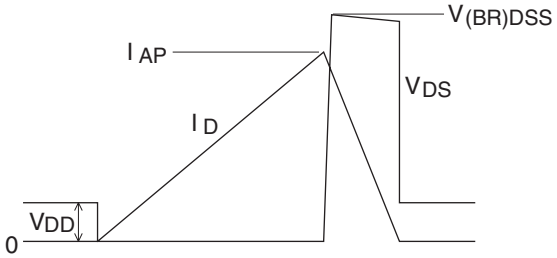


Avalanche Test Circuit

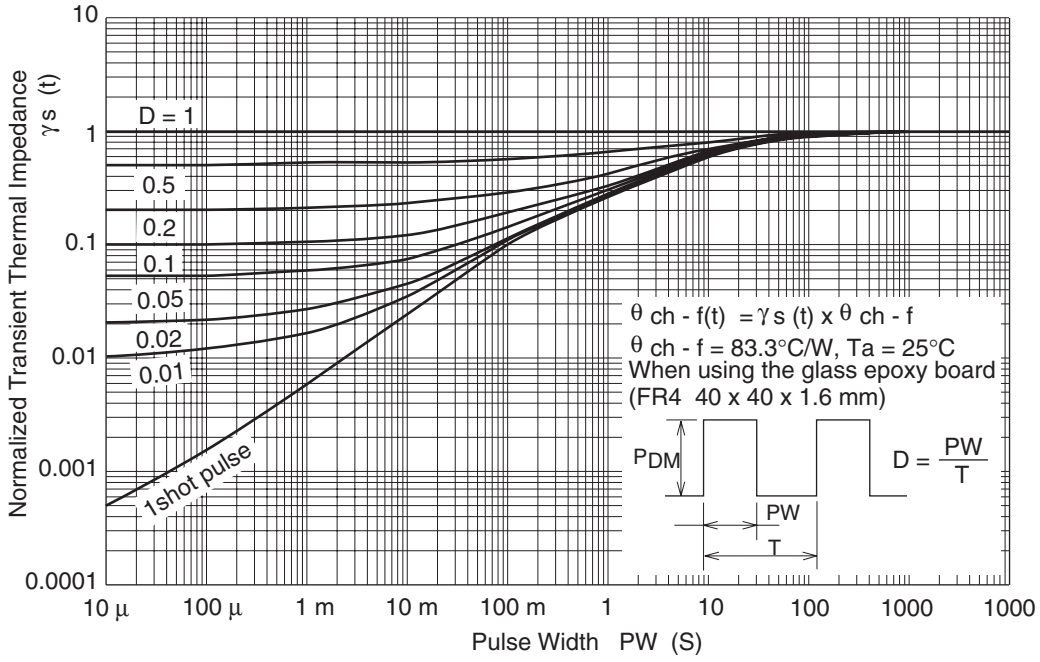


Avalanche Waveform

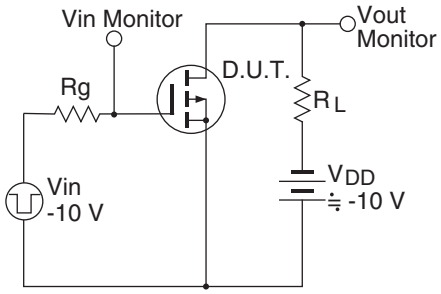
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



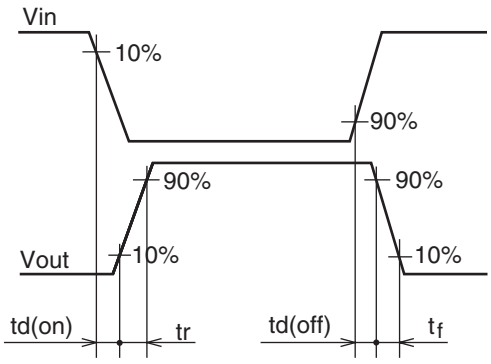
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



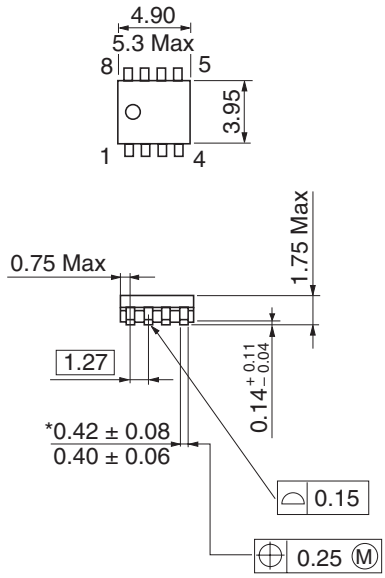
Switching Time Waveform



Package Dimensions

As of January, 2003

Unit: mm



*Dimension including the plating thickness
Base material dimension

Package Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

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