

## HAT1055R, HAT1055RJ

Silicon P Channel Power MOS FET  
High Speed Power Switching

REJ03G0067-0100Z

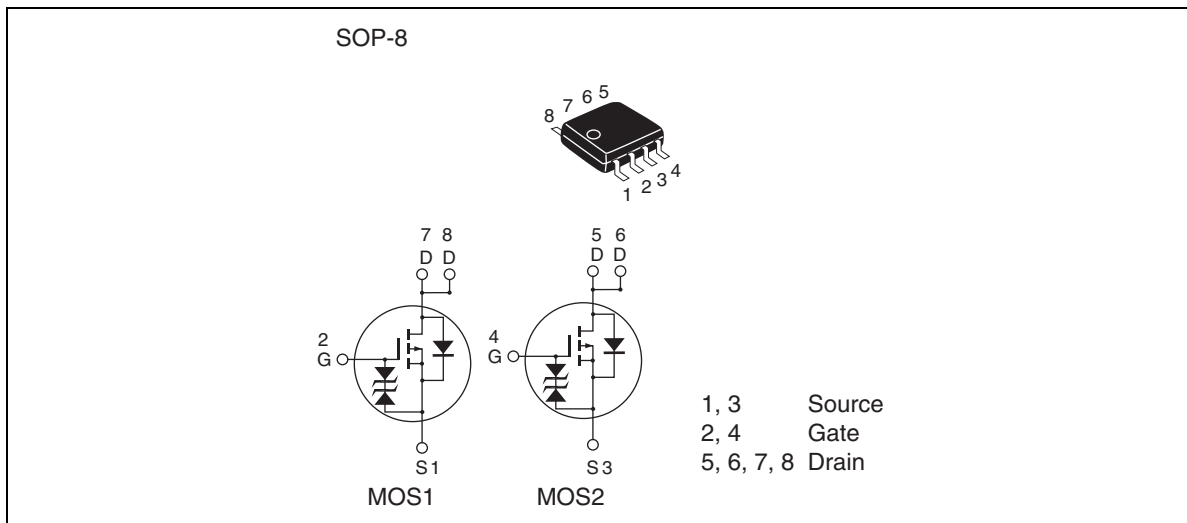
Rev.1.00

Aug.29.2003

### Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- “J” is for Automotive application  
High temperature D-S leakage guarantee  
Avalanche rating

### Outline



**Absolute Maximum Ratings**

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		HAT1055R	HAT1055RJ	
Drain to source voltage	V <sub>DSS</sub>	-60	-60	V
Gate to source voltage	V <sub>GSS</sub>	±20	±20	V
Drain current	I <sub>D</sub>	-5	-5	A
Drain peak current	I <sub>D</sub> (pulse) <sup>Note1</sup>	-40	-40	A
Avalanche current	I <sub>AP</sub> <sup>Note4</sup>	—	-5	A
Avalanche energy	E <sub>AR</sub> <sup>Note4</sup>	—	2.14	mJ
Channel dissipation	P <sub>ch</sub> <sup>Note2</sup>	2	2	W
Channel dissipation	P <sub>ch</sub> <sup>Note3</sup>	3	3	W
Channel temperature	T <sub>ch</sub>	150	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	-55 to +150	°C

Notes: 1. PW ≤ 10μs, duty cycle ≤ 1%

2. 1 Drive operation: When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s

3. 2 Drive operation: When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s

4. Value at T<sub>ch</sub> = 25°C, R<sub>g</sub> ≥ 50 Ω

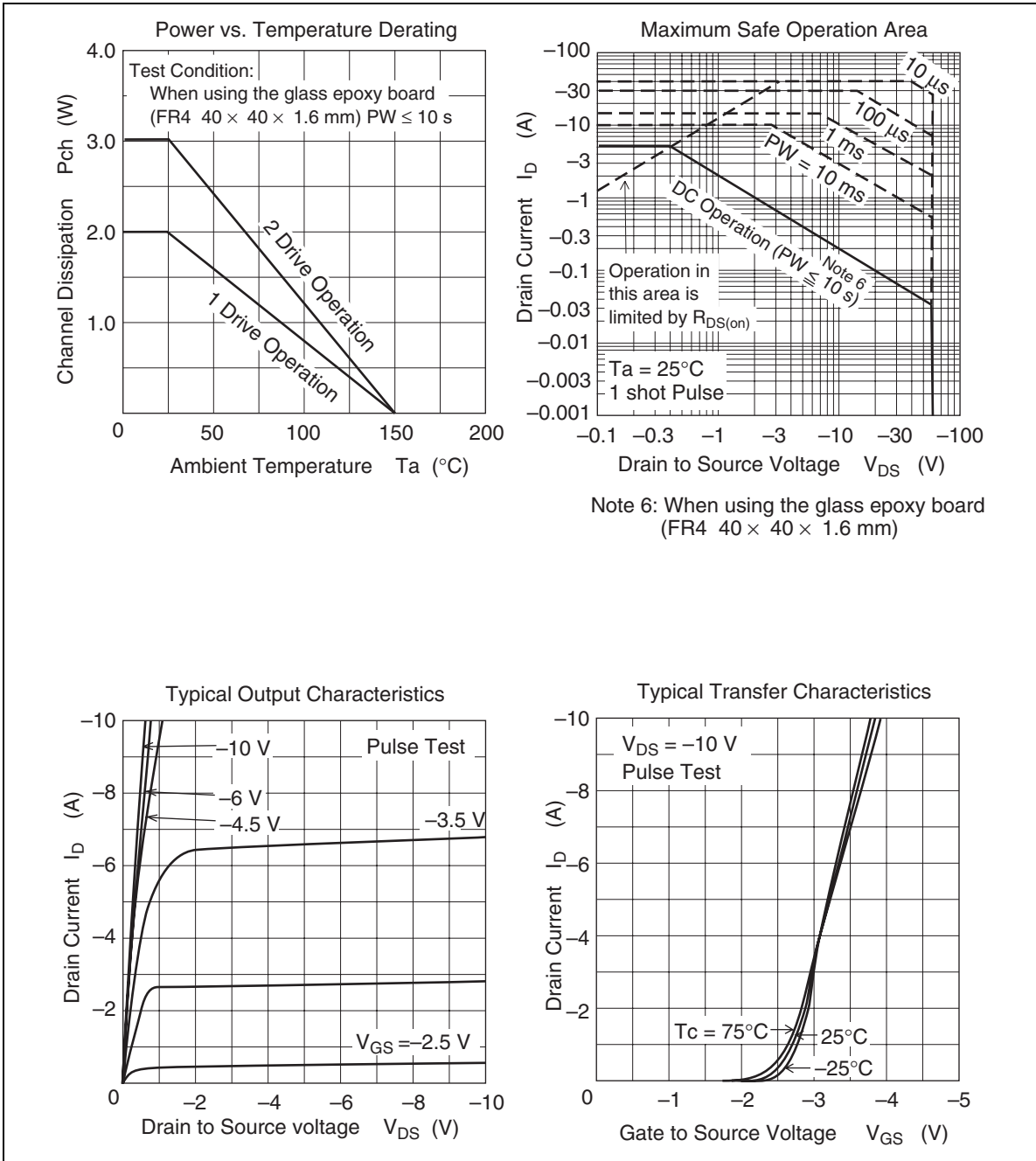
**Electrical Characteristics**

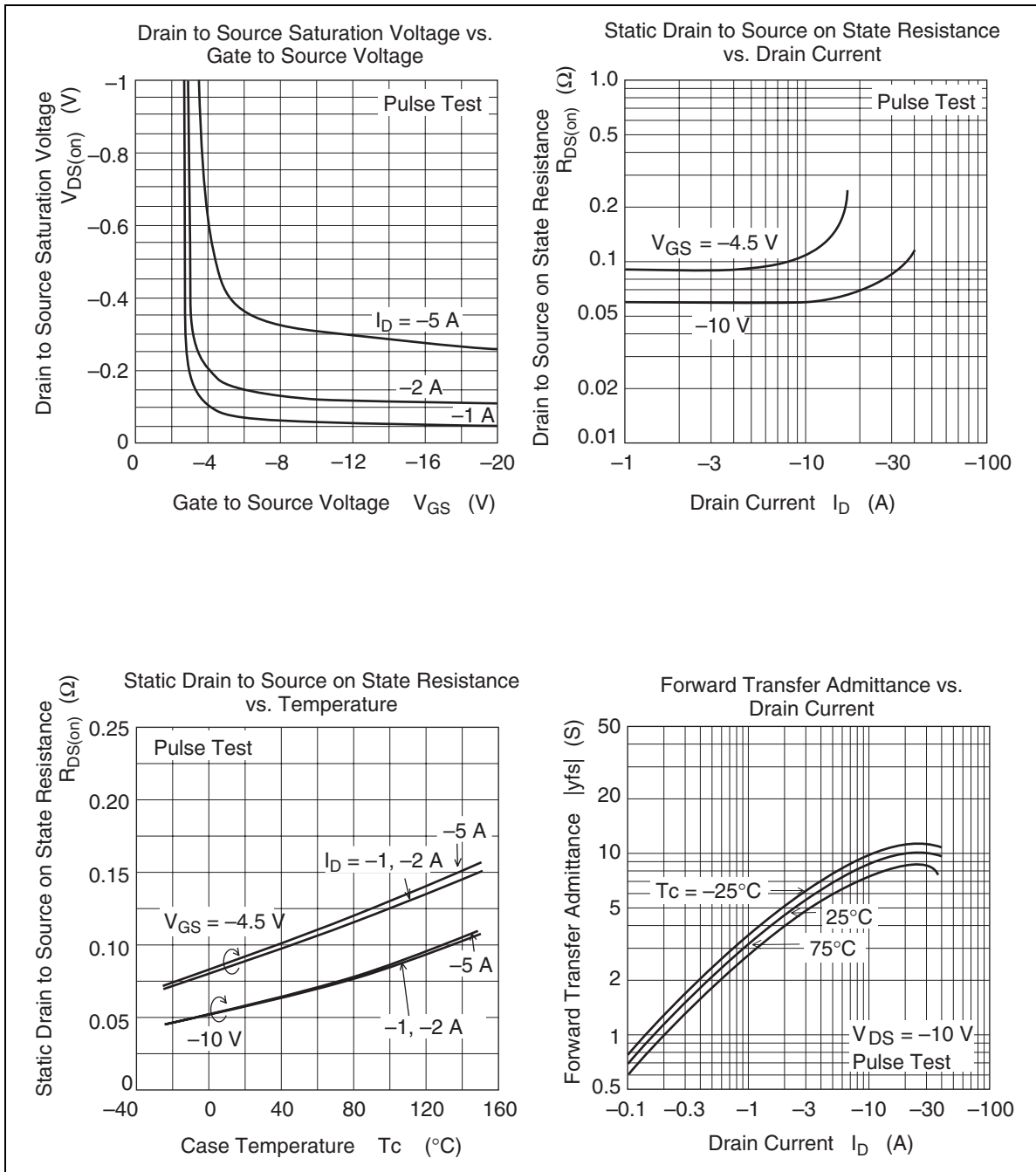
(Ta = 25°C)

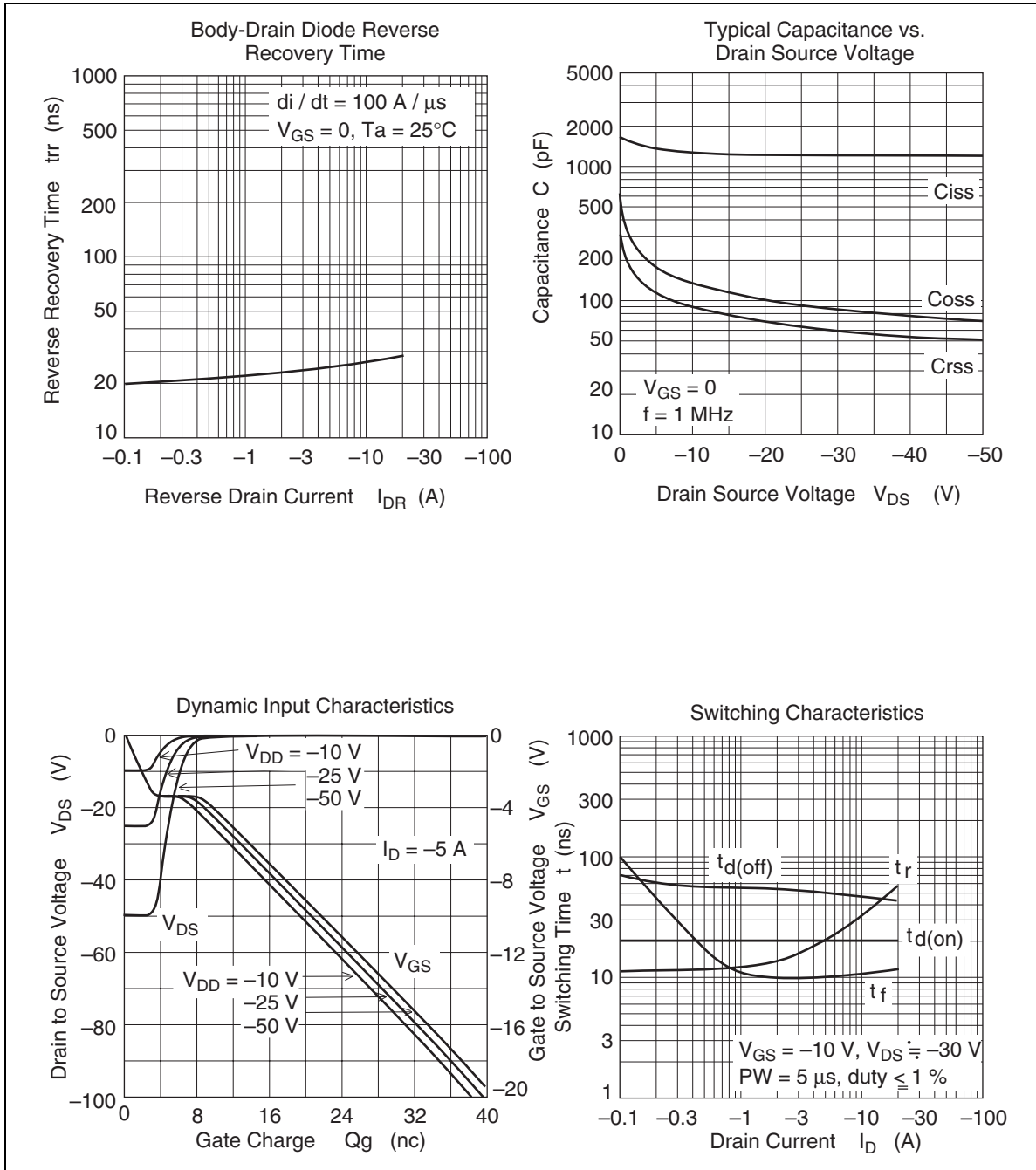
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}$ , $V_{GS} = 0$
Gate to Source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \text{ } \mu\text{A}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-1	μA	$V_{DS} = -60 \text{ V}$ , $V_{GS} = 0$
Zero gate voltage drain current	HAT1055R	$I_{DSS}$	—	—	μA	$V_{DS} = -48 \text{ V}$ , $V_{GS} = 0$
	HAT1055RJ	$I_{DSS}$	—	-10	μA	Ta = 125°C
Gate to source leak current	$I_{GSS}$	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$ , $I_D = -1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	3	5	—	S	$I_D = -2.5 \text{ A}^{\text{Note5}}$ , $V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	60	76	mΩ	$I_D = -2.5 \text{ A}^{\text{Note5}}$ , $V_{GS} = -10 \text{ V}$
	$R_{DS(on)}$	—	90	130	mΩ	$I_D = -2.5 \text{ A}^{\text{Note5}}$ , $V_{GS} = -4.5 \text{ V}$
Input capacitance	$C_{iss}$	—	1350	—	pF	$V_{DS} = -10 \text{ V}$ , $V_{GS} = 0$
Output capacitance	$C_{oss}$	—	135	—	pF	f = 1 MHz
Reverse transfer capacitance	$C_{rss}$	—	85	—	pF	
Total gate charge	$Q_g$	—	21	—	nC	$V_{DD} = -25 \text{ V}$
Gate to source charge	$Q_{gs}$	—	3	—	nC	$V_{GS} = -10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	4	—	nC	$I_D = -5 \text{ A}$
Turn-on delay time	td(on)	—	20	—	ns	$V_{GS} = -10 \text{ V}$ , $I_D = -2.5 \text{ A}$
Rise time	tr	—	15	—	ns	$V_{DD} \cong -30 \text{ V}$
Turn-off delay time	td(off)	—	55	—	ns	$R_L = 12 \text{ } \Omega$
Fall time	tf	—	10	—	ns	$R_G = 4.7 \text{ } \Omega$
Body-drain diode forward voltage	$V_{DF}$	—	-0.85	-1.10	V	$I_F = -5 \text{ A}$ , $V_{GS} = 0^{\text{Note5}}$
Body-drain diode reverse recovery time	trr	—	25	—	ns	$I_F = -5 \text{ A}$ , $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

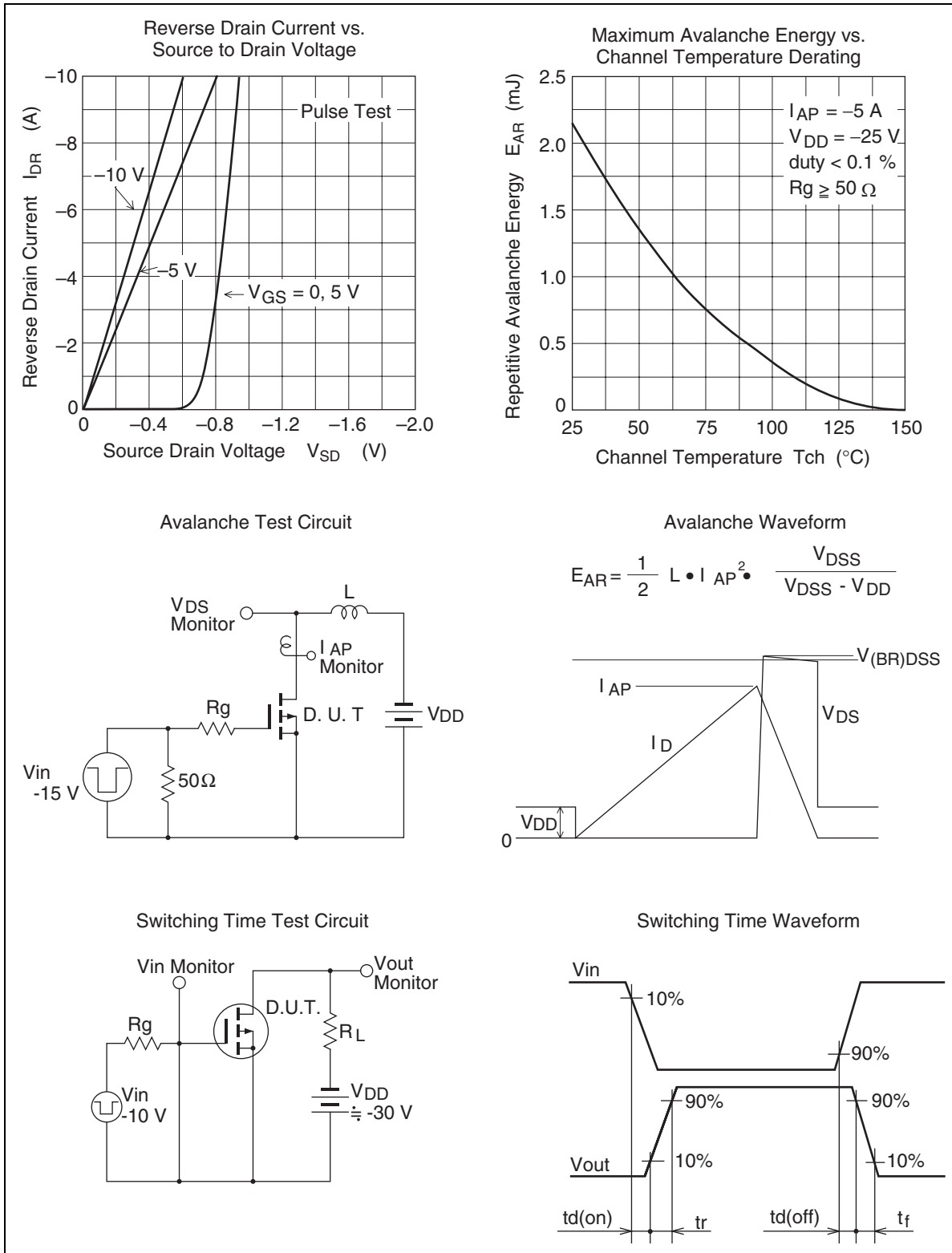
Notes: 5. Pulse test

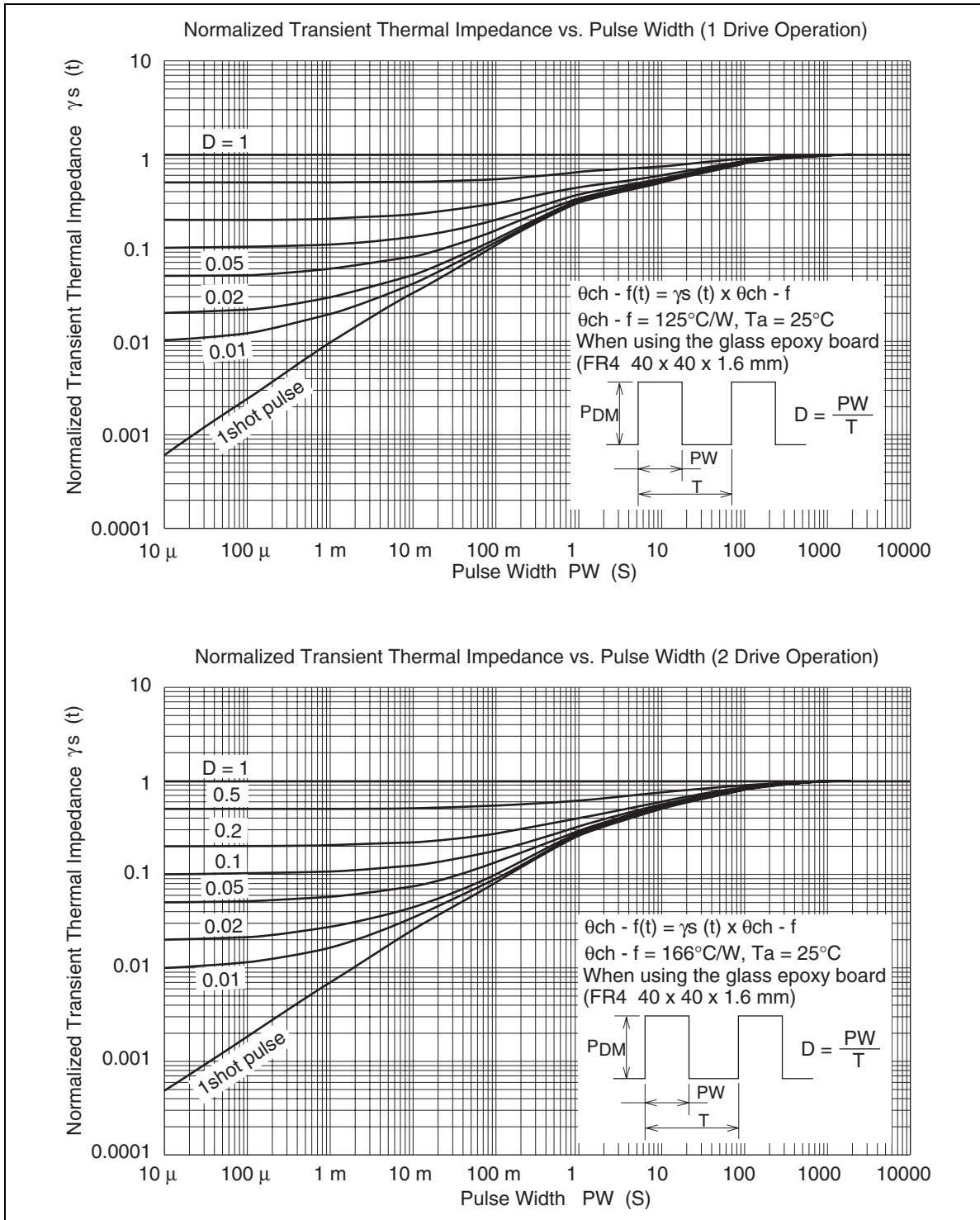
Main Characteristics





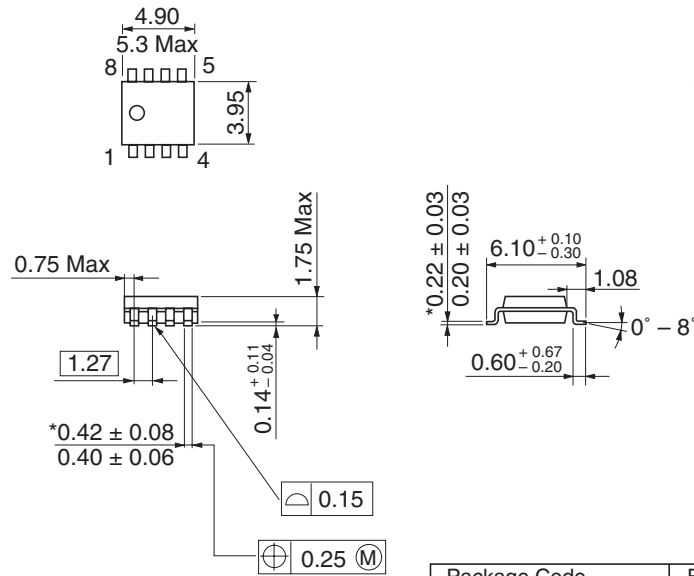






Package Dimensions

As of January, 2003  
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Package Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

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