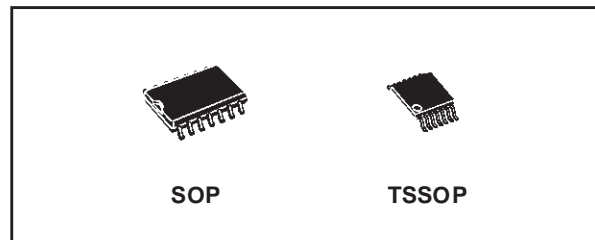




# 74LVX132

## LOW VOLTAGE CMOS QUAD 2-INPUT SCHMITT NAND GATE WITH 5V TOLERANT INPUTS

- HIGH SPEED :  
 $t_{PD} = 5.9\text{ns}$  (TYP.) at  $V_{CC} = 3.3\text{V}$
- 5V TOLERANT INPUTS
- LOW POWER DISSIPATION:  
 $I_{CC} = 2\ \mu\text{A}$  (MAX.) at  $T_A = 25^\circ\text{C}$
- TYPICAL HYSTERESIS :  $0.7\text{V}$  at  $V_{CC} = 3.3\text{V}$
- LOW NOISE:  
 $V_{OLP} = 0.3\text{V}$  (TYP.) at  $V_{CC} = 3.3\text{V}$
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 4\text{mA}$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}(\text{OPR}) = 2\text{V}$  to  $3.6\text{V}$  ( $1.2\text{V}$  Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 132
- IMPROVED LATCH-UP IMMUNITY
- POWER DOWN PROTECTION ON INPUTS



### ORDER CODES

PACKAGE	TUBE	T & R
SOP	74LVX132M	74LVX132MTR
TSSOP		74LVX132TTR

This device can be used to interface 5V to 3V system. It combines high speed performance with the true CMOS low power consumption.

Pin configuration and function are the same as those of the 74LVX00 but the 74LVX132 has hysteresis.

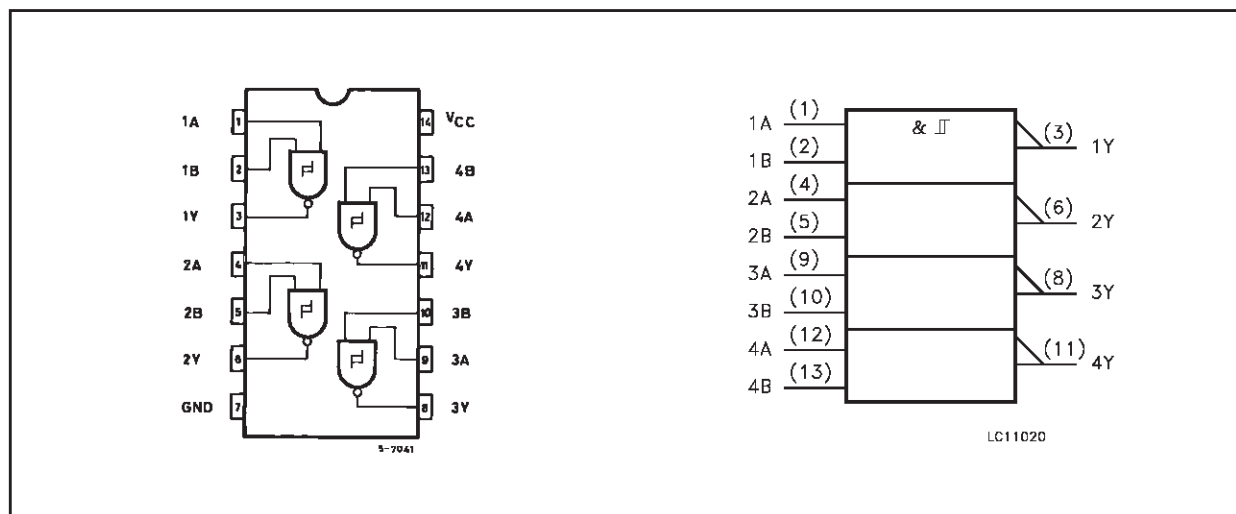
This together with its schmitt trigger function allows it to be used on line receivers with slow rise/fall input signals.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

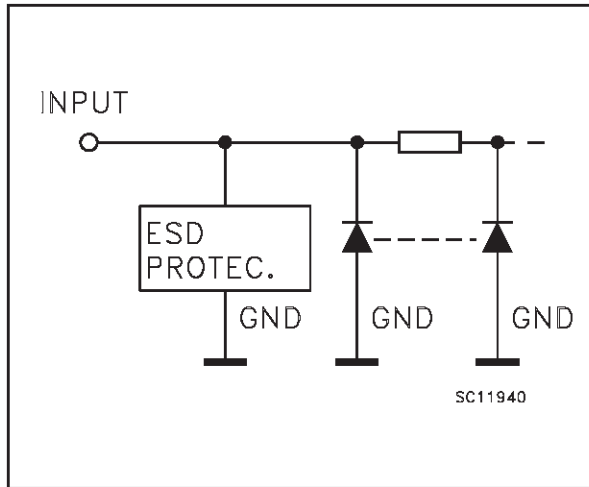
### DESCRIPTION

The 74LVX132 is a low voltage CMOS QUAD 2-INPUT SCHMITT NAND GATE fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. It is ideal for low power, battery operated and low noise 3.3V applications. Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



**INPUT EQUIVALENT CIRCUIT**



**PIN DESCRIPTION**

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V <sub>CC</sub>	Positive Supply Voltage

**TRUTH TABLE**

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7.0	V
V <sub>I</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>O</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	- 20	mA
I <sub>OK</sub>	DC Output Diode Current	± 20	mA
I <sub>O</sub>	DC Output Current	± 25	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	± 50	mA
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage (note 1)	2 to 3.6	V
V <sub>I</sub>	Input Voltage	0 to 5.5	V
V <sub>O</sub>	Output Voltage	0 to V <sub>CC</sub>	V
T <sub>op</sub>	Operating Temperature	-55 to 125	°C

1) Truth Table guaranteed: 1.2V to 3.6V

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>t+</sub>	High Level Input Threshold	3.0				2.2		2.2		2.2	V
V <sub>t-</sub>	Low Level Input Threshold	3.0		0.9				0.9		0.9	V
V <sub>H</sub>	Hysteresis Voltage	3.0		0.3		1.2	0.3	1.2	0.3	1.2	V
V <sub>OH</sub>	High Level Output Voltage	2.0	I <sub>O</sub> =-50 μA	1.9	2.0		1.9		1.9		V
		3.0	I <sub>O</sub> =-50 μA	2.9	3.0		2.9		2.9		
		3.0	I <sub>O</sub> =-4 mA	2.58			2.48		2.4		
V <sub>OL</sub>	Low Level Output Voltage	2.0	I <sub>O</sub> =50 μA		0.0	0.1		0.1		0.1	V
		3.0	I <sub>O</sub> =50 μA		0.0	0.1		0.1		0.1	
		3.0	I <sub>O</sub> =4 mA			0.36		0.44		0.55	
I <sub>I</sub>	Input Leakage Current	3.6	V <sub>I</sub> = 5V or GND			± 0.1		± 1		± 1	μA
I <sub>CC</sub>	Quiescent Supply Current	3.6	V <sub>I</sub> = V <sub>CC</sub> or GND			2		20		20	μA

## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>OLP</sub>	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C <sub>L</sub> = 50 pF		0.3	0.5					V
V <sub>OLV</sub>				-0.5	-0.3						
V <sub>IHD</sub>	Dynamic High Voltage Input (note 1, 3)	3.3		2.2							
V <sub>ILD</sub>	Dynamic Low Voltage Input (note 1, 3)	3.3				0.9					

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f=1MHz.

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r = t_f = 3\text{ns}$ )

Symbol	Parameter	Test Condition		Value								Unit
		$V_{CC}$ (V)	$C_L$ (pF)	$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time	2.7	15		7.5	10.5	1.0	12.0	1.0	12.0	ns	
		2.7	50		8.3	12.0	1.0	13.5	1.0	13.5		
		3.3 <sup>(*)</sup>	15		5.9	8.0	1.0	9.0	1.0	9.0		
		3.3 <sup>(*)</sup>	50		6.5	9.0	1.0	10.0	1.0	10.0		
$t_{OSLH}$ $t_{OSHL}$	Output To Output Skew Time (note 1, 2)	2.7	50		0.5	1.0		1.5		1.5	ns	
		3.3 <sup>(*)</sup>	50		0.5	1.0		1.5		1.5		

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW

2) Parameter guaranteed by design

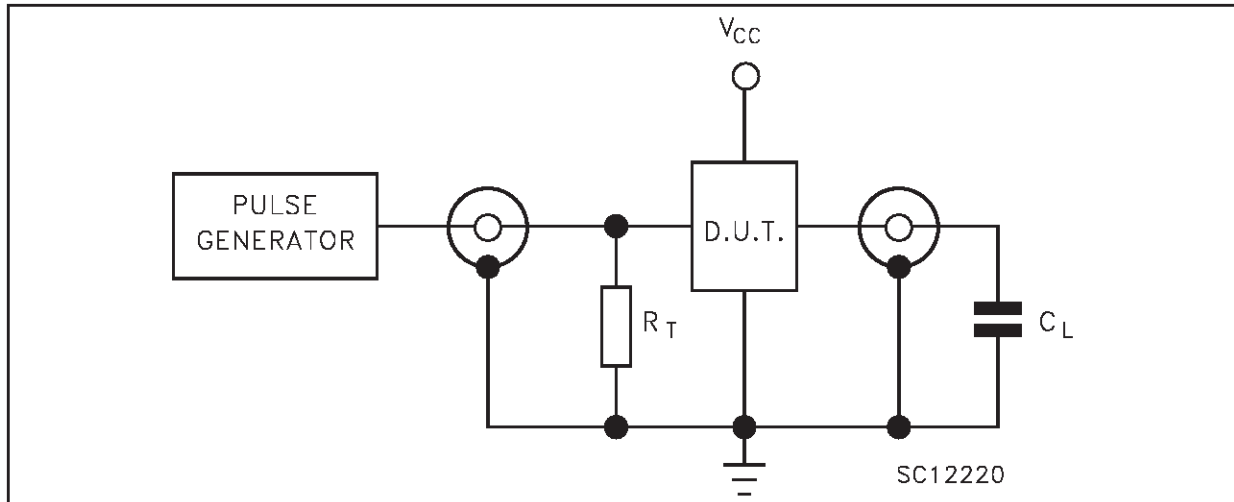
(\*) Voltage range is  $3.3\text{V} \pm 0.3\text{V}$

**CAPACITIVE CHARACTERISTICS**

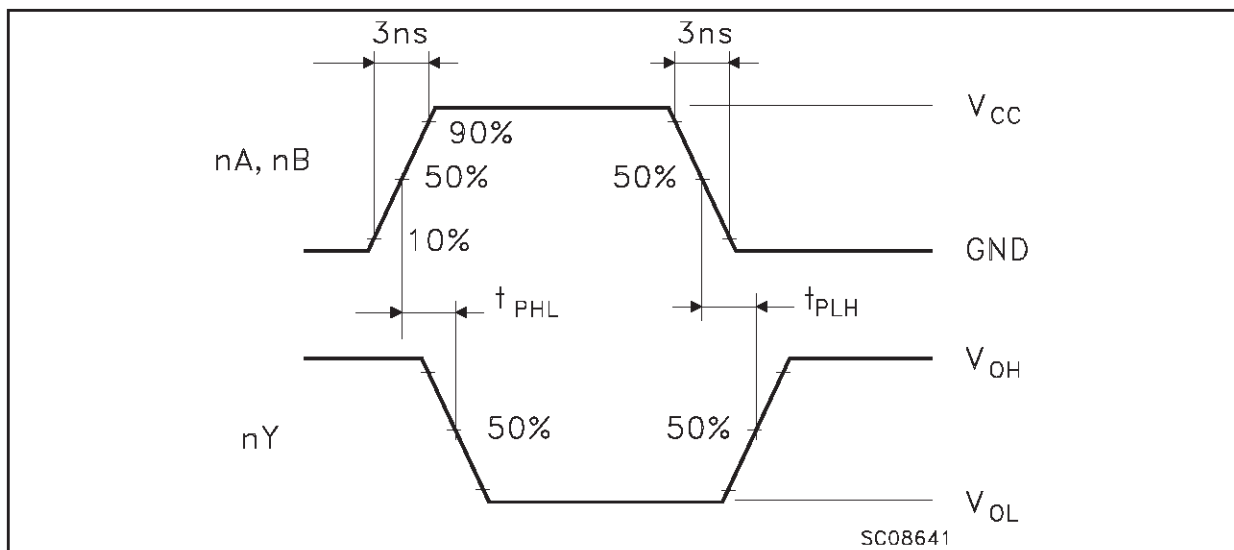
Symbol	Parameter	Test Condition		Value								Unit
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
$C_{IN}$	Input Capacitance	3.3			6	10		10		10	pF	
$C_{PD}$	Power Dissipation Capacitance (note 1)	3.3			16						pF	

1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$  (per gate)

## TEST CIRCUIT

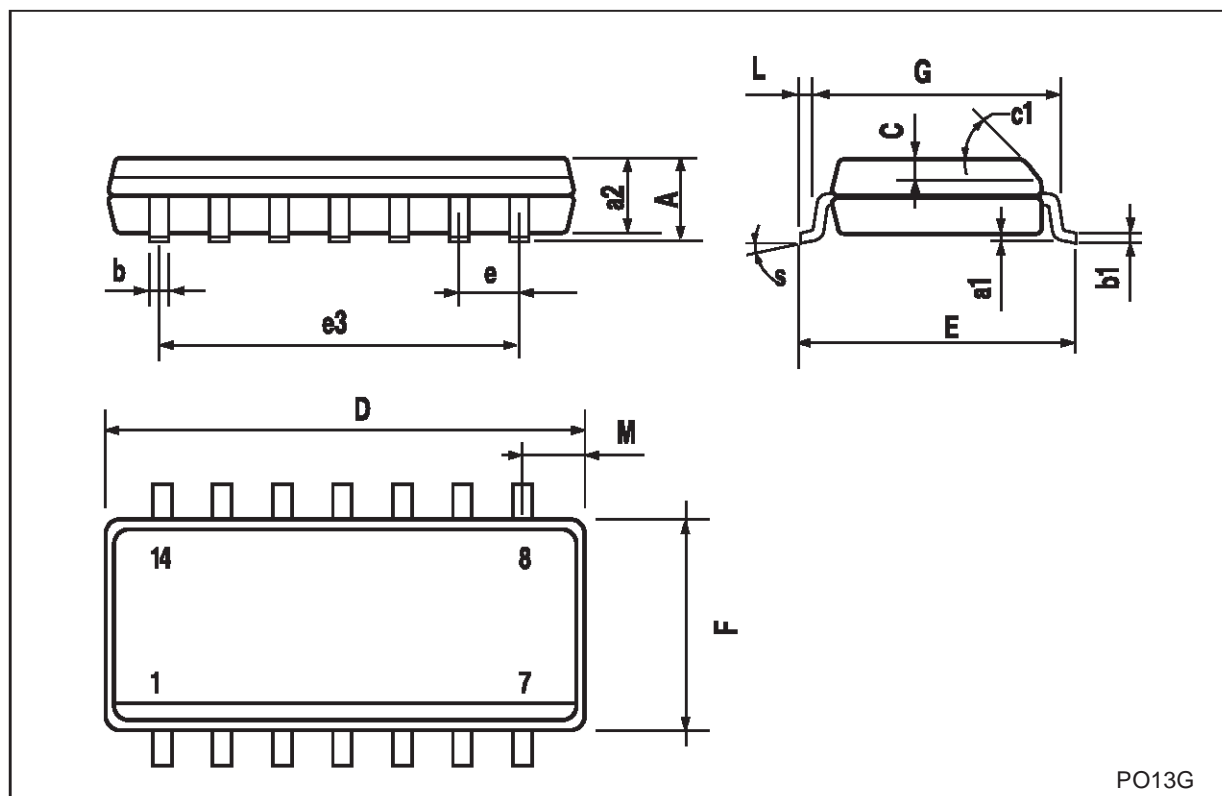


$C_L = 15/50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

WAVEFORM : PROPAGATION DELAYS ( $f=1\text{MHz}$ ; 50% duty cycle)

## SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G

## TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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