FAIRCHILD SEMICONDUCTOR™

November 1988
Revised August 2000

74AC821 • 74ACT821
10-Bit D-Type Flip-Flop with 3-STATE Outputs

General Description

The AC/ACT821 is a 10-bit D-type flip-flop with 3-STATE outputs arranged in a broadside pinout.

Features

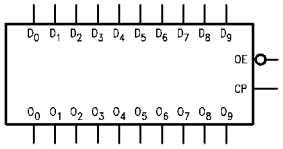
- 3-STATE outputs for bus interfacing
- Noninverting outputs
- Outputs source/sink 24 mA
- TTL compatible inputs

Ordering Code:

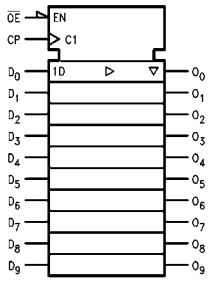
Order Number	Package Number	Package Description
74AC821SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74AC821SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74ACT821SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACT821MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT821SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code. (SPC not available in Tape and Reel.)

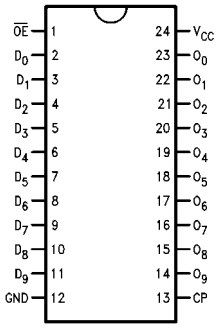
Logic Symbols



IEEE/IEC



Connection Diagram



Pin Descriptions

Pin Names	Description
D_0–D_9	Data Inputs
O_0–O_9	Data Outputs
$\overline{OE}$	Output Enable Input
CP	Clock Input

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Functional Description

The AC/ACT821 consists of ten D-type edge-triggered flip-flops. The buffered Clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition.

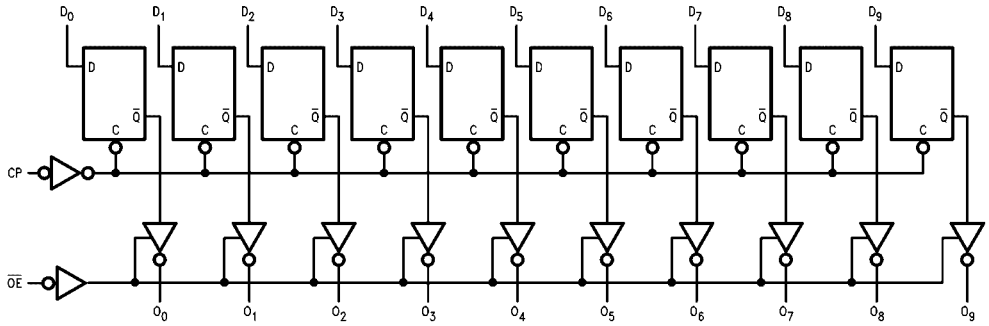
With $\overline{OE}$ LOW the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	⌐	L	L	Z	High Z
H	⌐	H	H	Z	High Z
L	⌐	L	L	L	Load
L	⌐	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	− 0.5V to + 7.0V
DC Input Diode Current (I_{IK})	
V_I = − 0.5V	− 20 mA
V_I = V_{CC} + 0.5V	+ 20 mA
DC Input Voltage (V_I)	− 0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	− 20 mA
V_O = V_{CC} + 0.5V	+ 20 mA
DC Output Voltage (V_O)	− 0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	− 65°C to + 150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	− 40°C to + 85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = − 50 µA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.46	V	I_{OH} = − 12 mA
		4.5		3.86	3.76		I_{OH} = − 24 mA
		5.5		4.86	4.76		I_{OH} = − 24 mA (Note 2)
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 µA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.44	V	I_{OL} = 12 mA
		4.5		0.36	0.44		I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	µA	V_I = V_{CC}, GND
I_{OZ}	Maximum 3-STATE Current	5.5		±0.5	±5.0	µA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		8.0	80.0	µA	V_{IN} = V_{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum LOW Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum HIGH Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	$I_{OUT} = -50\ \mu A$
		4.5 5.5		3.86 4.86	3.76 4.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 5)
V_{OL}	Maximum LOW Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	$I_{OUT} = 50\ \mu A$
		4.5 5.5		0.36 0.36	0.44 0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 5)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum 3-STATE Current	5.5		±0.5	±5.0	μA	$V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic Output Current (Note 6)	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V) (Note 7)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	3.3 5.0	110 120	145 160		100 110		MHz
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0	3.0 2.0	8.0 6.0	13.0 9.5	3.0 2.0	15.0 10.5	ns
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0	3.0 2.0	8.0 5.5	13.0 9.5	3.0 2.0	15.0 10.5	ns
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0	2.5 1.5	6.0 4.5	11.0 8.0	2.5 1.5	12.0 9.0	ns
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0	2.5 1.5	6.5 5.0	11.0 8.0	2.5 1.5	12.0 9.0	ns
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0	2.5 1.5	6.5 5.0	10.5 8.0	2.5 1.5	11.0 8.5	ns
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0	2.5 1.5	6.0 4.5	10.5 8.0	2.5 1.5	11.0 8.5	ns

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for AC

Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW D_n to CP	3.3	−1.0	1.5	1.5	ns
		5.0	−1.0	1.5	1.5	
t_H	Hold Time, HIGH or LOW D_n to CP	3.3	−1.0	3.5	4.0	ns
		5.0	−1.0	3.5	4.0	
t_W	CP Pulse Width HIGH or LOW	3.3	3.5	5.0	5.5	ns
		5.0	2.5	4.0	4.0	

Note 8: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V) (Note 9)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	5.0	120	150		110		MHz
t_{PLH}	Propagation Delay CP to O_n	5.0	2.0	6.0	9.5	1.5	10.5	ns
t_{PHL}	Propagation Delay CP to O_n	5.0	2.5	6.0	9.5	2.0	10.5	ns
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.5	7.0	10.5	2.0	11.5	ns
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.5	7.0	10.5	2.0	12.0	ns
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	7.5	12.0	1.0	13.0	ns
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	7.0	10.5	1.0	11.5	ns

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for ACT

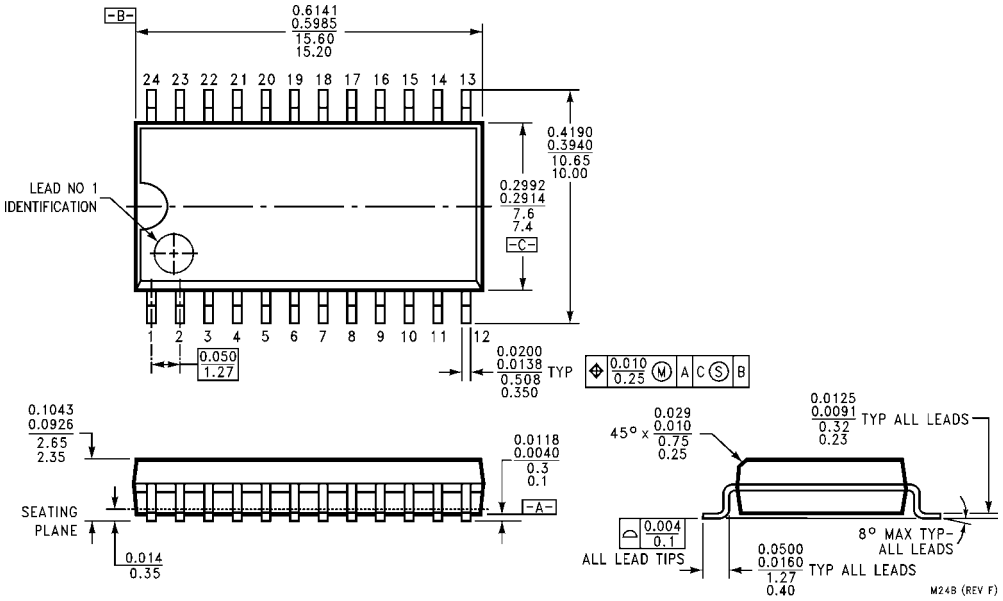
Symbol	Parameter	V_{CC} (V) (Note 10)	$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW D_n to CP	5.0	2.5	2.0	2.5	ns
t_H	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	2.0	2.5	ns
t_W	CP Pulse Width HIGH or LOW	5.0	3.0	4.5	5.5	ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

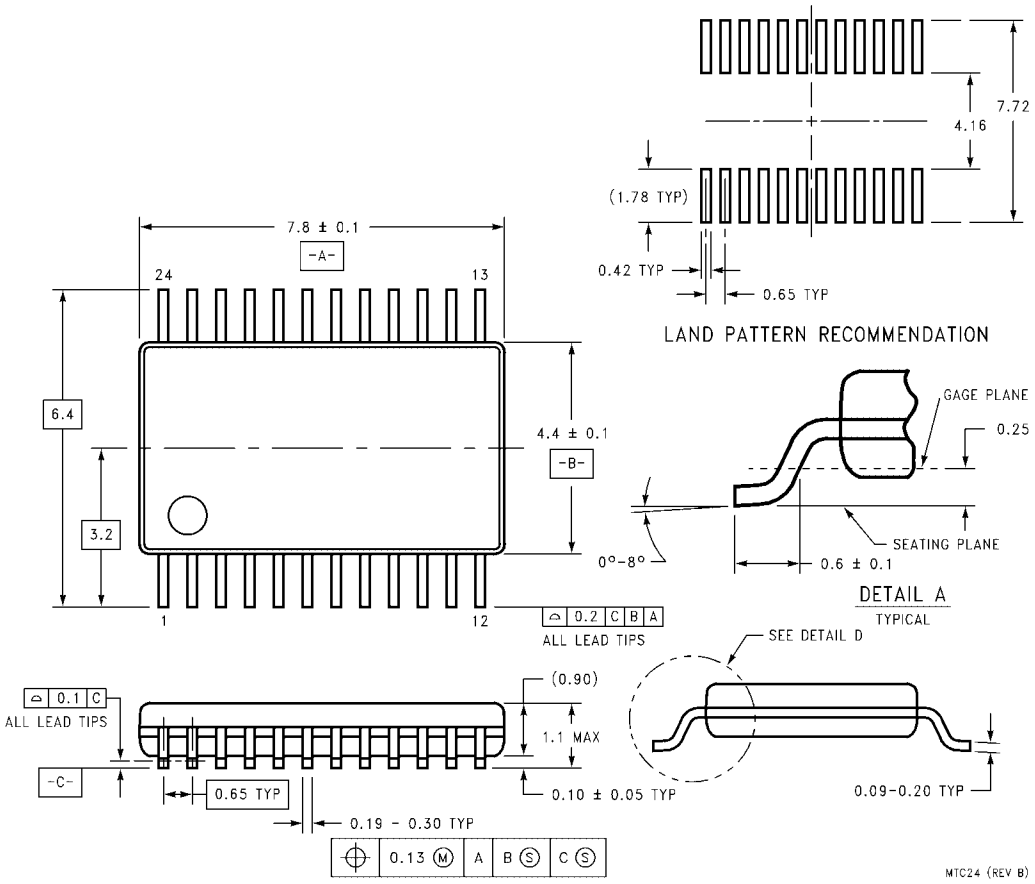
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	35.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



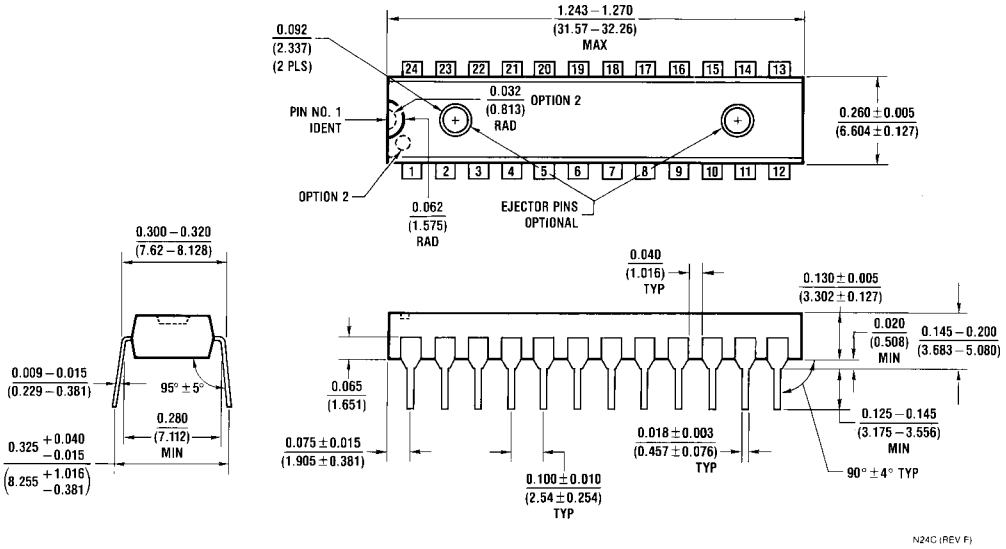
24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N24C

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