

## CD4021BC 8-Stage Static Shift Register

### General Description

The CD4021BC is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual JAM inputs to each of 8 stages. Q outputs are available from the sixth, seventh, and eighth stages. All outputs have equal source and sink current capabilities and conform to standard "B" series output drive.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control is in the logical "1" state, data is jammed into each stage of the register asynchronously with the clock.

All inputs are protected against static discharge with diodes to  $V_{DD}$  and  $V_{SS}$ .

### Features

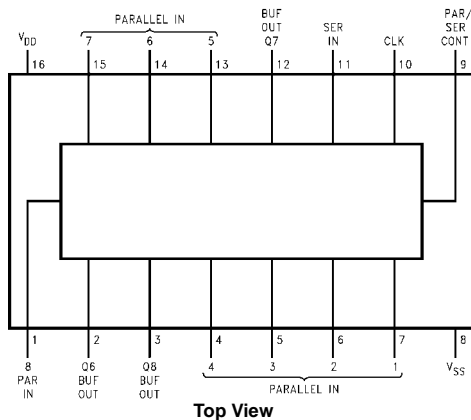
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45  $V_{DD}$  (typ.)
- Low power TTL compatibility:
  - Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1  $\mu$ A at 15V over full temperature range

### Ordering Code:

Order Number	Order Code	Package Description
CD4021BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4021BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



### Truth Table

$C_L$ (Note 1)	Serial Input	Parallel/ Serial Control	PI 1	PI n	Q1 (Internal)	$Q_n$ (Note 2)
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
↗	0	0	X	X	0	$Q_{n-1}$
↘	1	0	X	X	1	$Q_{n-1}$
↔	X	0	X	X	$Q_1$	$Q_n$

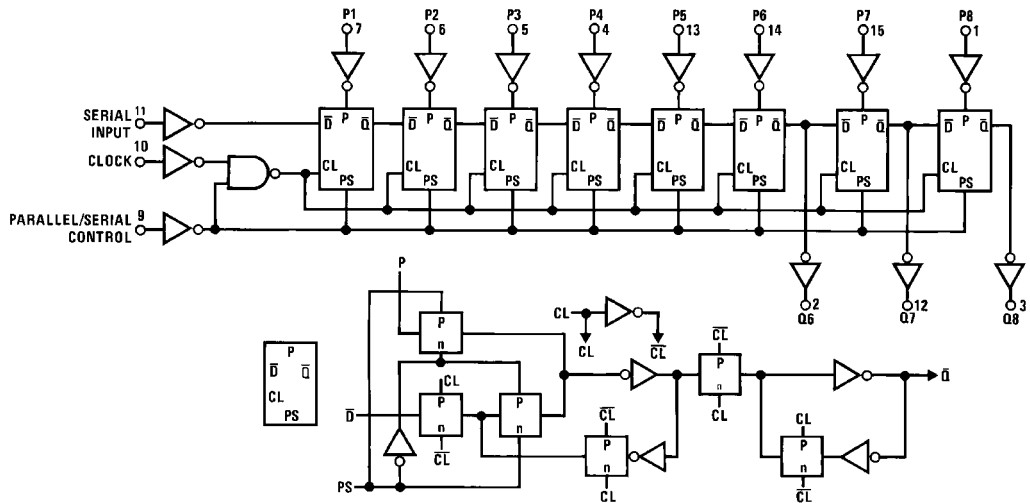
X = Don't care case

Note 1: Level change

Note 2: No change

CD4021BC

### Logic Diagram



**Absolute Maximum Ratings**(Note 3)

(Note 4)

Supply Voltage ( $V_{DD}$ )	-0.5V to +18V
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{DD} + 0.5V$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

**Recommended Operating Conditions** (Note 4)

Supply Voltage ( $V_{DD}$ )	3V to 15V
Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$
Operating Temperature Range ( $T_A$ )	
CD4021BCN	-55°C to +125°C

**Note 3:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 4:**  $V_{SS} = 0V$  unless otherwise specified.

**DC Electrical Characteristics** (Note 4)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$		5		0.1	5		150	$\mu A$
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$		10		0.2	10		300	
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		20		0.3	20		600	
$V_{OL}$	LOW Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ $ I_O  < 1 \mu A$		0.05		0	0.05		0.05	
		$V_{DD} = 15V$		0.05		0	0.05		0.05	
$V_{OH}$	HIGH Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$ $ I_O  < 1 \mu A$	9.95		9.95	10		9.95		
		$V_{DD} = 15V$	14.95		14.95	15		14.95		
$V_{IL}$	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0		4	3.0		3.0	
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0		6	4.0		4.0	
$V_{IH}$	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0	6		7.0		
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0	9		11.0		
$I_{OL}$	LOW Level Output Current (Note 5)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.2		0.90		
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8		2.4		
$I_{OH}$	HIGH Level Output Current (Note 5)	$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3	-2.2		-0.90		
		$V_{DD} = 15V, V_O = 13.5V$	-4.2		-3.4	-8		-2.4		
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		$-10^{-5}$	-0.1		-1.0	$\mu A$
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		$10^{-5}$	0.1		1.0	

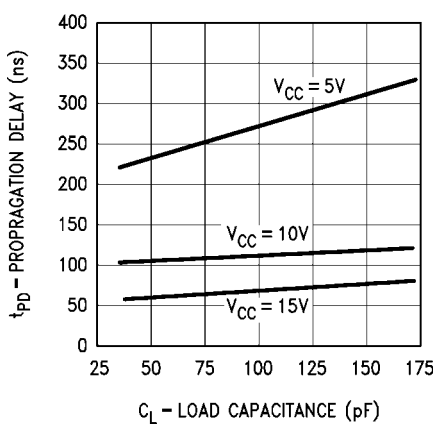
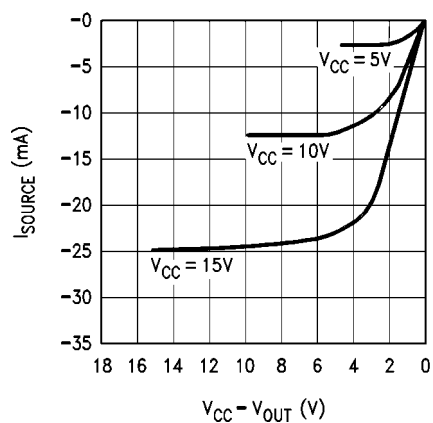
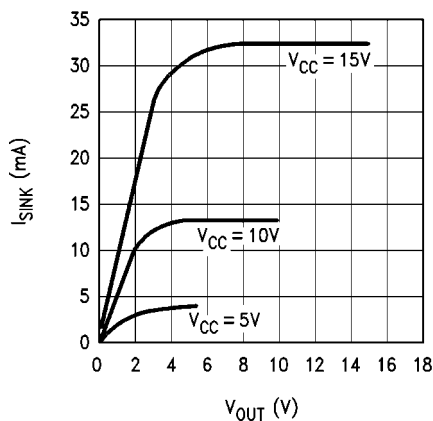
**Note 5:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

**AC Electrical Characteristics** (Note 6) $T_A = 25^\circ\text{C}$ , input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$ 

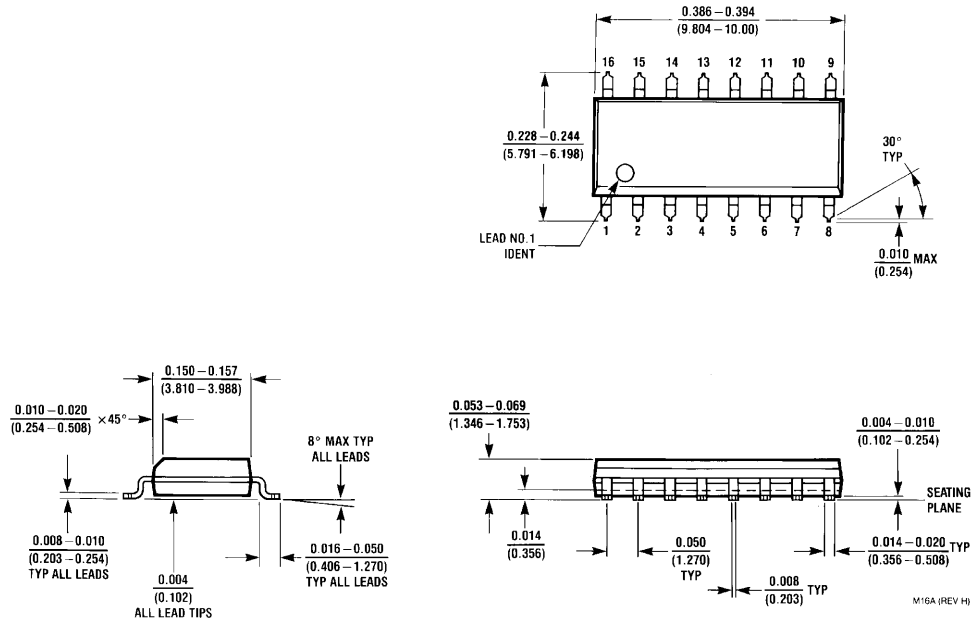
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH}, t_{PHL}$	Propagation Delay Time	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		240 100 70	350 175 140	ns
$t_{THL}, t_{TLH}$	Transition Time	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		100 50 40	200 100 80	ns
$f_{CL}$	Maximum Clock Input Frequency	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$	2.5 5 8	3.5 10 16		MHz
$t_W$	Minimum Clock Pulse Width	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		100 50 40	200 100 80	ns
$t_{rCL}, t_{fCL}$	Clock Rise and Fall Time (Note 6)	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$			15 15 15	$\mu\text{s}$
$t_s$	Minimum Set-Up Time					
	Serial Input $t_H \geq 200\text{ ns}$ (Ref. to CL)	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		60 40 30	120 80 60	ns
	Parallel Inputs $t_H \geq 200\text{ ns}$ (Ref. to P/S)	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		25 15 10	50 30 20	ns
$t_H$	Minimum Hold Time	$V_{DD} = 5V$			0	
	Serial In, Parallel In, $t_s \geq 400\text{ ns}$	$V_{DD} = 10V$			10	ns
	Parallel/Serial Control	$V_{DD} = 15V$			15	
$t_{WH}$	Minimum P/S Pulse Width	$V_{DD} = 5V$		150	250	
		$V_{DD} = 10V$		75	125	ns
		$V_{DD} = 15V$		50	100	
$t_{REM}$	Minimum P/S Removal Time (Ref. to CL)	$V_{DD} = 5V$		100	200	
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	
$C_I$	Average Input Capacitance	Any Input		5	7.5	pF
$C_{PD}$	Power Dissipation Capacitance (Note 8)			100		pF

**Note 6:** AC Parameters are guaranteed by DC correlated testing.**Note 7:** If more than one unit is cascaded  $t_{rCL}$  should be made less than or equal to the fixed propagation delay of the output of the driving stage for the estimated capacitive load.**Note 8:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation, see 74C family characteristics application note AN-90.

Typical Performance Characteristics

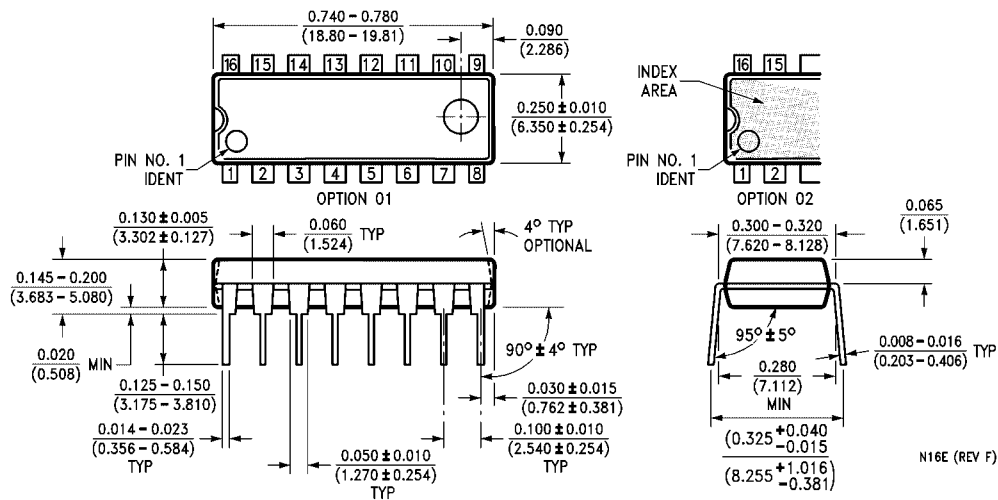


**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N16E**

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