

Integrated Device Technology, Inc.

# FAST CMOS OCTAL TRANSPARENT LATCHES

IDT54/74FCT373/A/C  
IDT54/74FCT533/A/C  
IDT54/74FCT573/A/C

## FEATURES

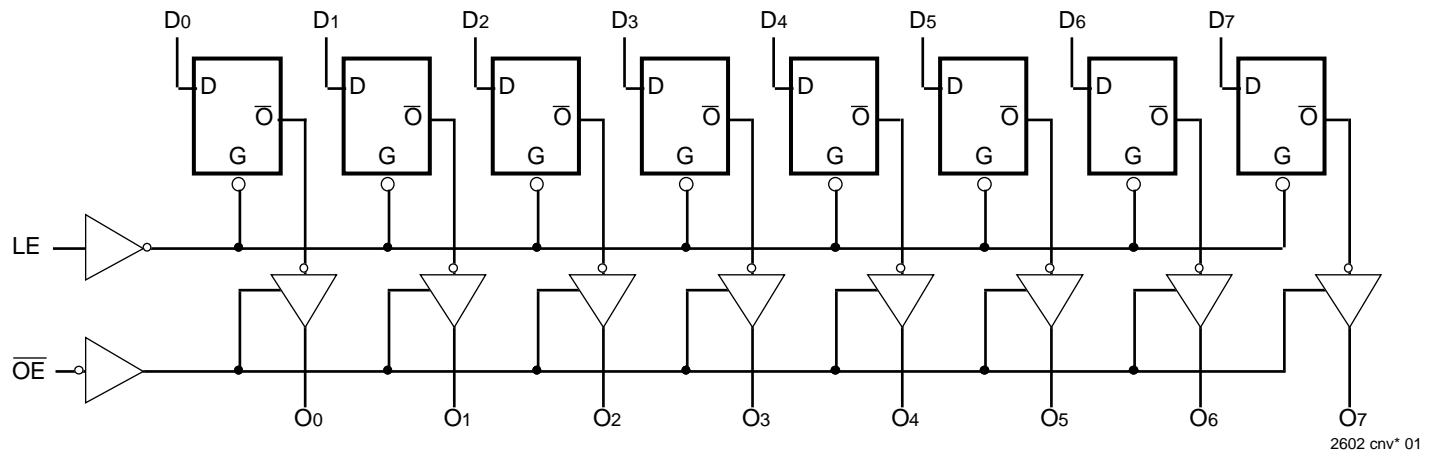
- IDT54/74FCT373/533/573 equivalent to FAST™ speed and drive
- **IDT54/74FCT373A/533A/573A up to 30% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Octal transparent latch with 3-state output control
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION

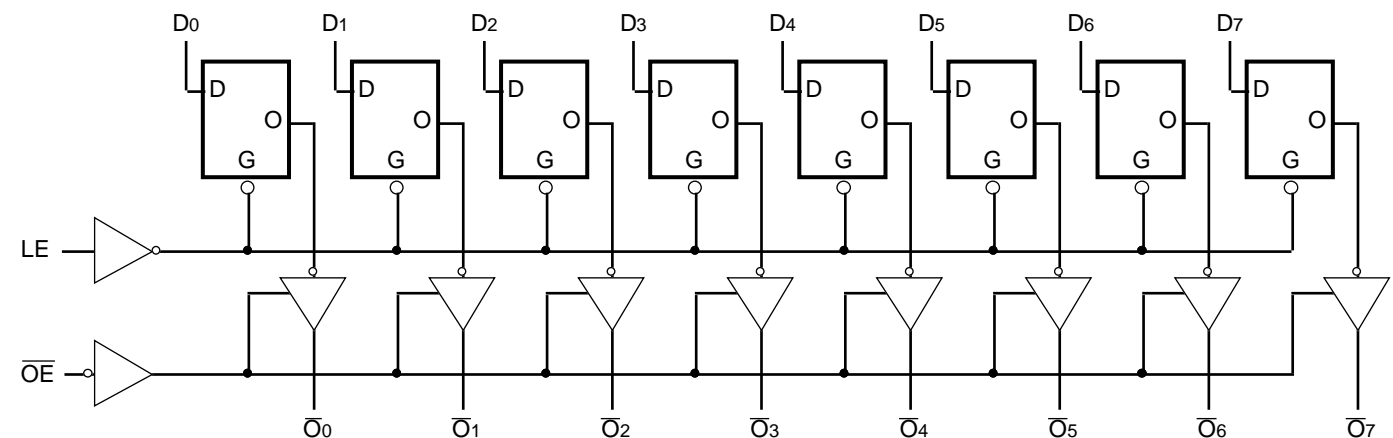
The IDT54/74FCT373/A/C, IDT54/74FCT533/A/C and IDT54/74FCT573/A/C are octal transparent latches built using an advanced dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH, the bus output is in the high-impedance state.

## FUNCTIONAL BLOCK DIAGRAMS

### IDT54/74FCT373 AND IDT54/74FCT573



### IDT54/74FCT533



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FAST is a trademark of National Semiconductor Co.

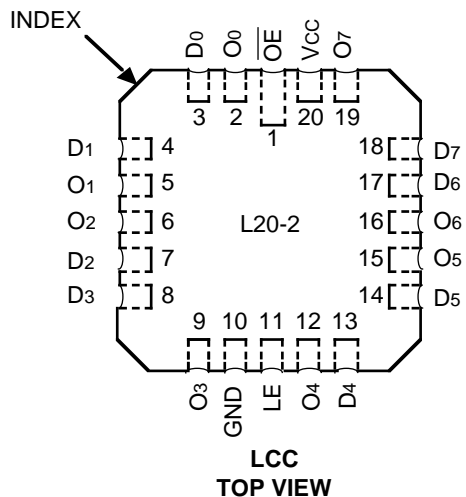
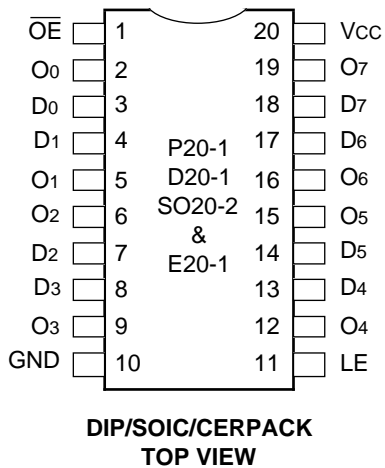
2602 cnv\* 02

MILITARY AND COMMERCIAL TEMPERATURE RANGES

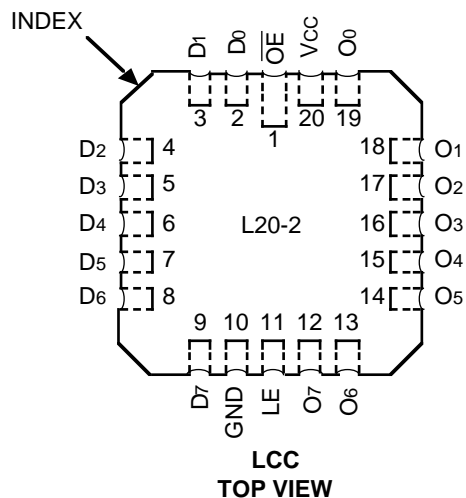
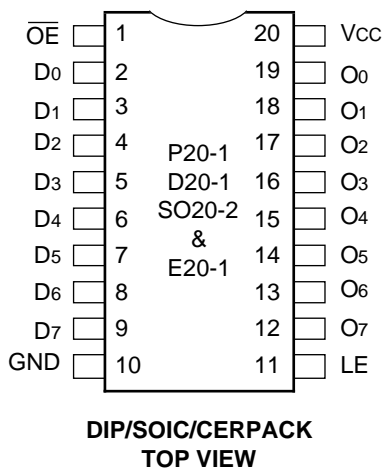
MAY 1992

## PIN CONFIGURATIONS

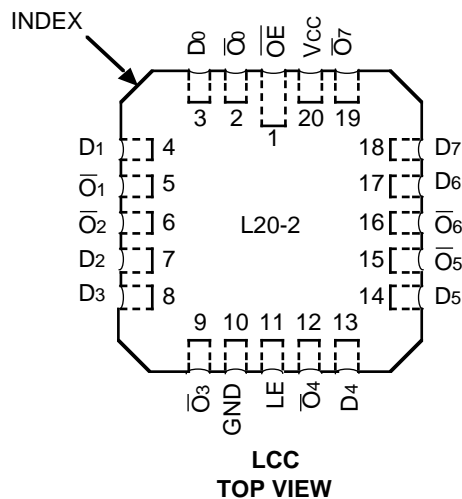
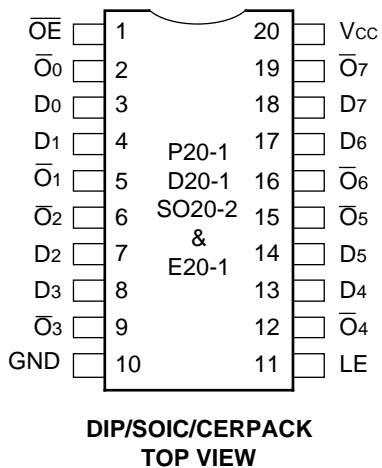
### IDT54/74FCT373



### IDT54/74FCT573



### IDT54/74FCT533



**FUNCTION TABLE (FCT533)<sup>(1)</sup>**

Inputs			Outputs
DN	LE	$\overline{OE}$	$\overline{ON}$
H	H	L	L
L	H	L	H
X	X	H	Z

**NOTE:** 2602 tbl 05  
 1. H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 Z = High Impedance

**FUNCTION TABLE (FCT373 and FCT573)<sup>(1)</sup>**

Inputs			Outputs
DN	LE	$\overline{OE}$	ON
H	H	L	H
L	H	L	L
X	X	H	Z

**NOTE:** 2602 tbl 06  
 1. H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 Z = High Impedance

**PIN DESCRIPTION**

Pin Names	Description
DN	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
ON	3-State Outputs
$\overline{ON}$	Complementary 3-State Outputs

2602 tbl 07

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub>	-0.5 to V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	0.5	W
I <sub>OUT</sub>	DC Output Current	120	120	mA

**NOTES:** 2602 tbl 01  
 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.  
 2. Input and V<sub>CC</sub> terminals only.  
 3. Outputs and I/O terminals only.

**CAPACITANCE** (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

**NOTE:** 2602 tbl 02  
 1. This parameter is measured at characterization but not tested.

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:  $V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

Commercial:  $T_A = 0^\circ C$  to  $+70^\circ C$ ,  $V_{CC} = 5.0V \pm 5\%$ ; Military:  $T_A = -55^\circ C$  to  $+125^\circ C$ ,  $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	5	$\mu A$
$I_{IL}$	Input LOW Current		$V_i = 2.7V$	—	—	5 <sup>(4)</sup>	
			$V_i = 0.5V$	—	—	-5 <sup>(4)</sup>	
			$V_i = GND$	—	—	-5	
$I_{OZH}$	Off State (High Impedance) Output Current	$V_{CC} = \text{Max.}$	$V_o = V_{CC}$	—	—	10	$\mu A$
$I_{OZL}$			$V_o = 2.7V$	—	—	10 <sup>(4)</sup>	
			$V_o = 0.5V$	—	—	-10 <sup>(4)</sup>	
			$V_o = GND$	—	—	-10	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_o = GND$		-60	-120	—	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$		$V_{HC}$	$V_{CC}$	—	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -300\mu A$	$V_{HC}$	$V_{CC}$	—	
			$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3	—	
			$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$		—	GND	$V_{LC}$	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 300\mu A$	—	GND	$V_{LC}^{(4)}$	
			$I_{OL} = 32mA \text{ MIL.}$	—	0.3	0.5	
			$I_{OL} = 48mA \text{ COM'L.}$	—	0.3	0.5	

**NOTES:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ C$  ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

2602 tbl 03

## POWER SUPPLY CHARACTERISTICS

V<sub>LC</sub> = 0.2V; V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max. V <sub>IN</sub> ≥ V <sub>HC</sub> ; V <sub>IN</sub> ≤ V <sub>LC</sub>		—	0.2	1.5	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub>	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V <sub>CC</sub> One Bit Toggling	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	1.7	4.0	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	2.0	5.0	
		V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V <sub>CC</sub> Eight Bits Toggling	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	3.2	6.5 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	5.2	14.5 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.

2602 tbl 04

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT373/A/C/FCT573/A/C**

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT373/573				FCT373A/573A				FCT373C/573C				Unit
			Com'l. <sup>(2)</sup>		Mil. <sup>(2)</sup>		Com'l. <sup>(2)</sup>		Mil. <sup>(2)</sup>		Com'l. <sup>(2)</sup>		Mil. <sup>(2)</sup>		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	1.5	4.2	1.5	5.1	ns
tPLH tPHL	Propagation Delay LE to ON		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	2.0	5.5	2.0	8.0	ns
tPZH tPZL	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
tPHZ tPLZ	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
tsu	Set-up Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

2602 tbl 08

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT533/A/C**

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT533				FCT533A				FCT533C				Unit
			Com'l. <sup>(2)</sup>		Mil. <sup>(2)</sup>		Com'l. <sup>(2)</sup>		Mil. <sup>(2)</sup>		Com'l. <sup>(2)</sup>		Mil. <sup>(2)</sup>		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	10.0	1.5	12.0	1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1	ns
tPLH tPHL	Propagation Delay LE to ON		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.8	2.0	6.9	2.0	8.0	ns
tPZH tPZL	Output Enable Time		1.5	11.0	1.5	12.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
tPHZ tPLZ	Output Disable Time		1.5	7.0	1.5	8.5	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
tsu	Set-up Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

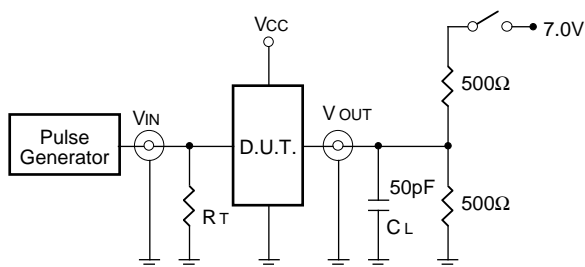
**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2602 tbl 09

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

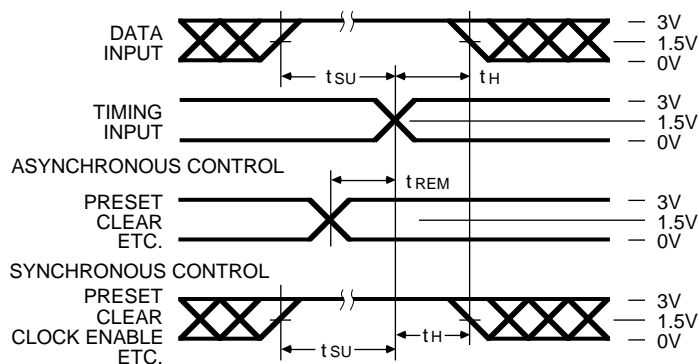
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

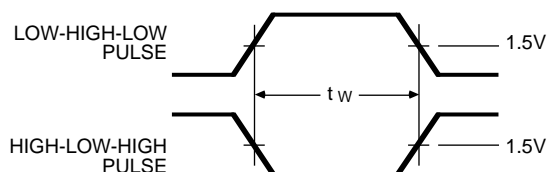
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

2537 tbl 10

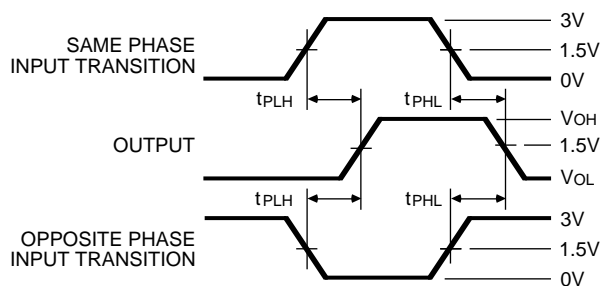
### SET-UP, HOLD AND RELEASE TIMES



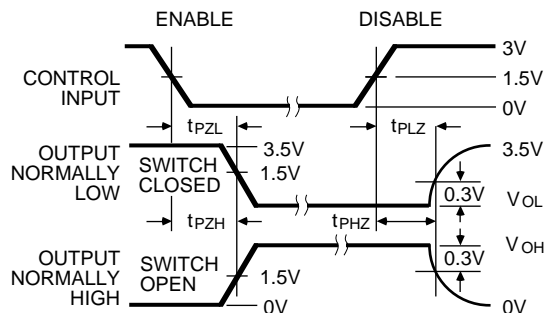
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES



#### NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0$  MHz;  $Z_o \leq 50\Omega$ ;  $t_f \leq 2.5$  ns;  $t_r \leq 2.5$  ns.

2537 drw 04

**ORDERING INFORMATION**

IDT	XX	FCT	XXXX	X	X	
Temp. Range			Device Type	Package	Process	
						Blank
						B Commercial MIL-STD-883, Class B
						P Plastic DIP
						D CERDIP
						SO Small Outline IC
						L Leadless Chip Carrier
						E CERPACK
						373 Non-Inverting Octal Transparent Latch
						573 Non-Inverting Octal Transparent Latch
						533 Inverting Octal Transparent Latch
						373A Fast Non-Inverting Octal Transparent Latch
						573A Fast Non-Inverting Octal Transparent Latch
						533A Fast Inverting Octal Transparent Latch
						373C Super Fast Non-Inverting Octal Transparent Latch
						573C Super Fast Non-Inverting Octal Transparent Latch
						533C Super Fast Inverting Octal Transparent Latch
						54 -55°C to +125°C
						74 0°C to +70°C

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