July 2005

LM118JAN
Operational Amplifier

General Description

The LM118 is a precision high speed operational amplifier designed for applications requiring wide bandwidth and high slew rate. It features a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed forward compensation will boost the slew rate to over 150V/µs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 µs.

The high speed and fast settling time of this op amp makes it useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. This device is easy to apply and offers an order of magnitude better AC performance than industry standards such as the LM709.

Features

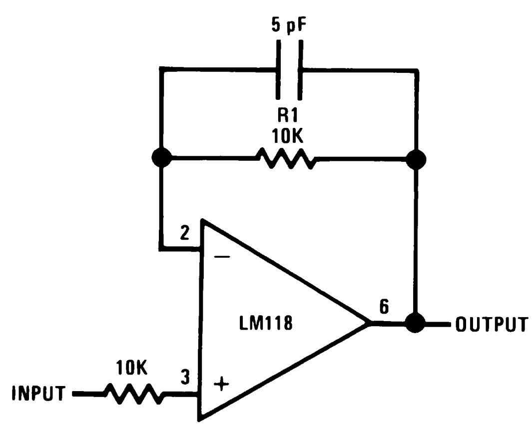
- 15 MHz small signal bandwidth
- Guaranteed 50V/µs slew rate
- Maximum bias current of 250 nA
- Operates from supplies of ±5V to ±20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

Ordering Information

NS Part Number	JAN Part Number	NS Package Number	Package Description
JL118BGA	JM38510/10107BGA	H08C	8LD TO-99 Metal Can
JL118BPA	JM38510/10107BPA	J08A	8LD CERDIP
JL118BCA	JM38510/10107BCA	J14A	14LD CERDIP
JL118BHA	JM38510/10107BHA	W10A	10LD CERPACK
JL118SGA	JM38510/10107SGA	H08C	8LD TO-99 Metal Can
JL118SPA	JM38510/10107SPA	J08A	8LD CERDIP
JL118SHA	JM38510/10107SHA	W10A	10LD CERPACK

Fast Voltage Follower

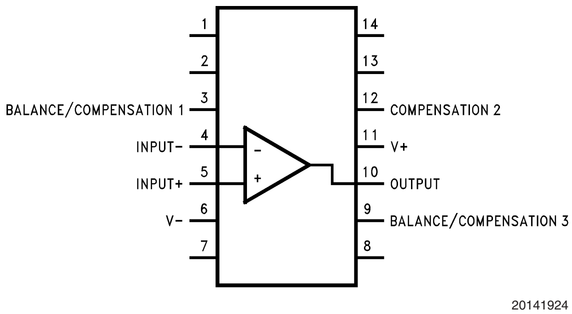
(Note 1)



Note 1: Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

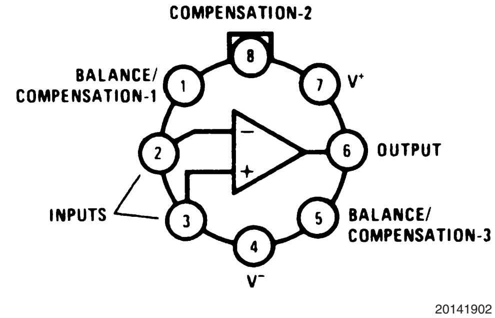
Connection Diagram

Dual-In-Line Package



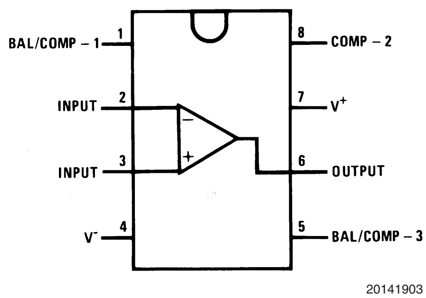
Top View
See NS Package Number J14A

Metal Can Package
(Note 2)



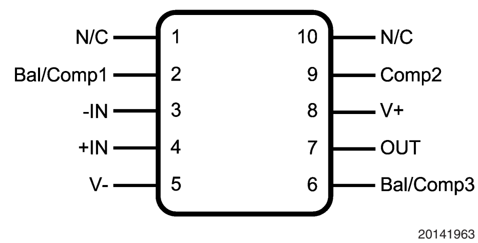
Top View
See NS Package Number H08C

Dual-In-Line Package



Top View
See NS Package Number J08A

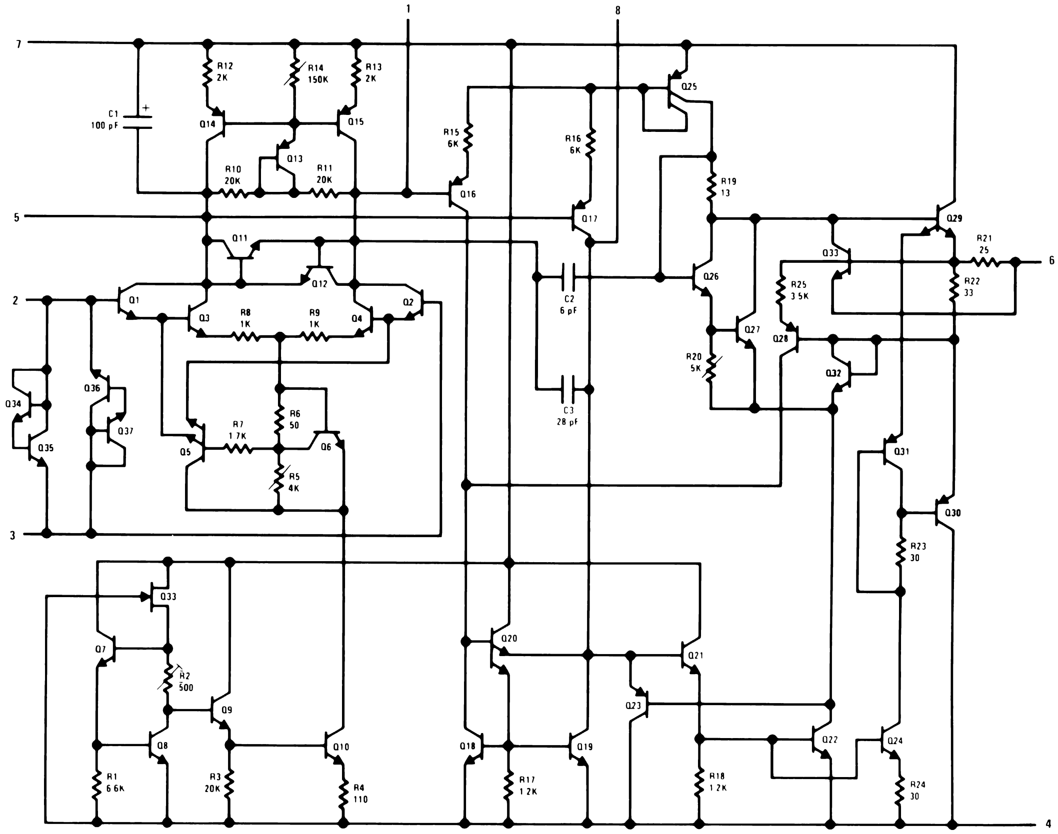
Ceramic Flatpack Package



Top View
See NS Package Number W10A

Note 2: Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Schematic Diagram



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Absolute Maximum Ratings (Note 3)

Supply Voltage	±20V
Power Dissipation (Note 4)	
8 LD Metal Can	750mW
8LD CERDIP	1000mW
14LD CERDIP	1250mW
10LD CERPACK	600mW
Differential Input Current (Note 5)	±10 mA
Input Voltage (Note 6)	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	−55˚C ≤ T_A ≤ +125˚C
Thermal Resistance	
θ_{JA}	
8 LD Metal Can (Still Air @ 0.5W)	160˚C/W
8 LD Metal Can (500LF / Min Air flow @ 0.5W)	86˚C/W
8LD CERDIP (Still Air @ 0.5W)	120˚C/W
8LD CERDIP (500LF / Min Air flow @ 0.5W)	66˚C/W
14LD CERDIP (Still Air @ 0.5W)	87˚C/W
14LD CERDIP (500LF / Min Air flow @ 0.5W)	51˚C/W
10LD CERPACK (Still Air @ 0.5W)	198˚C/W
10LD CERPACK (500LF / Min Air flow @ 0.5W)	124˚C/W
θ_{JC}	
8 LD Metal Can	48˚C/W
8LD CERDIP	17˚C/W
14LD CERDIP	17˚C/W
10LD CERPACK	22˚C/W
Storage Temperature Range	−65˚C ≤ T_A ≤ +150˚C
Lead Temperature (Soldering, 10 seconds)	300˚C
ESD Tolerance (Note 7)	2000V

Quality Conformance Inspection

Mil-Std-883, Method 5005; Group A

Subgroup	Description	Temp˚C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

LM118 JAN Electrical Characteristics

DC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

DC: V_{CC} = ±20V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V		-4.0	4.0	mV	1
				-6.0	6.0	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = 15V		-4.0	4.0	mV	1
				-6.0	6.0	mV	2, 3
		V_{CM} = 0V		-4.0	4.0	mV	1
				-6.0	6.0	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V		-4.0	4.0	mV	1
				-6.0	6.0	mV	2, 3
I_{IO}	Input Offset Current	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V, R_S = 100KΩ	(Note 11)	-40	40	nA	1
			(Note 11)	-80	80	nA	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = 15V, R_S = 100KΩ	(Note 11)	-40	40	nA	1
			(Note 11)	-80	80	nA	2, 3
		V_{CM} = 0V, R_S = 100KΩ	(Note 11)	-40	40	nA	1
			(Note 11)	-80	80	nA	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V, R_S = 100KΩ	(Note 11)	-40	40	nA	1
			(Note 11)	-80	80	nA	2, 3
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V, R_S = 100KΩ	(Note 11)	1.0	250	nA	1, 2
			(Note 11)	1.0	400	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = 15V, R_S = 100KΩ	(Note 11)	1.0	250	nA	1, 2
			(Note 11)	1.0	400	nA	3
		V_{CM} = 0V, R_S = 100KΩ	(Note 11)	1.0	250	nA	1, 2
			(Note 11)	1.0	400	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V, R_S = 100KΩ	(Note 11)	1.0	250	nA	1, 2
			(Note 11)	1.0	400	nA	3
+PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 10V, $-V_{CC}$ = -20V		-100	100	μV/V	1
				-150	150	μV/V	2, 3
-PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 20V, $-V_{CC}$ = -10V		-100	100	μV/V	1
				-150	150	μV/V	2, 3
CMRR	Common Mode Rejection Ratio	V_{CM} = ±15V, V_{CC} = ± 35V to ±5V		80		dB	1, 2, 3
$+V_{IO}$ adj.	Offset Null			7.0		mV	1, 2, 3
$-V_{IO}$ adj.	Offset Null				-7.0	mV	1, 2, 3
Delta V_{IO} / Delta T	Temperature Coefficient of Input Offset Voltage	25˚C ≤ T_A ≤ 125˚C	(Note 9)	-50	50	μV/˚C	2
		-55˚C ≤ T_A ≤ 25˚C	(Note 9)	-50	50	μV/˚C	3
Delta I_{IO} / Delta T	Temperature Coefficient of Input Offset Current	25˚C ≤ T_A ≤ 125˚C	(Note 9)	-1000	1000	pA/˚C	2
		-55˚C ≤ T_A ≤ 25˚C	(Note 9)	-1000	1000	pA/˚C	3
$+I_{OS}$	Short Circuit Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, t ≤ 25mS, V_{CM} = -15V		-65		mA	1, 2, 3
$-I_{OS}$	Short Circuit Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, t ≤ 25mS, V_{CM} = 15V			65	mA	1, 2
					80	mA	3
I_{CC}	Power Supply Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V			8.0	mA	1
					7.0	mA	2
					9.0	mA	3
$+V_{Opp}$	Output Voltage Swing	R_L = 10KΩ, V_{CM} = -20V		17		V	4, 5, 6
		R_L = 2KΩ, V_{CM} = -20V		16		V	4, 5, 6

LM118 JAN Electrical Characteristics (Continued)

DC Parameters (Continued)

The following conditions apply to all the following parameters, unless otherwise specified.

DC: V_{CC} = ±20V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$-V_{Opp}$	Output Voltage Swing	R_L = 10KΩ, V_{CM} = 20V			-17	V	4, 5, 6
		R_L = 2KΩ, V_{CM} = 20V			-16	V	4, 5, 6
$+A_{VS}$	Open Loop Voltage Gain	V_O = 15V, R_L = 2KΩ	(Note 8)	50		V/mV	4
			(Note 8)	32		V/mV	5, 6
		V_O = 15V, R_L = 10KΩ	(Note 8)	50		V/mV	4
			(Note 8)	32		V/mV	5, 6
$-A_{VS}$	Open Loop Voltage Gain	V_O = -15V, R_L = 2KΩ	(Note 8)	50		V/mV	4
			(Note 8)	32		V/mV	5, 6
		V_O = -15V, R_L = 10KΩ	(Note 8)	50		V/mV	4
			(Note 8)	32		V/mV	5, 6
A_{VS}	Open Loop Voltage Gain	$\pm V_{CC}$ = ±5V, V_O = ±2V, R_L = 2KΩ	(Note 8)	10		V/mV	4, 5, 6
		$\pm V_{CC}$ = ±5V, V_O = ±2V, R_L = 10KΩ	(Note 8)	10		V/mV	4, 5, 6

AC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

AC: V_{CC} = ±20V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
NI_{BB}	Noise Input Broadband	BW = 10Hz to 5KHz, R_S = 0Ω			25	μV_{RMS}	7
NI_{PC}	Noise Input Popcorn	BW = 10Hz to 5KHz, R_S = 20KΩ			80	μV_{PK}	7
TR_{tR}	Transient Response: Rise Time	V_I = 50mV, PRR = 1KHz			40	nS	7, 8A, 8B
TR_{OS}	Transient Response: Overshoot	V_I = 50mV, PRR = 1KHz			50	%	7, 8A, 8B
+SR	Slew Rate	A_V = 1, V_I = -5V to +5V		50		V/µS	7, 8B
				40		V/µS	8A
-SR	Slew Rate	A_V = 1, V_I = +5V to -5V		50		V/µS	7, 8B
				40		V/µS	8A
$+t_S$	Settling Time	V_I = -5V to +5V	(Note 10)		800	nS	12
			(Note 10)		1200	nS	13, 14
$-t_S$	Settling Time	V_I = +5V to -5V	(Note 10)		800	nS	12
			(Note 10)		1200	nS	13, 14

LM118 JAN Electrical Characteristics (Continued)

DC Drift Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

DC: V_{CC} = ±20V

Delta calculations performed on JAN S devices at group B, subgroup 5 only.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_{CM} = 0V		-1.0	1.0	mV	1
$\pm I_{IB}$	Input Bias Current	V_{CM} = 0V, R_S = 100KΩ		-25	25	nA	1

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 5: The inputs are shunted with back-to-back diodes for over voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 6: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 7: Human body model, 1.5 kΩ in series with 100 pF.

Note 8: Datalog in K = V/mV

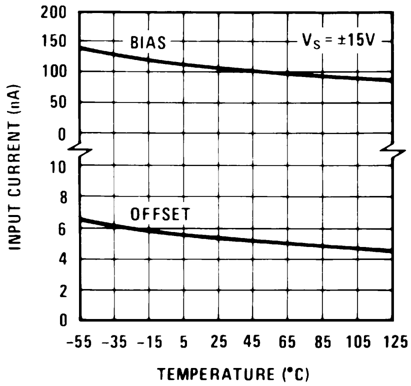
Note 9: Calculated parameter.

Note 10: Errorband = ±2%.

Note 11: Slash Sheet: R_S = 20KΩ, tested with R_S = 100KΩ for better resolution.

Typical Performance Characteristics

Input Current



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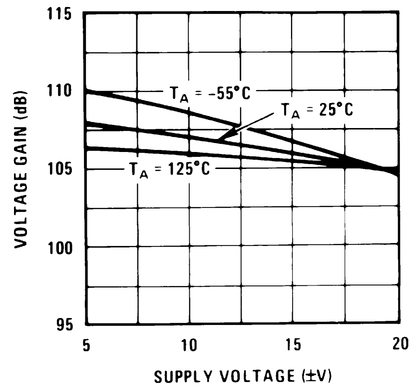
Voltage Gain



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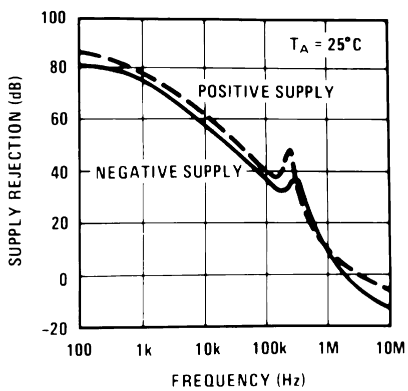
Power Supply Rejection



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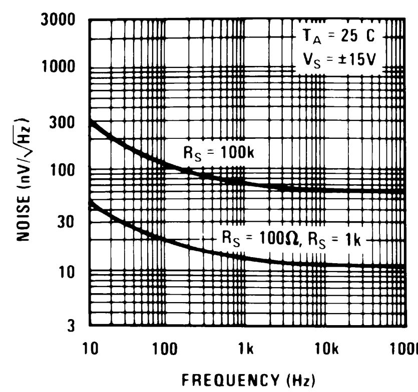
Input Noise Voltage



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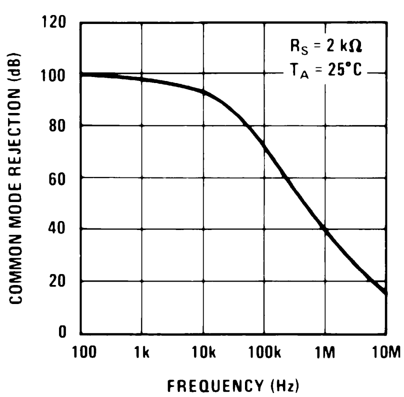
Common Mode Rejection



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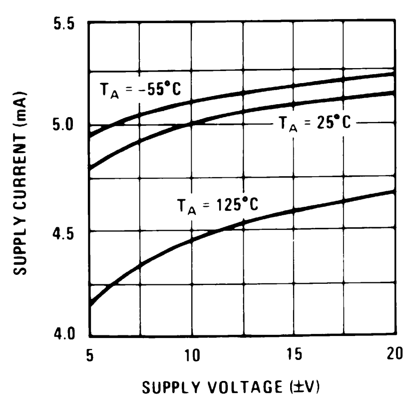
Supply Current



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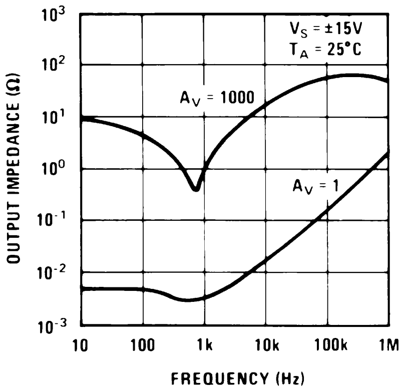
Typical Performance Characteristics (Continued)

Closed Loop Output Impedance



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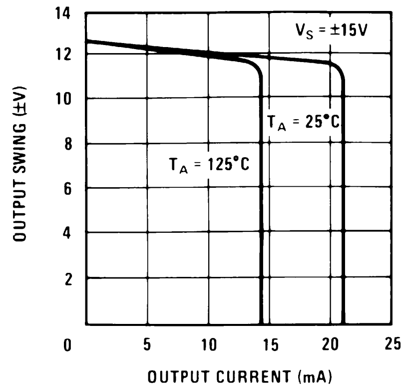
Current Limiting



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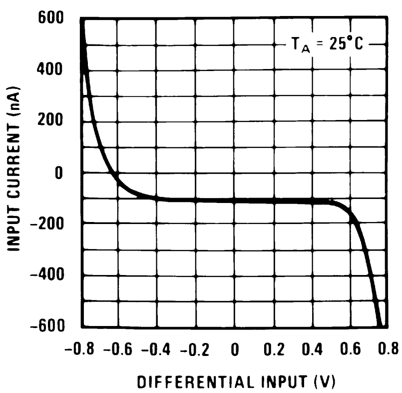
Input Current



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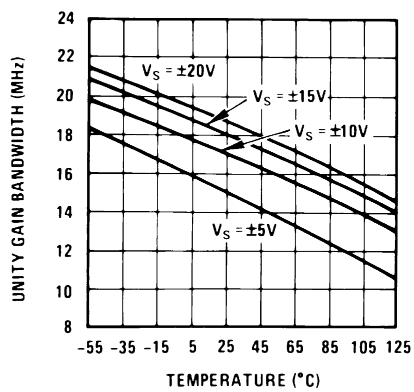
Unity Gain Bandwidth



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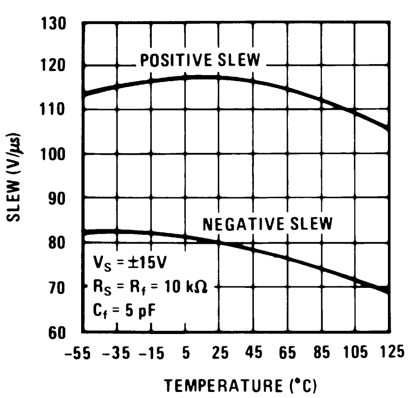
Voltage Follower Slew Rate



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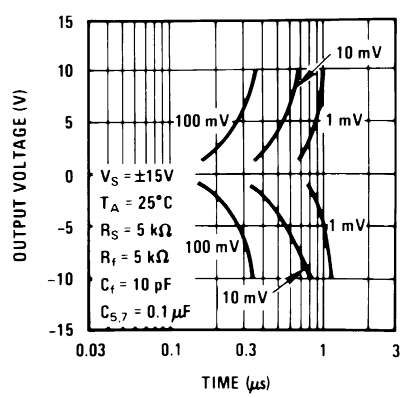
Inverter Settling Time



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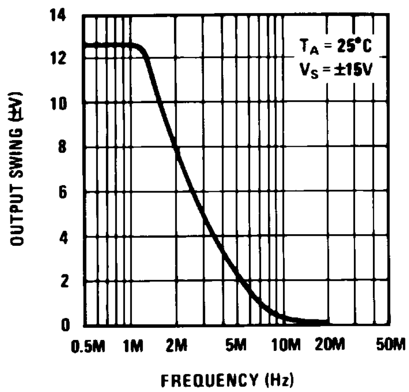
Typical Performance Characteristics (Continued)

Large Signal Frequency Response



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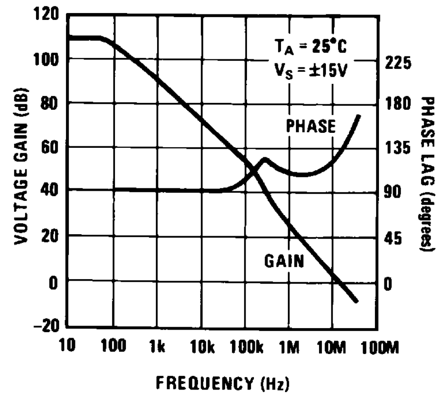
Open Loop Frequency Response



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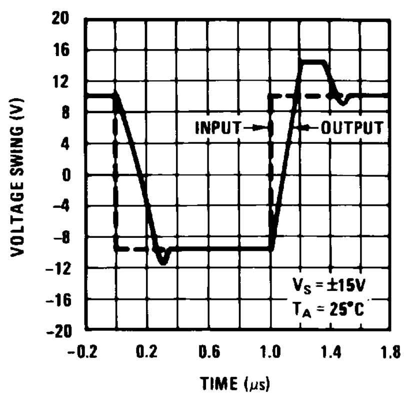
Voltage Follower Pulse Response



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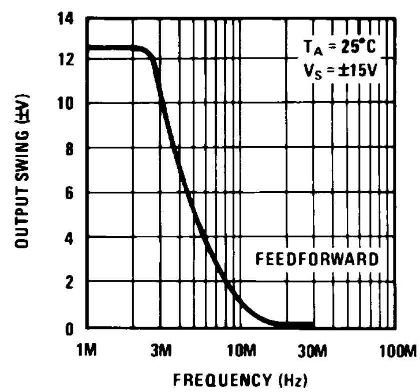
Large Signal Frequency Response



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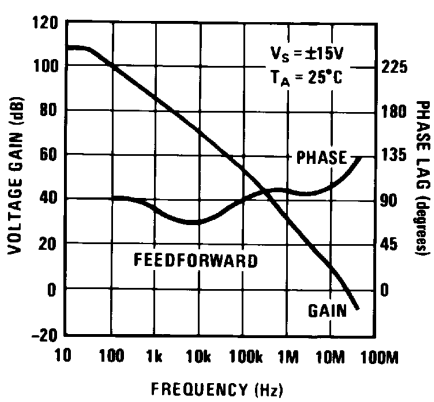
Open Loop Frequency Response



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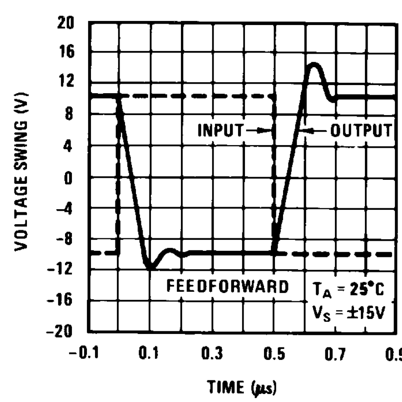
Inverter Pulse Response



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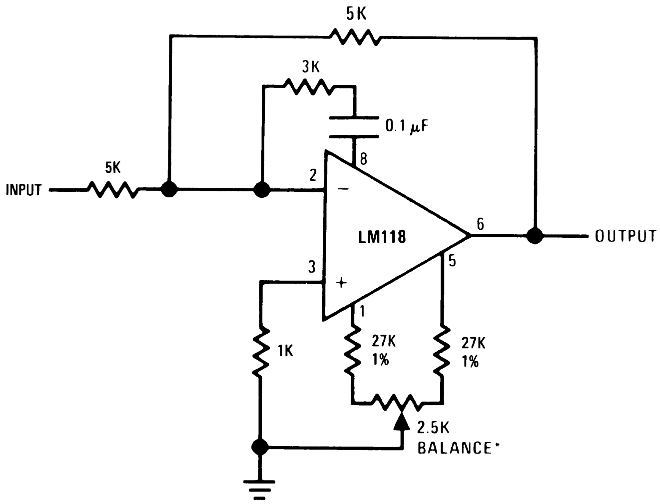
Auxiliary Circuits

Feedforward Compensation for Greater Inverting Slew Rate
(Note 12)



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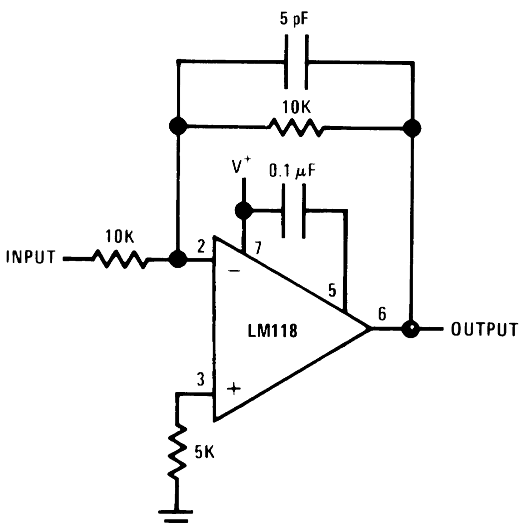
*Balance circuit necessary for increased slew.

Note 12: Slew rate typically 150V/μs.

Compensation for Minimum Settling Time
(Note 13)



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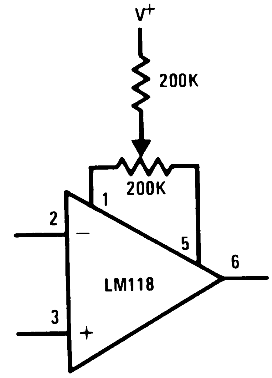
Note 13: Slew and settling time to 0.1% for a 10V step change is 800 ns.

Offset Balancing



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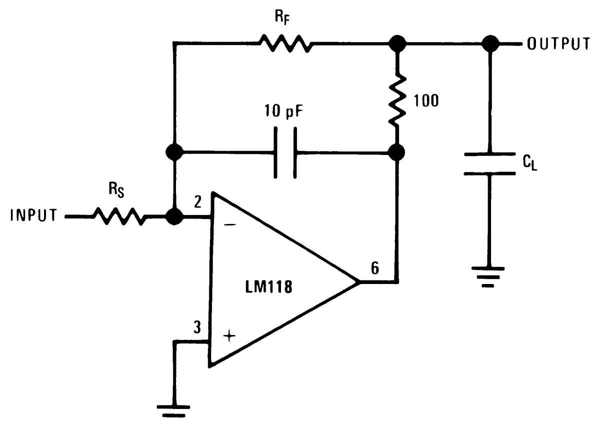
Isolating Large Capacitive Loads



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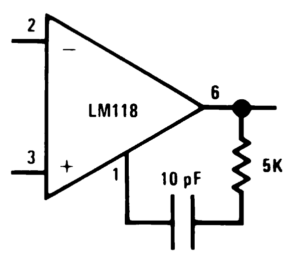
Overcompensation



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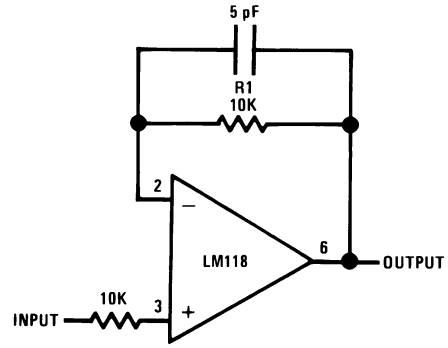
Typical Applications

Fast Voltage Follower
(Note 14)



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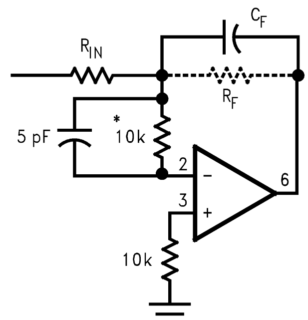
Integrator or Slow Inverter



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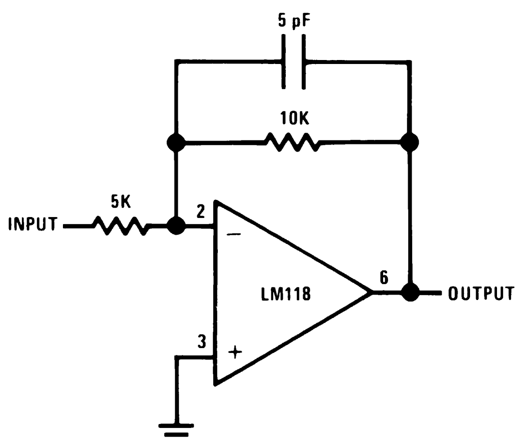
C_F = Large
($C_F \geq$ 50 pF)
*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

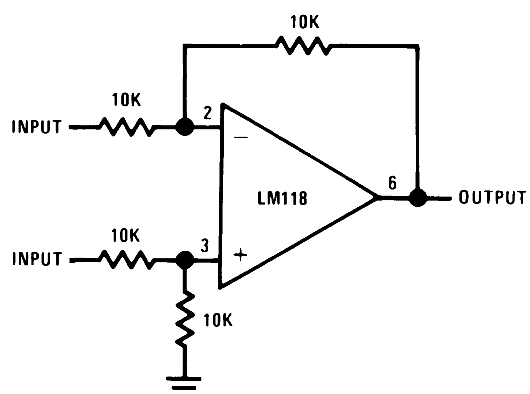
Note 14: Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

Fast Summing Amplifier



20141915

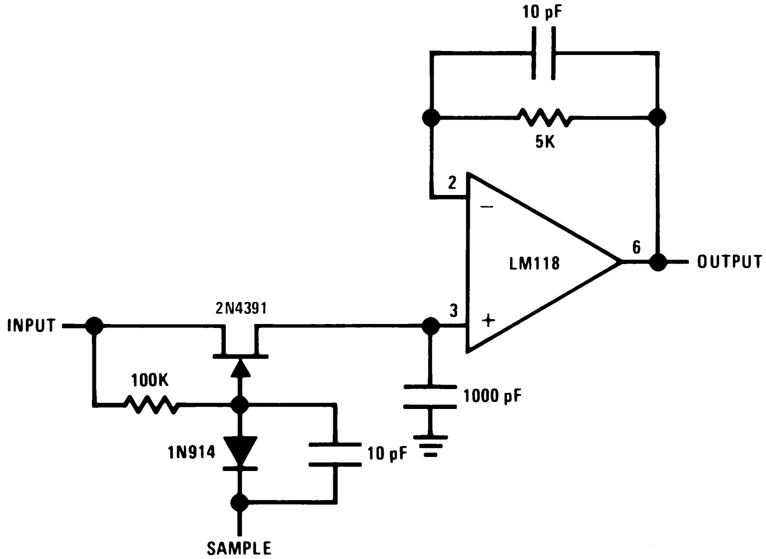
Differential Amplifier



20141916

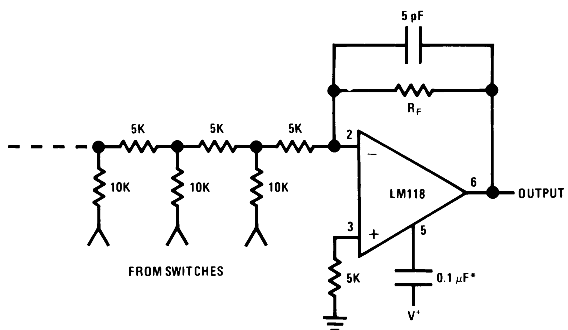
Typical Applications (Continued)

Fast Sample and Hold



20141918

D/A Converter Using Ladder Network

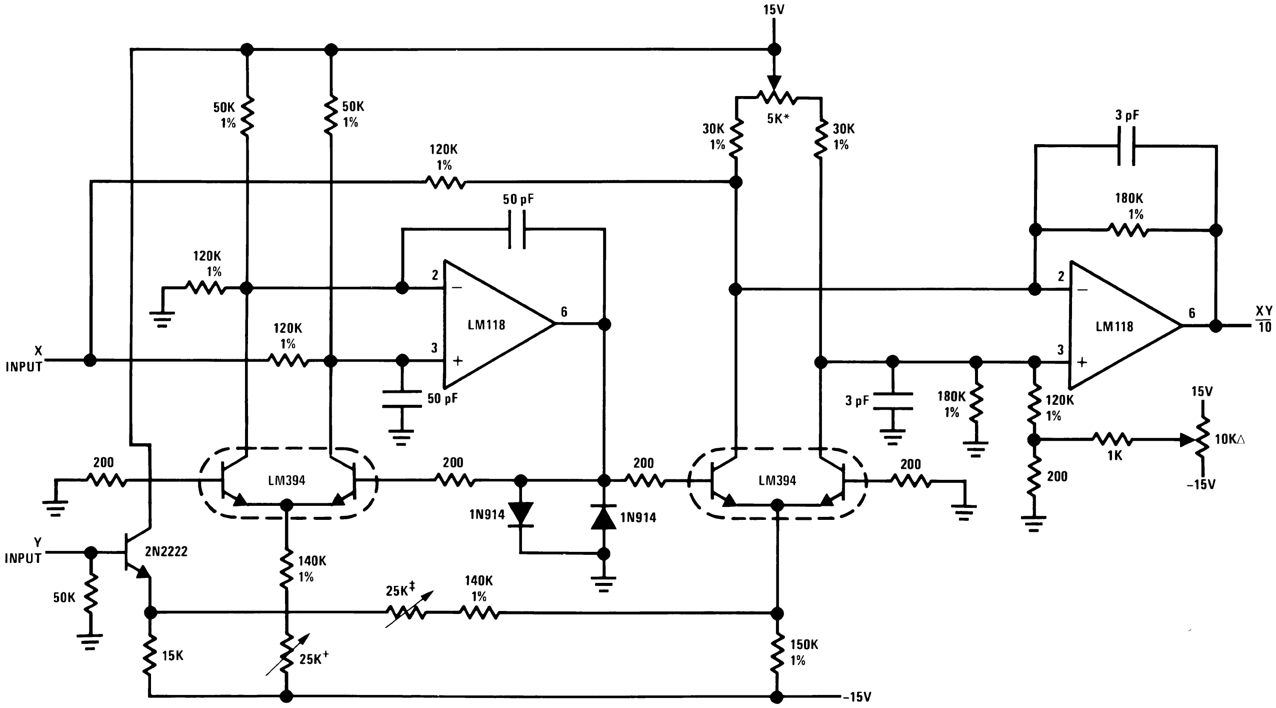


20141919

*Optional — Reduces settling time.

Typical Applications (Continued)

Four Quadrant Multiplier



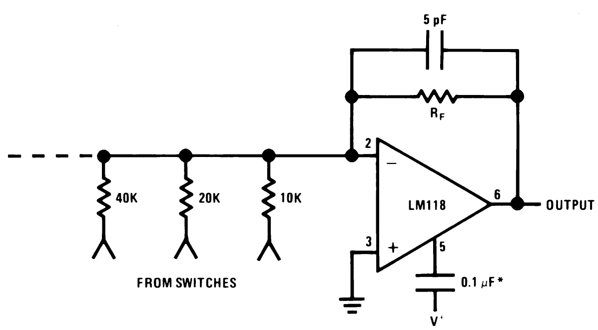
ΔOutput zero.

*"Y" zero

+"X" zero

‡Full scale adjust.

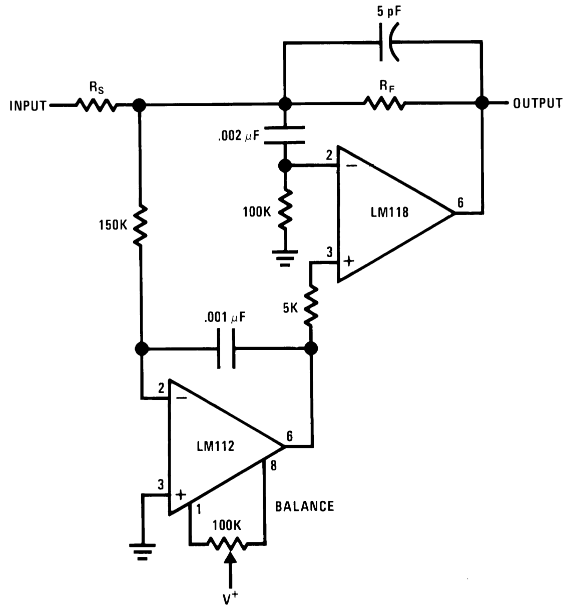
D/A Converter Using Binary Weighted Network



*Optional — Reduces settling time.

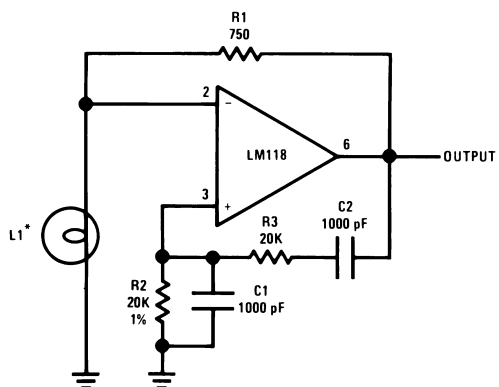
Typical Applications (Continued)

Fast Summing Amplifier with Low Input Current



20141921

Wein Bridge Sine Wave Oscillator



20141922

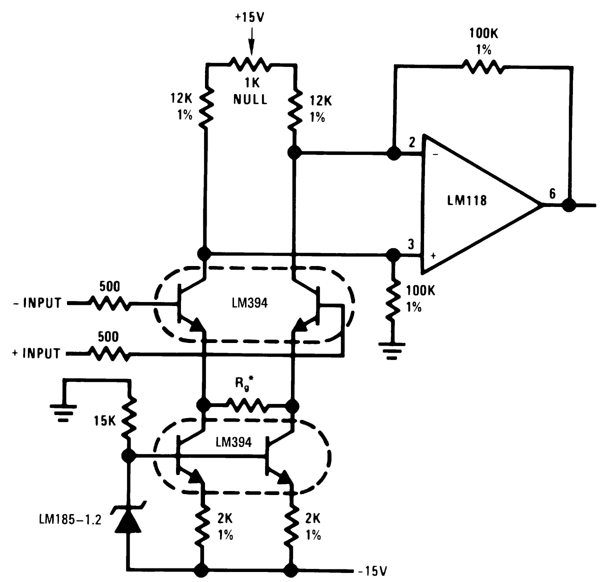
*L1—10V—14 mA bulb ELDEMA 1869

R1 = R2

C1 = C2

$$f = \frac{1}{2\pi R2\,C1}$$

Instrumentation Amplifier



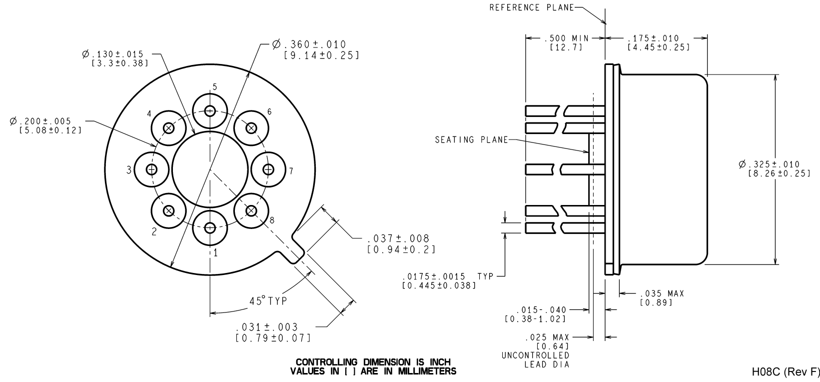
20141923

$$\text{*Gain} \geq \frac{200K}{R_g} \text{ for } 1.5K \leq R_g \leq 200K$$

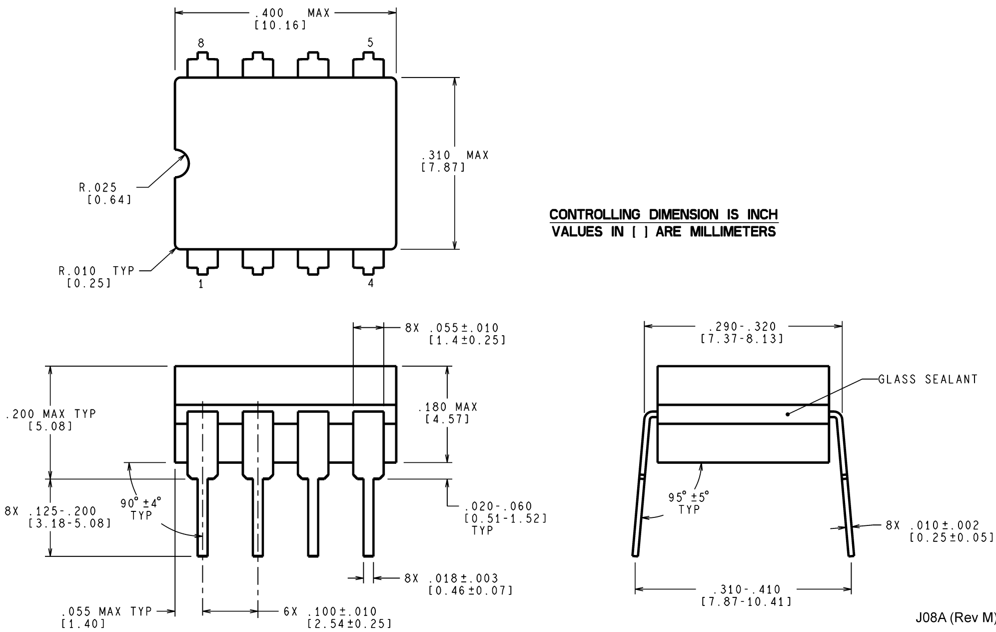
Revision History Section

Date Released	Revision	Section	Originator	Changes
07/12/05	A	New Release, Corporate format	L. Lytle	1 MDS data sheet, MJLM118–X Rev 0A0 was converted into the Corp. datasheet format. MDS datasheet will be archived.

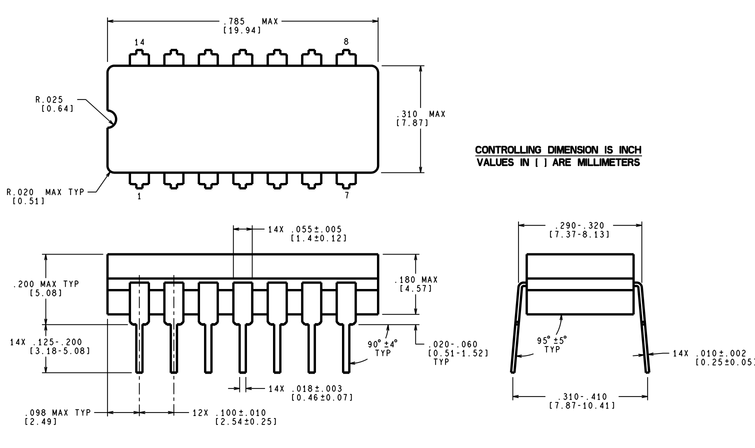
Physical Dimensions inches (millimeters) unless otherwise noted



Metal Can Package (H)
NS Package Number H08C

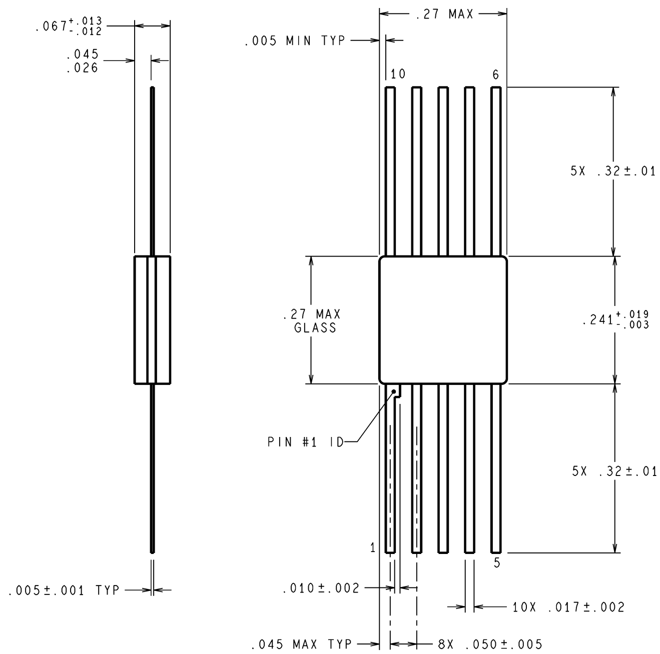


Ceramic Dual-In-Line Package (J)
NS Package Number J08A



Ceramic Dual-In-Line Package (J)
NS Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN INCHES

W10A (Rev H)

Ceramic SOIC (W)
NS Package Number W10A

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