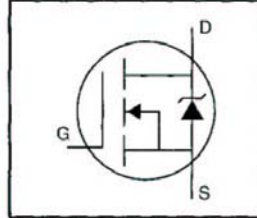


HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Isolated Central Mounting Hole
- 175°C Operating Temperature
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DSS} = 60V$$

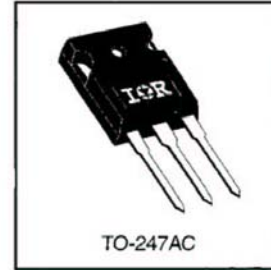
$$R_{DS(on)} = 0.018\Omega$$

$$I_D = 70^*A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.



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Absolute Maximum Ratings

	Parameter	Max.	Units	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	70*	A	
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	52		
I_{DM}	Pulsed Drain Current ①	290		
$P_D @ T_C = 25^\circ C$	Power Dissipation	190	W	
	Linear Derating Factor	1.3	W/°C	
V_{GS}	Gate-to-Source Voltage	±20	V	
E_{AS}	Single Pulse Avalanche Energy ②	200	mJ	
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns	
T_J	Operating Junction and Storage Temperature Range	-55 to +175	°C	
T_{STG}		Soldering Temperature, for 10 seconds		300 (1.6mm from case)
		Mounting Torque, 6-32 or M3 screw		10 lbf•in (1.1 N•m)

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.80	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	40	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	60	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _{(BR)DSS} /ΔT _J	—	0.060	—	V/°C	Reference to 25°C, I _D =1mA
R _{DS(on)}	—	—	0.018	Ω	V _{GS} =10V, I _D =44A ④
V _{GS(th)}	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	20	—	—	S	V _{DS} =25V, I _D =44A ④
I _{DSS}	—	—	25	μA	V _{DS} =60V, V _{GS} =0V
	—	—	250	μA	V _{DS} =48V, V _{GS} =0V, T _J =150°C
I _{GSS}	—	—	100	nA	V _{GS} =20V
	—	—	-100	nA	V _{GS} =-20V
Q _G	—	—	110	nC	I _D =72A
Q _{GS}	—	—	29	nC	V _{DS} =48V
Q _{gd}	—	—	38	nC	V _{GS} =10V See Fig. 6 and 13 ④
t _{d(on)}	—	8.1	—	ns	V _{DD} =30V
t _r	—	250	—	ns	I _D =72A
t _{d(off)}	—	210	—	ns	R _G =9.1Ω
t _f	—	250	—	ns	R _D =0.34Ω See Figure 10 ④
L _D	—	5.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	—	13	—	nH	
C _{iss}	—	2400	—	pF	V _{GS} =0V
C _{oss}	—	1300	—	pF	V _{DS} =25V
C _{rss}	—	190	—	pF	f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	—	—	70*	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	—	—	290	A	
V _{SD}	—	—	2.0	V	T _J =25°C, I _S =73A, V _{GS} =0V ④
t _{rr}	—	120	180	ns	T _J =25°C, I _F =72A
Q _{rr}	—	0.50	0.80	μC	di/dt=100A/μs ④
t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11) ③ I_{SD}≤72A, di/dt≤200A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤175°C

② V_{DD}=25V, starting T_J=25°C, L=43μH, R_G=25Ω, I_{AS}=73A (See Figure 12) ④ Pulse width ≤ 300 μs; duty cycle ≤2%.

* Current limited by the package, (Die Current =73A)

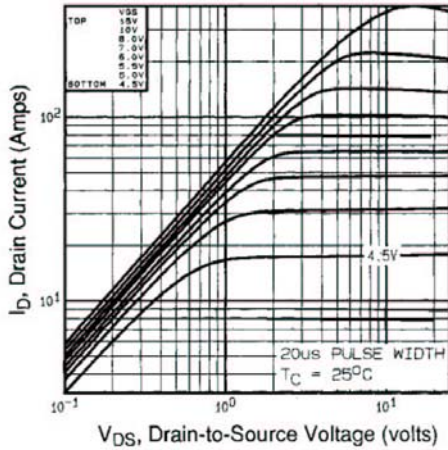


Fig 1. Typical Output Characteristics,
 $T_C=25^\circ\text{C}$

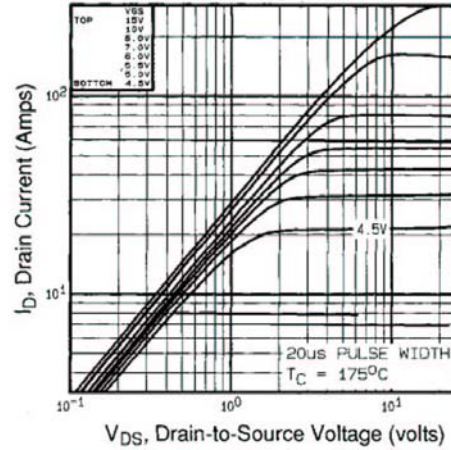


Fig 2. Typical Output Characteristics,
 $T_C=175^\circ\text{C}$

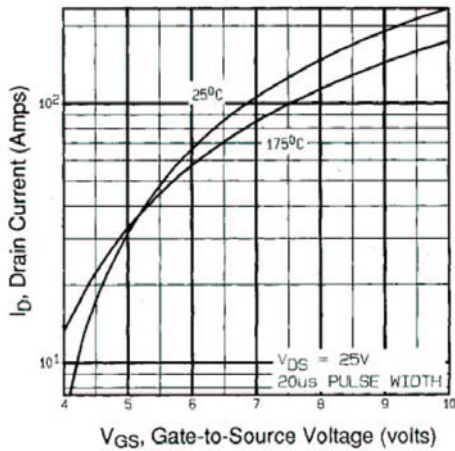


Fig 3. Typical Transfer Characteristics

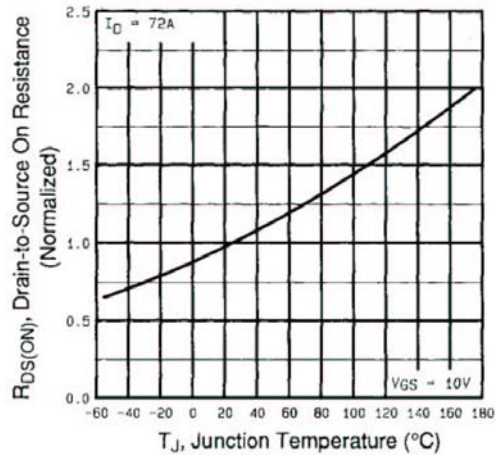


Fig 4. Normalized On-Resistance
Vs. Temperature

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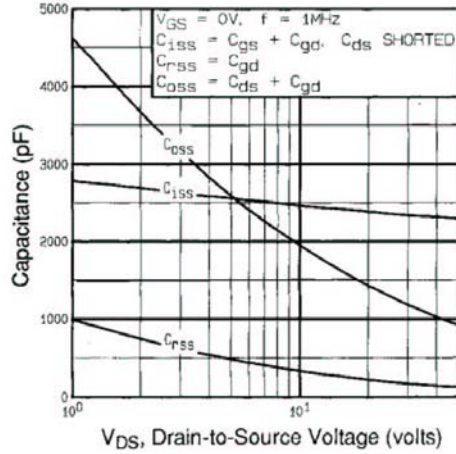


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

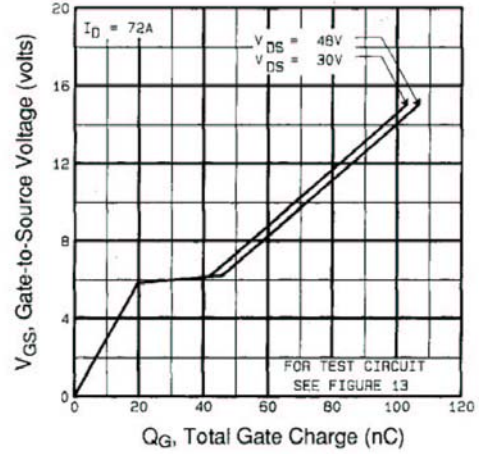


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

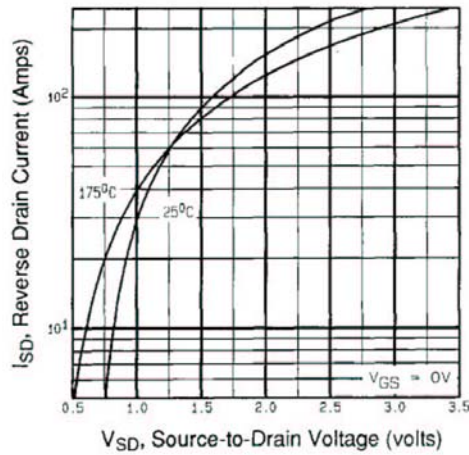


Fig 7. Typical Source-Drain Diode Forward Voltage

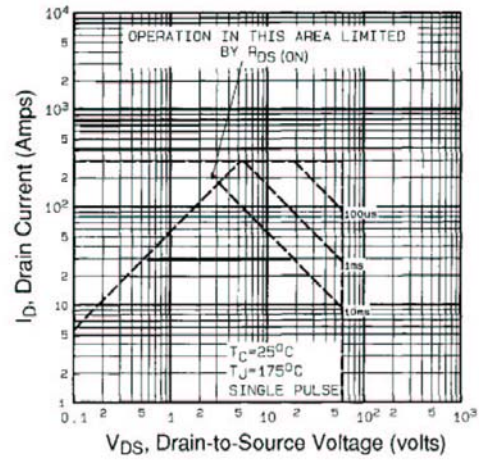


Fig 8. Maximum Safe Operating Area

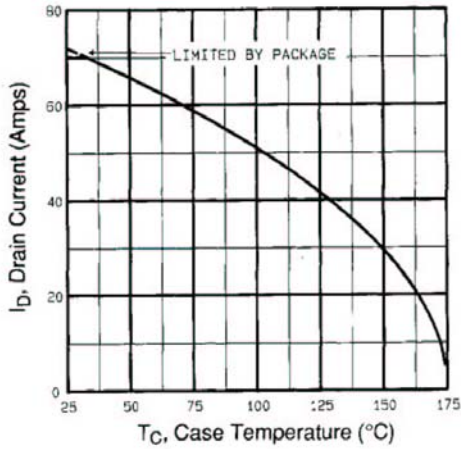


Fig 9. Maximum Drain Current Vs. Case Temperature

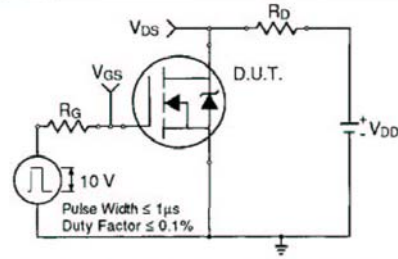


Fig 10a. Switching Time Test Circuit

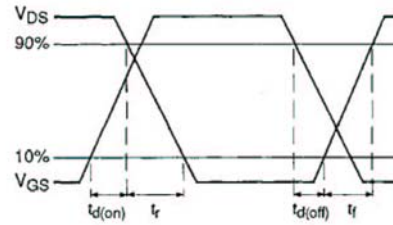


Fig 10b. Switching Time Waveforms

DATA SHEETS

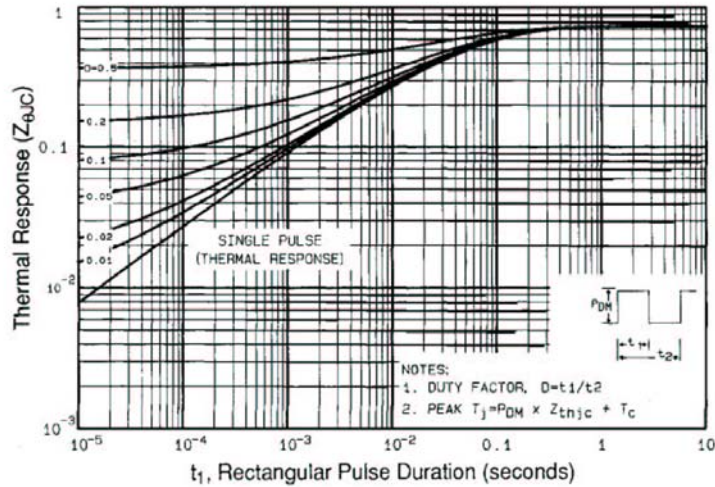


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

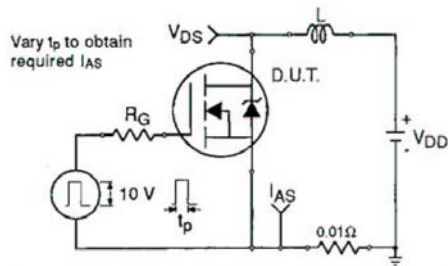


Fig 12a. Unclamped Inductive Test Circuit

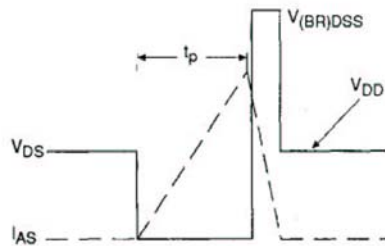


Fig 12b. Unclamped Inductive Waveforms

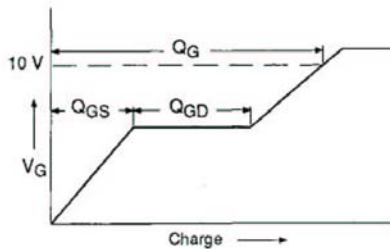


Fig 13a. Basic Gate Charge Waveform

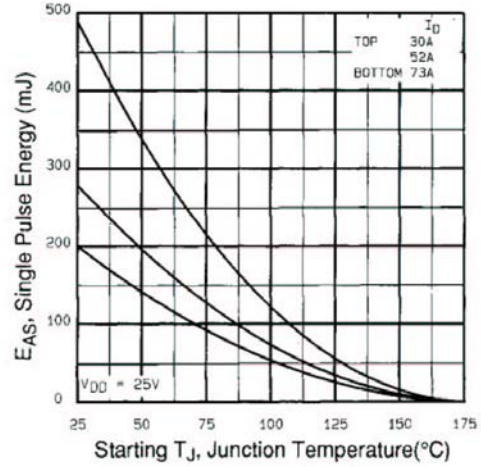


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

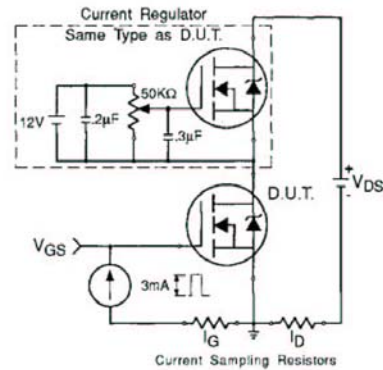


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1511

Appendix C: Part Marking Information – See page 1517



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