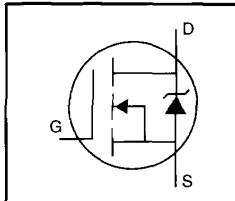


HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Dynamic dv/dt Rating
- Low Thermal Resistance



$$V_{DSS} = 450V$$

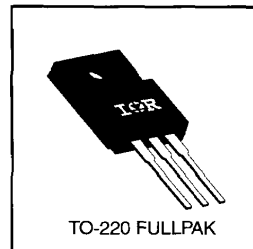
$$R_{DS(on)} = 1.2\Omega$$

$$I_D = 3.4A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



Absolute Maximum Ratings

Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	3.4	A
$I_D @ T_C = 100^\circ C$	2.1	
I_{DM}	14	
$P_D @ T_C = 25^\circ C$	35	W
	Linear Derating Factor	0.28
V_{GS}	±20	V
E_{AS}	100	mJ
I_{AR}	3.4	A
E_{AR}	3.5	mJ
dv/dt	4.0	V/ns
T_J	-55 to +150	°C
T_{STG}	Soldering Temperature, for 10 seconds	
	Mounting Torque, 6-32 or M3 screw	
		300 (1.6mm from case)
		10 lbf·in (1.1 N·m)

Thermal Resistance

Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	—	—	3.6	°C/W
$R_{\theta JA}$	—	—	65	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	450	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.63	—	V/°C	Reference to 25°C, I _D =1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	1.2	Ω	V _{GS} =10V, I _D =2.0A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	Forward Transconductance	1.5	—	—	S	V _{DS} =50V, I _D =2.0A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} =450V, V _{GS} =0V
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} =20V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V _{GS} =-20V
Q _g	Total Gate Charge	—	—	45	nC	I _D =4.9A
Q _{gs}	Gate-to-Source Charge	—	—	6.6	nC	V _{DS} =360V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	24	nC	V _{GS} =10V See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	5.9	—	ns	V _{DD} =225V
t _r	Rise Time	—	22	—		I _D =4.9A
t _{d(off)}	Turn-Off Delay Time	—	40	—		R _G =12Ω
t _f	Fall Time	—	21	—		R _D =45Ω See Figure 10 ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	680	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	190	—		V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	75	—		f=1.0MHz See Figure 5
C	Drain to Sink Capacitance	—	12	—		f=1.0MHz


Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	3.4	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	14		
V _{SD}	Diode Forward Voltage	—	—	2.0	V	T _J =25°C, I _S =4.9A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	460	690	ns	T _J =25°C, I _F =4.9A
Q _{rr}	Reverse Recovery Charge	—	1.8	2.7	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DD}=50V, starting T_J=25°C, L=15mH R_G=25Ω, I_{AS}=3.4A (See Figure 12)
- ③ I_{SD}≤4.9A, di/dt≤80A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.
- ⑤ t=60s, f=60Hz

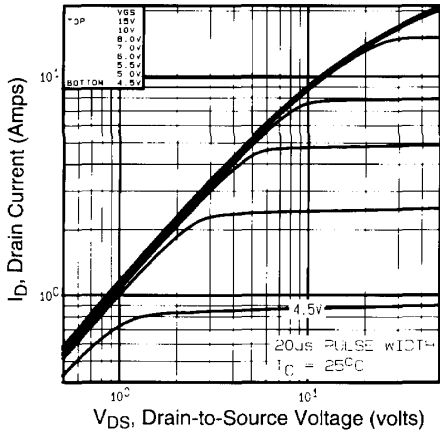


Fig 1. Typical Output Characteristics, $T_C = 25^\circ\text{C}$

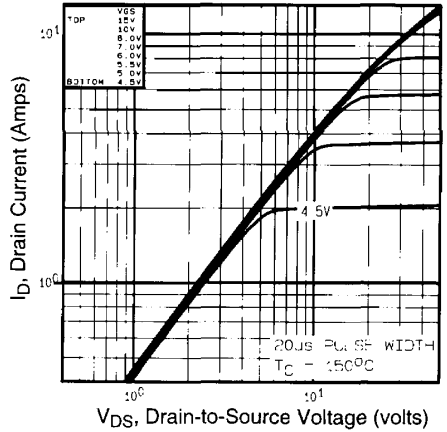


Fig 2. Typical Output Characteristics, $T_C = 150^\circ\text{C}$

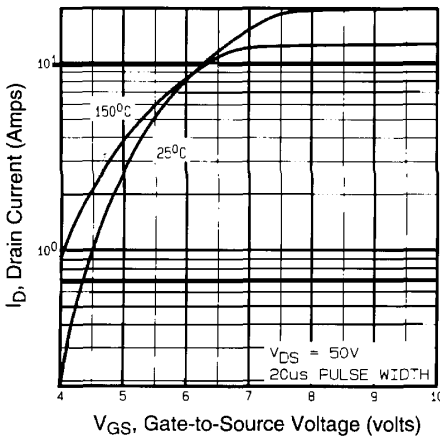


Fig 3. Typical Transfer Characteristics

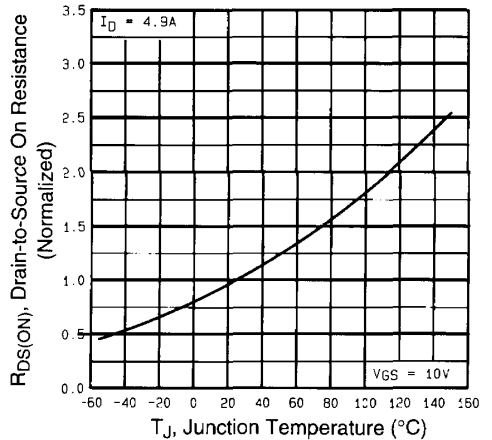


Fig 4. Normalized On-Resistance Vs. Temperature

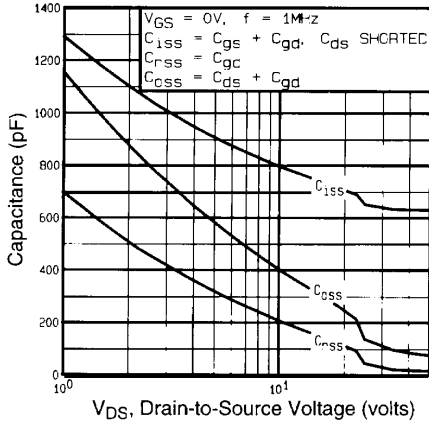


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

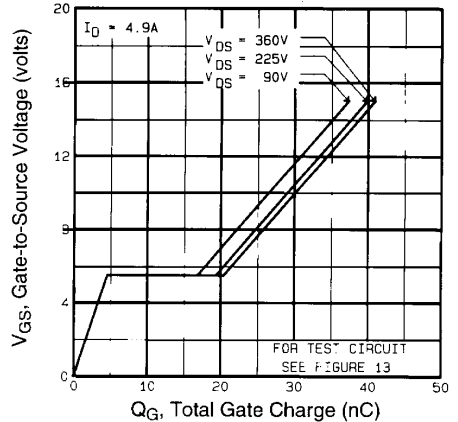


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

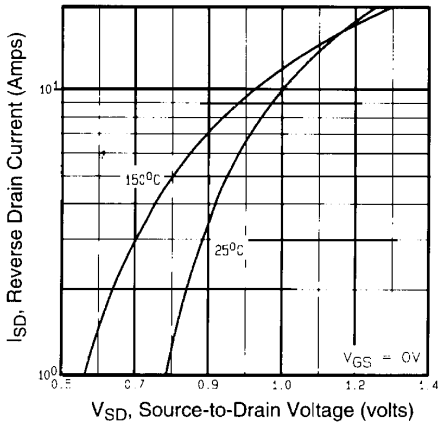


Fig 7. Typical Source-Drain Diode Forward Voltage

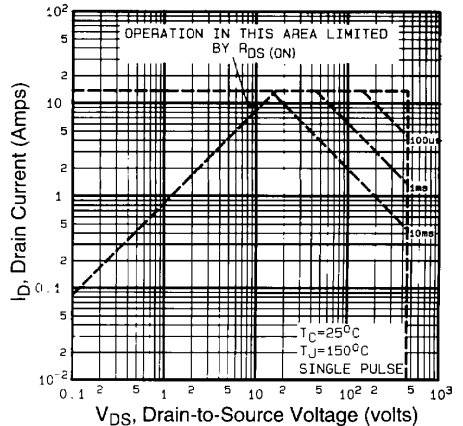


Fig 8. Maximum Safe Operating Area

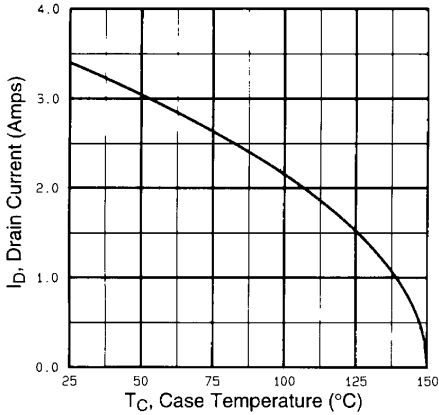


Fig 9. Maximum Drain Current Vs. Case Temperature

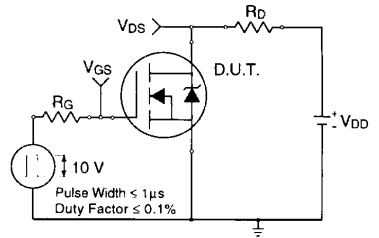


Fig 10a. Switching Time Test Circuit

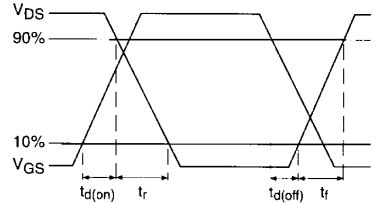


Fig 10b. Switching Time Waveforms

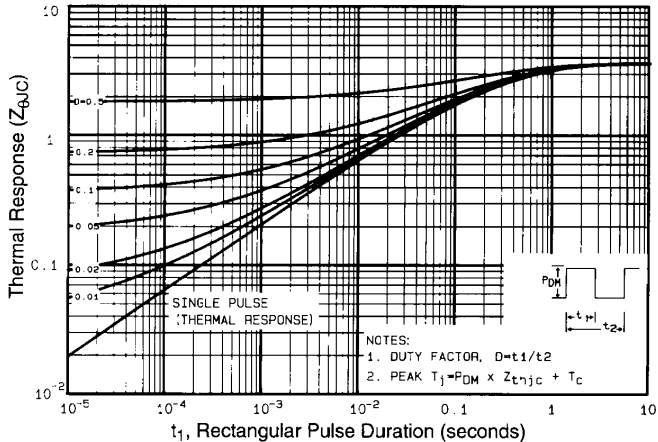


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

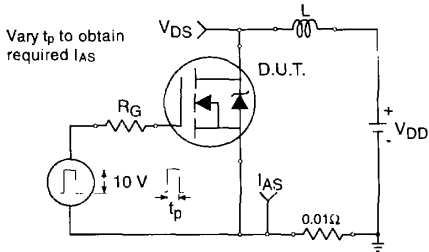


Fig 12a. Unclamped Inductive Test Circuit

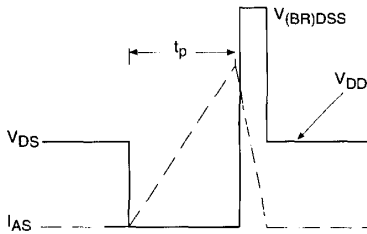


Fig 12b. Unclamped Inductive Waveforms

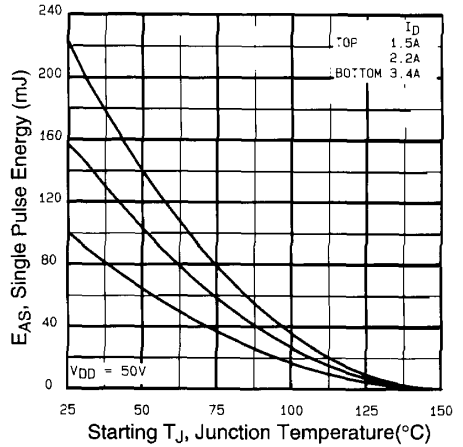


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

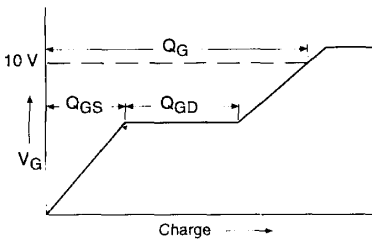


Fig 13a. Basic Gate Charge Waveform

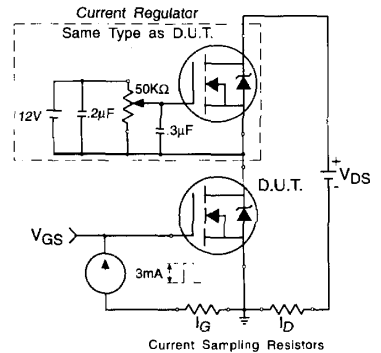


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit

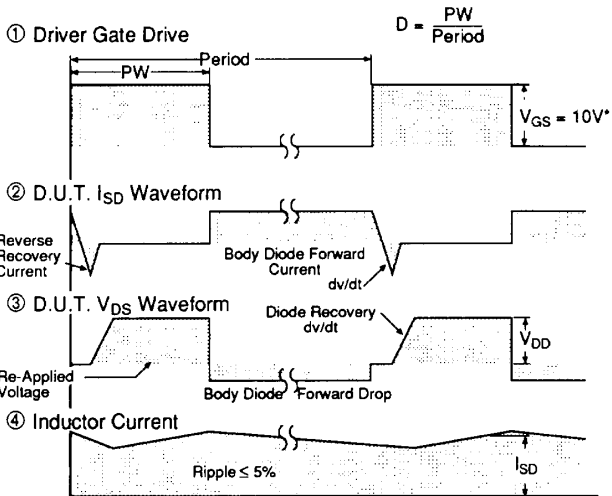
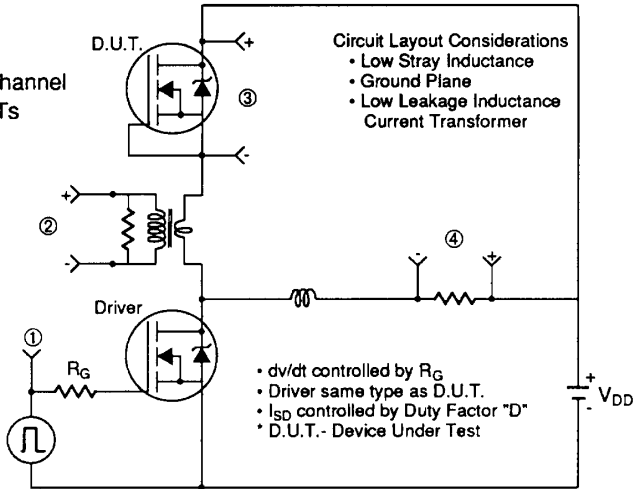
Appendix B: Package Outline Mechanical Drawing

Appendix C: Part Marking Information

Appendix A

Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs

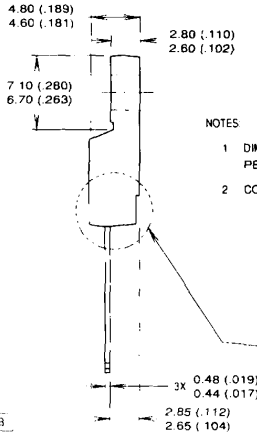
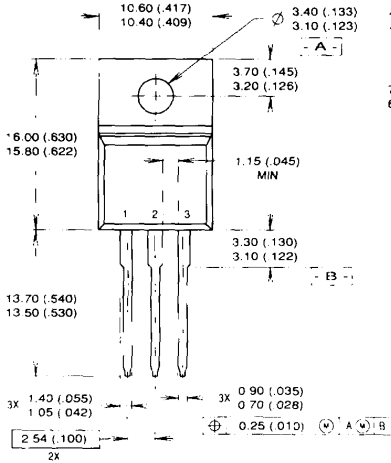


* $V_{GS} = 5V$ for Logic Level Devices

Package Outline

TO-220 FullPak Outline

Dimensions are shown in millimeters (inches)

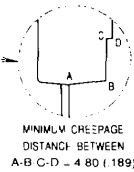


LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

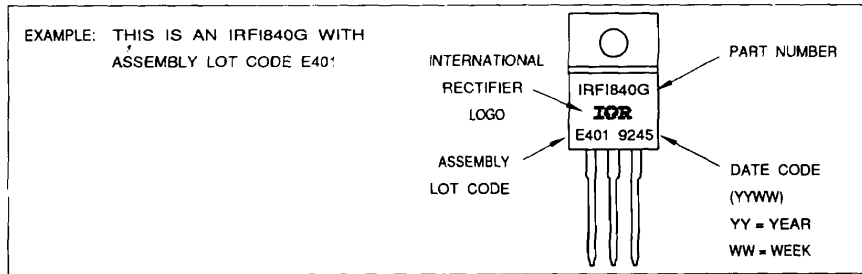
NOTES

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.



Part Marking Information

TO-220 FULL-PAK



Appendix C



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