

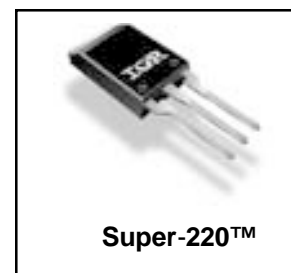
Applications

- High frequency DC-DC converters

V_{DSS}	R_{DS(on) max}	I_D
200V	0.023Ω	98A[Ⓒ]

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	98 [Ⓒ]	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	71 [Ⓒ]	
I _{DM}	Pulsed Drain Current [Ⓓ]	390	
P _D @ T _C = 25°C	Power Dissipation	650	W
	Linear Derating Factor	4.3	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt [Ⓔ]	6.3	V/ns
T _J	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T _{STG}			
	Recommended Clip Force	20	N

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.23	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.50	—	
R _{θJA}	Junction-to-Ambient	—	58	

Notes [Ⓓ] through [Ⓔ] are on page 8

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.22	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.023	Ω	$V_{GS} = 10V, I_D = 59A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

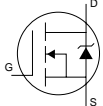
Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	41	—	—	S	$V_{DS} = 50V, I_D = 59A$
Q_g	Total Gate Charge	—	160	240	nC	$I_D = 59A$
Q_{gs}	Gate-to-Source Charge	—	45	67		$V_{DS} = 160V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	75	110		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	$V_{DD} = 100V$
t_r	Rise Time	—	160	—		$I_D = 59A$
$t_{d(off)}$	Turn-Off Delay Time	—	39	—		$R_G = 1.2\Omega$
t_f	Fall Time	—	77	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	6080	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1040	—		$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	150	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	7500	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	410	—		$V_{GS} = 0V, V_{DS} = 160V, f = 1.0MHz$
$C_{oss\ eff.}$	Effective Output Capacitance	—	790	—		$V_{GS} = 0V, V_{DS} = 0V\ to\ 160V$ ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	960	mJ
I_{AR}	Avalanche Current①	—	59	A
E_{AR}	Repetitive Avalanche Energy①	—	65	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	98	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	390		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 59A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	220	340	nS	$T_J = 25^\circ\text{C}, I_F = 59A$
Q_{rr}	Reverse Recovery Charge	—	1.9	2.8	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

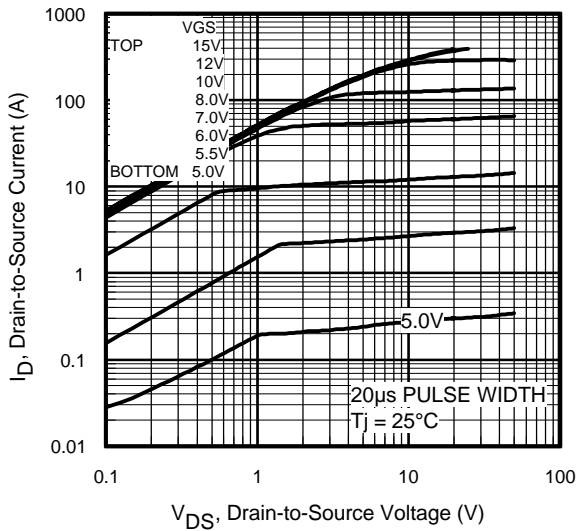


Fig 1. Typical Output Characteristics

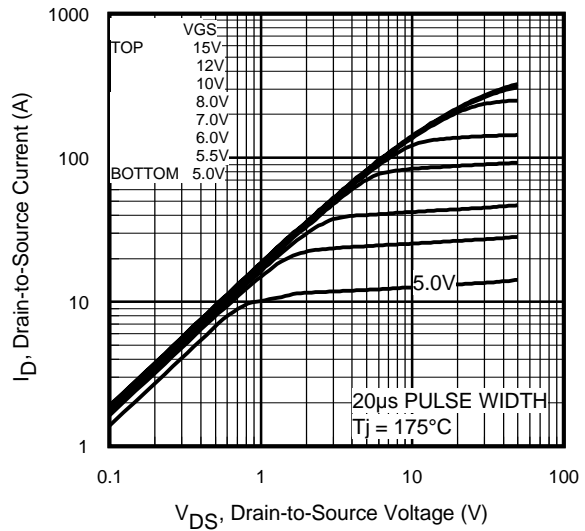


Fig 2. Typical Output Characteristics

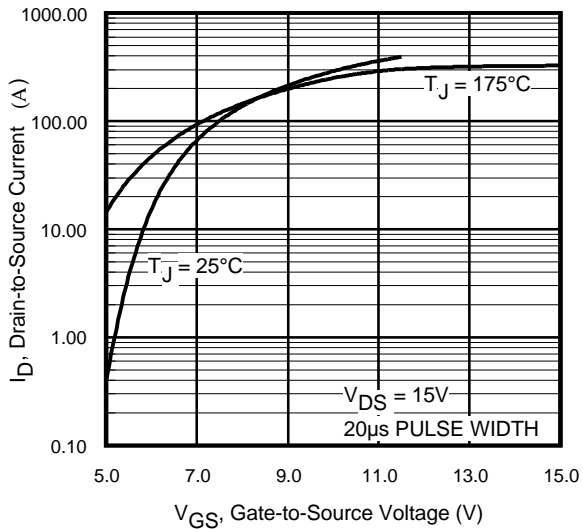


Fig 3. Typical Transfer Characteristics

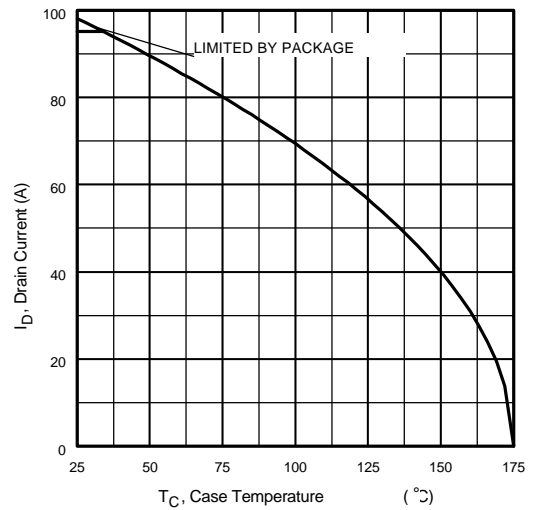


Fig 4. Normalized On-Resistance Vs. Temperature

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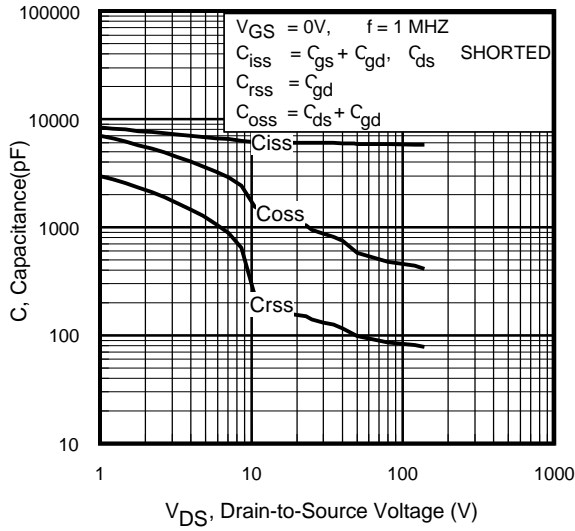


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

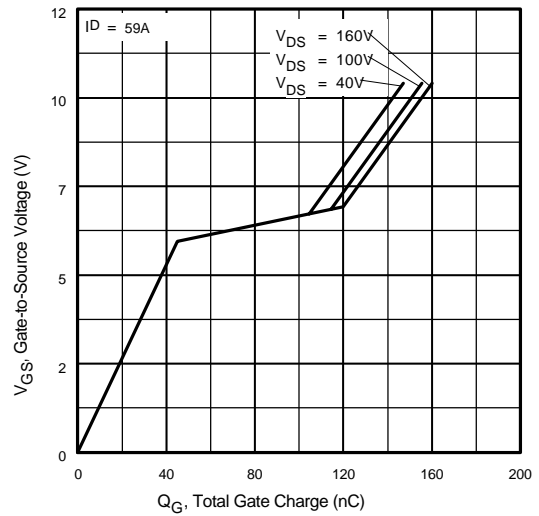


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

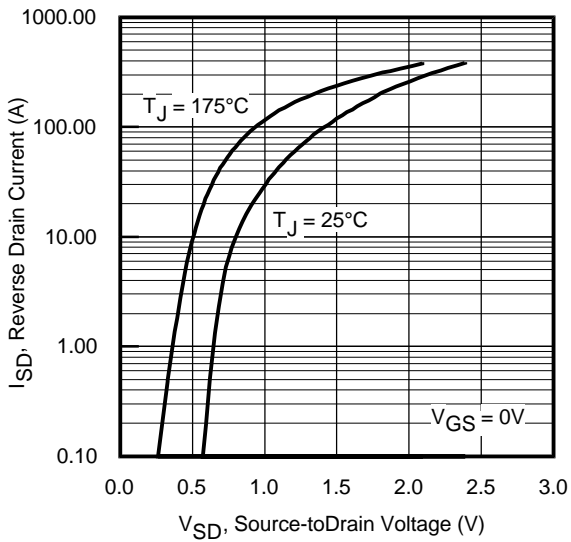


Fig 7. Typical Source-Drain Diode Forward Voltage

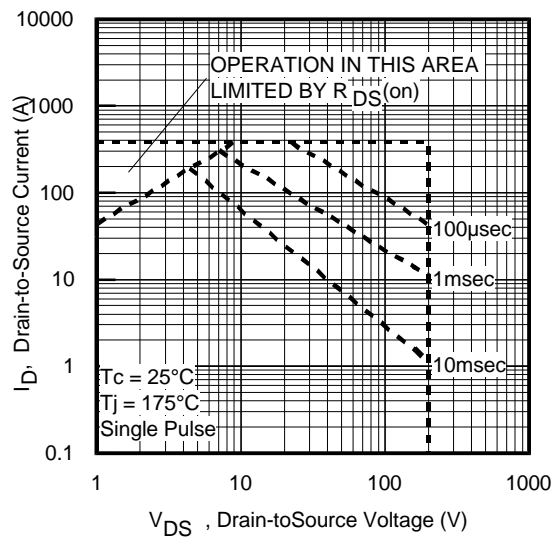


Fig 8. Maximum Safe Operating Area

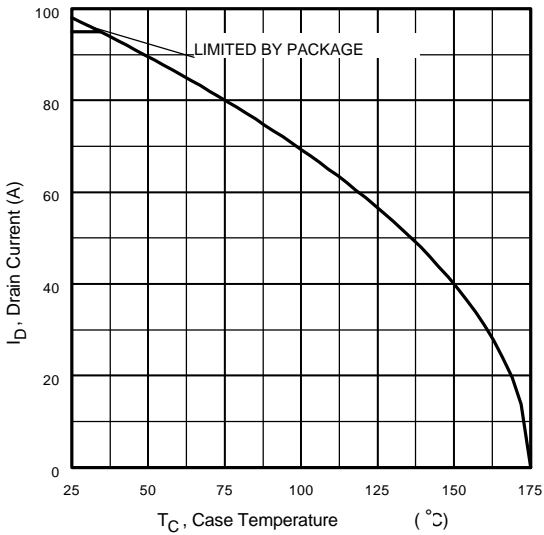


Fig 9. Maximum Drain Current Vs. Case Temperature

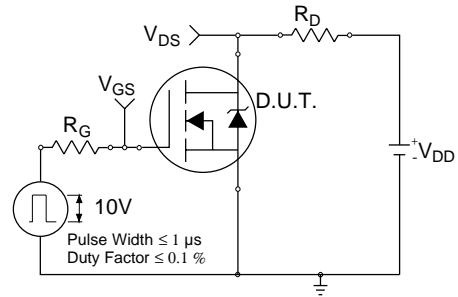


Fig 10a. Switching Time Test Circuit

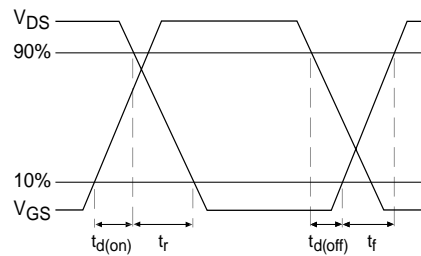


Fig 10b. Switching Time Waveforms

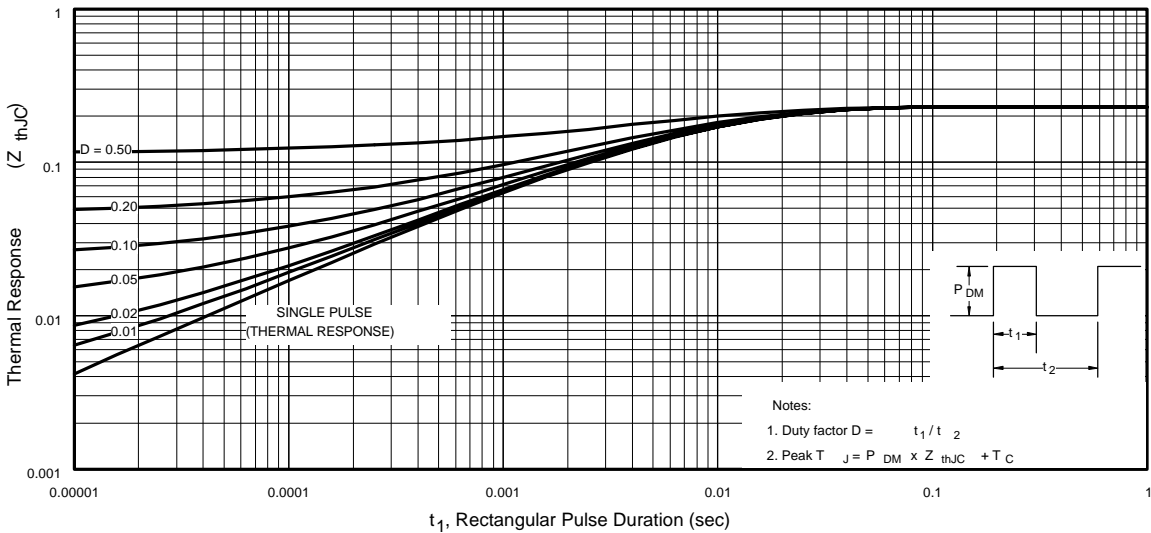


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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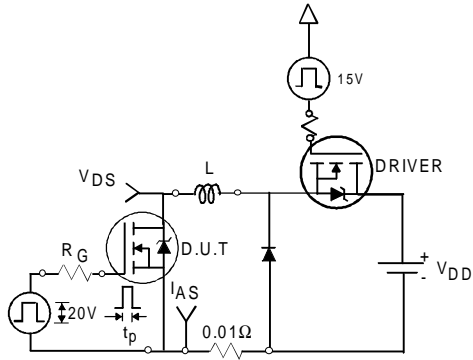


Fig 12a. Unclamped Inductive Test Circuit

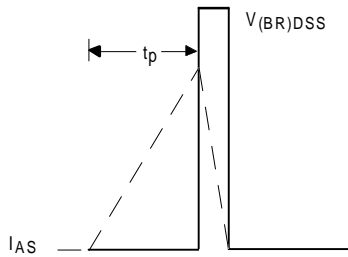


Fig 12b. Unclamped Inductive Waveforms

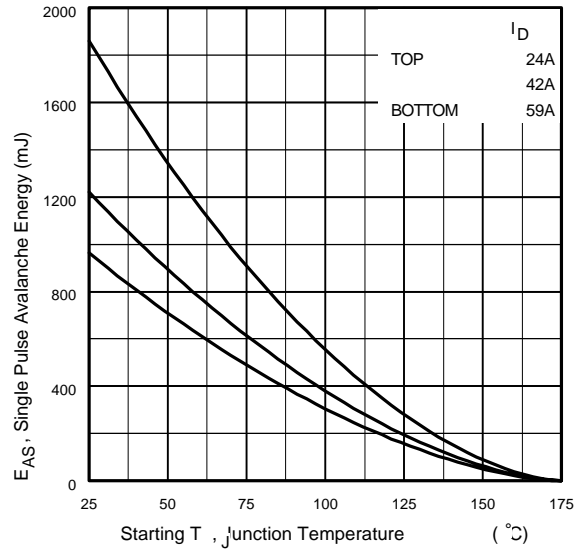


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

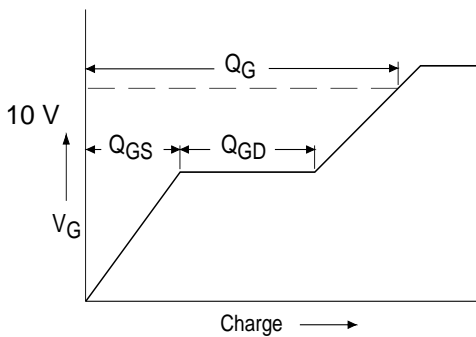


Fig 13a. Basic Gate Charge Waveform

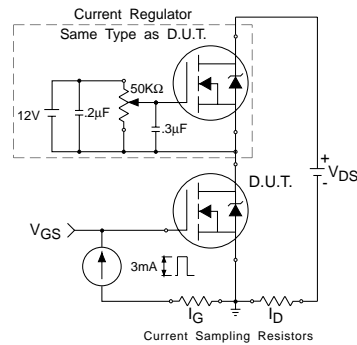
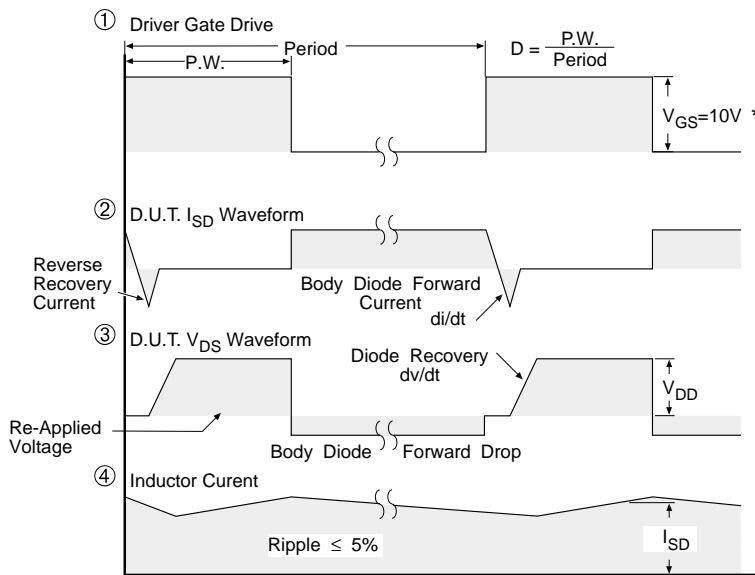
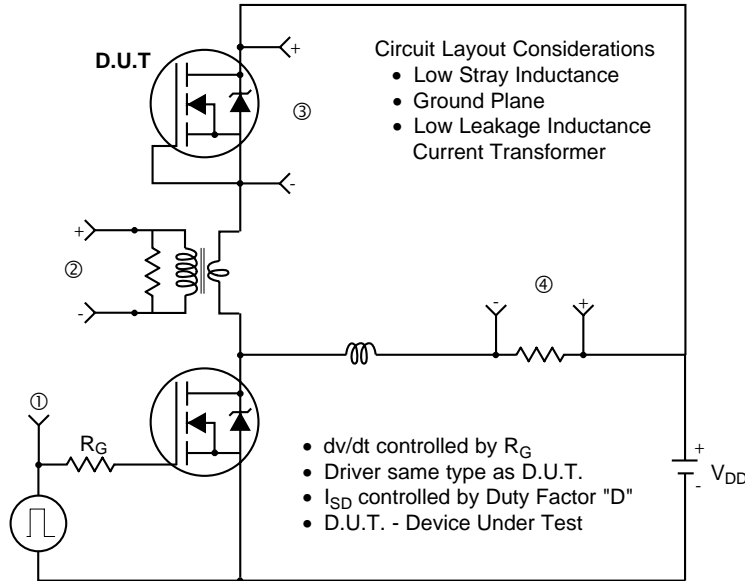


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

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