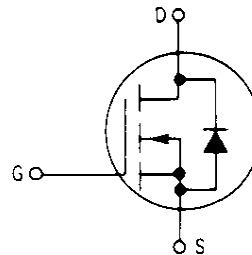


# Power Field Effect Transistor

## N-Channel Enhancement-Mode Silicon Gate

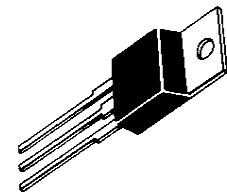
This TMOS Power FET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low  $R_{DS(on)}$  to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



**IRF640**

TMOS POWER FET  
18 AMPERES  
 $R_{DS(on)} = 0.18 \text{ OHM}$   
200 VOLTS



CASE 221A-06  
(TO-220AB)

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	200	Vdc
Drain-Gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	200	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 20$	Vdc
Drain Current	$I_D$		Adc
Continuous, $T_C = 25^\circ\text{C}$		18	
Peak, $T_C = 25^\circ\text{C}$		72	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	125 1	Watts W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 62.5	$^\circ\text{C/W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 10 Seconds	$T_L$	260	$^\circ\text{C}$

See the MTP20N20E Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Drain-Source Breakdown Voltage ( $V_{GS} = 0, I_D = 0.25 \text{ mA}$ )	$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0$ ) ( $V_{DS} = 0.8 \text{ Rated } V_{DSS}, V_{GS} = 0, T_J = 125^\circ\text{C}$ )	$I_{DSS}$	—	0.2 1	mAdc
Gate-Body Leakage Current, Forward ( $V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$ )	$I_{GSSF}$	—	100	nAdc
Gate-Body Leakage Current, Reverse ( $V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$ )	$I_{GSSR}$	—	100	nAdc

**ON CHARACTERISTICS\***

Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 0.25 \text{ mA}$ )	$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance ( $V_{GS} = 10 \text{ Vdc}, I_D = 10 \text{ Adc}$ )	$R_{DS(on)}$	—	0.18	Ohm
On-State Drain Current ( $V_{GS} = 10 \text{ V}$ ) ( $V_{DS} \geq 3.2 \text{ Vdc}$ )	$I_{D(on)}$	18	—	Adc
Forward Transconductance ( $V_{DS} \geq 3.2 \text{ V}, I_D = 10 \text{ A}$ )	$g_{FS}$	6	—	mhos

**DYNAMIC CHARACTERISTICS**

Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz})$	$C_{iss}$	—	1600	pF
Output Capacitance		$C_{oss}$	—	750	
Reverse Transfer Capacitance		$C_{rss}$	—	300	

**SWITCHING CHARACTERISTICS\***

Turn-On Delay Time	$(V_{DD} \approx 30 \text{ V}, I_D = 15 \text{ Apk}, R_{gen} = 4.7 \text{ Ohms})$	$t_{d(on)}$	—	30	ns
Rise Time		$t_r$	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	80	
Fall Time		$t_f$	—	60	
Total Gate Charge	$(V_{DS} = 0.8 \text{ Rated } V_{DSS}, V_{GS} = 10 \text{ Vdc}, I_D = \text{Rated } I_D)$	$Q_g$	36 (Typ)	60	nC
Gate-Source Charge		$Q_{gs}$	16 (Typ)	—	
Gate-Drain Charge		$Q_{gd}$	22 (Typ)	—	

**SOURCE DRAIN DIODE CHARACTERISTICS\***

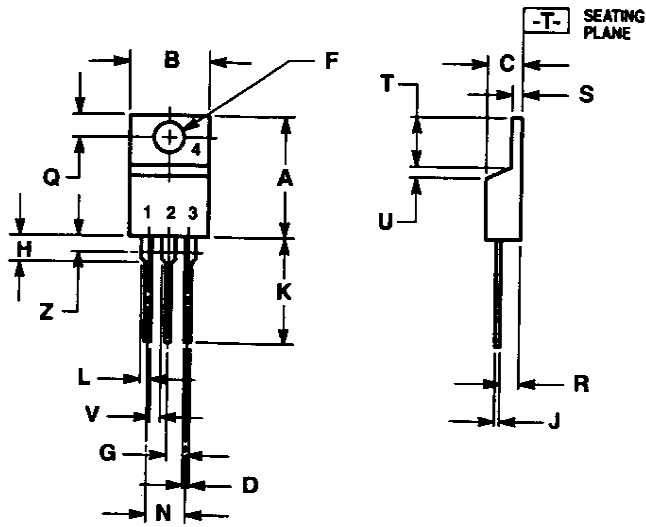
Forward On-Voltage	$(I_S = \text{Rated } I_D, V_{GS} = 0)$	$V_{SD}$	1.8 (Typ)	2.0	Vdc
Forward Turn-On Time		$t_{on}$	Limited by stray inductance		
Reverse Recovery Time		$t_{rr}$	450 (Typ)	—	ns

**INTERNAL PACKAGE INDUCTANCE**

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	$L_d$	3.5 (Typ) 4.5 (Typ)	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	$L_s$	7.5 (Typ)	—	

\*Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

**PACKAGE OUTLINE DIMENSIONS AND FOOTPRINTS (continued)**

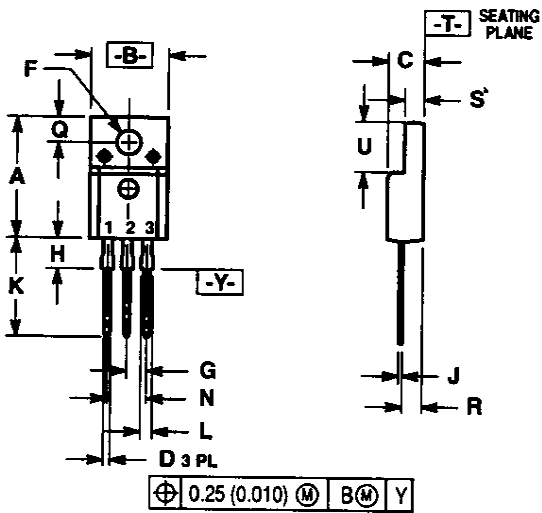


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.060	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.060	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

- STYLE 5:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE  
 4. DRAIN

**CASE 221A-06  
 (TO-220AB)  
 ISSUE Y**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC		2.54 BSC	
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

- STYLE 1:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE

**CASE 221D-02  
 (ISOLATE TO-220 TYPE)  
 ISSUE D**



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