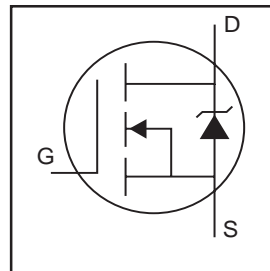


IRF530NS/L

HEXFET® Power MOSFET

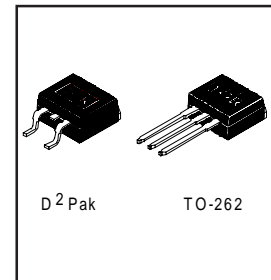
- Advanced Process Technology
- Surface Mount (IRF530NS)
- Low-profile through-hole (IRF530NL)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



$V_{DS} = 100V$
$R_{DS(on)} = 0.11\Omega$
$I_D = 17A$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications. The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRF530NL) is available for low-profile applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	17	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	12	
I_{DM}	Pulsed Drain Current ①⑤	60	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	79	W
	Linear Derating Factor	0.53	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	150	mJ
I_{AR}	Avalanche Current*9.0	A	
E_{AR}	Repetitive Avalanche Energy①	7.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
DV _{(BR)DSS} /DT _J	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I _D = 1mA ^⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.11	Ω	V _{GS} = 10V, I _D = 9.0A ^④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	6.4	—	—	S	V _{DS} = 50V, I _D = 9.0A ^⑤
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 100V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	44	nC	I _D = 9.0A
Q _{gs}	Gate-to-Source Charge	—	—	6.2		V _{DS} = 80V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	21		V _{GS} = 10V, See Fig. 6 and 13 ^{④ ⑤}
t _{d(on)}	Turn-On Delay Time	—	6.4	—	ns	V _{DD} = 50V
t _r	Rise Time	—	27	—		I _D = 9.0A
t _{d(off)}	Turn-Off Delay Time	—	37	—		R _G = 12Ω
t _f	Fall Time	—	25	—		R _D = 5.5Ω, See Fig. 10 ^{④ ⑤}
L _S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C _{iss}	Input Capacitance	—	640	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	160	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	88	—		f = 1.0MHz, See Fig. 5 ^⑤

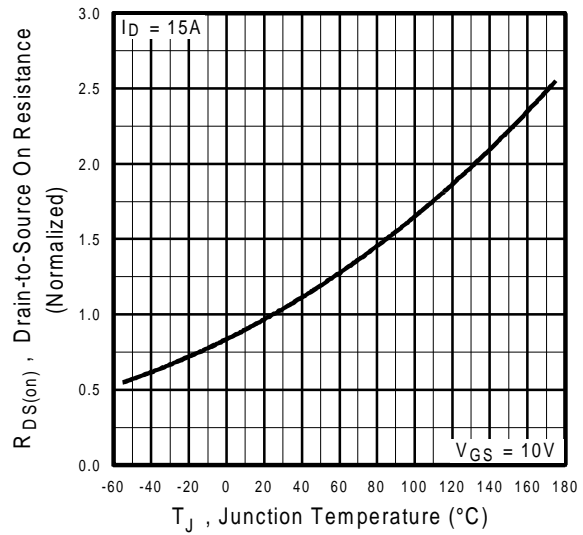
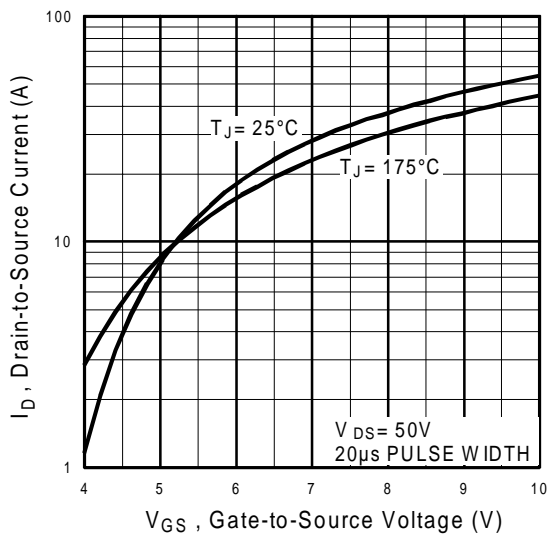
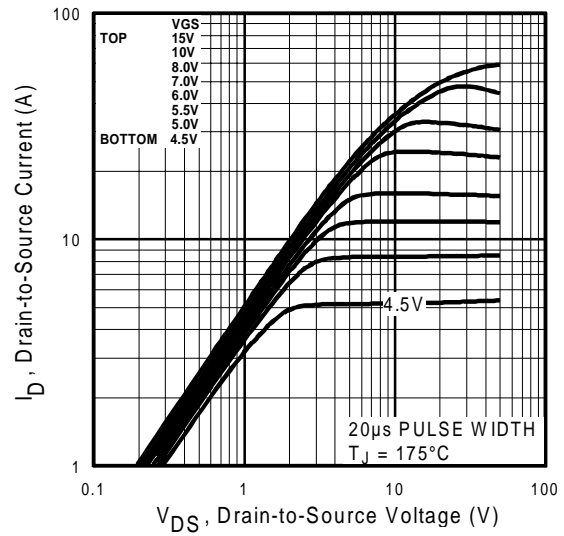
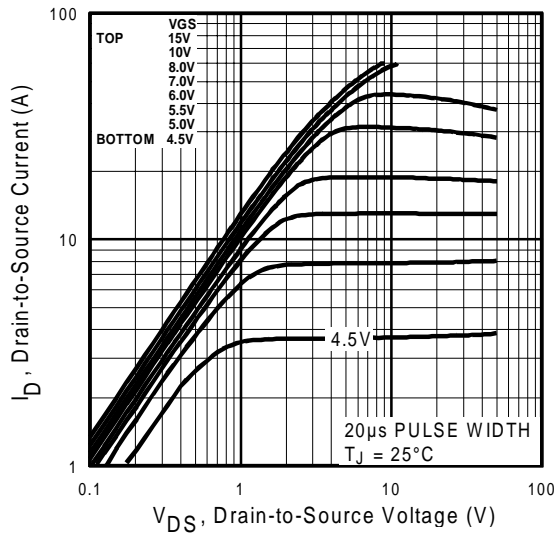
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ^{① ⑤}	—	—	60		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 9.0A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	130	190	ns	T _J = 25°C, I _F = 9.0A
Q _{rr}	Reverse Recovery Charge	—	650	970	nC	di/dt = 100A/μs ^{④ ⑤}
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 3.1mH
R_G = 25W, I_{AS} = 9.0A. (See Figure 12)
- ③ I_{SD} ≤ 9.0A, di/dt ≤ 180A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ Uses IRF530N data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended soldering techniques refer to application note #AN-994.



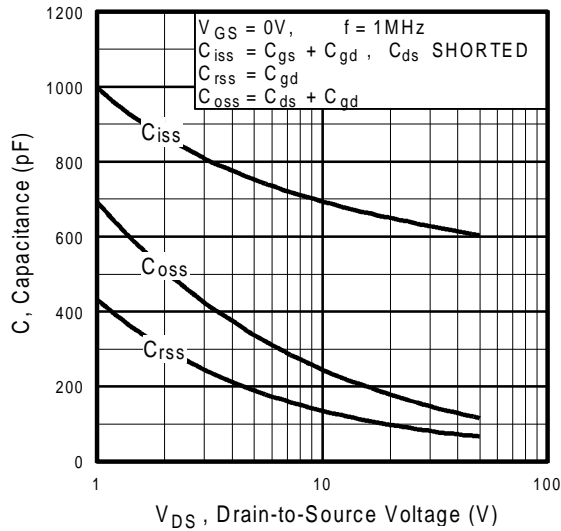


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

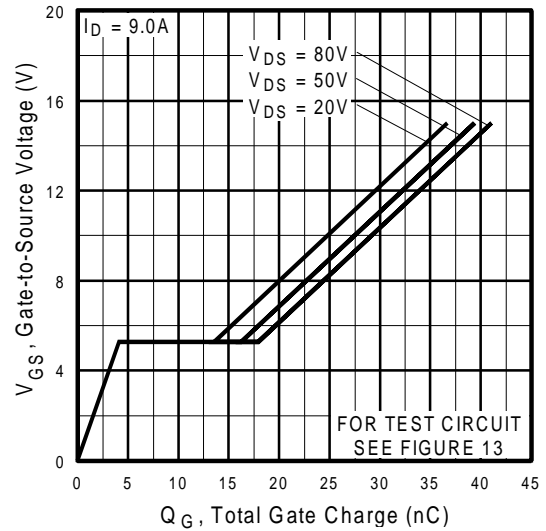


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

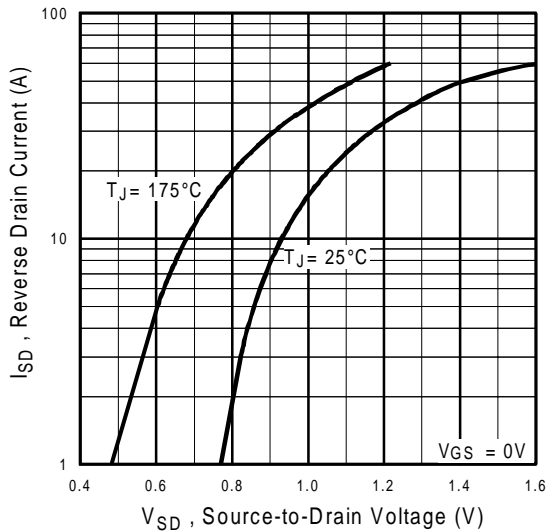


Fig 7. Typical Source-Drain Diode Forward Voltage

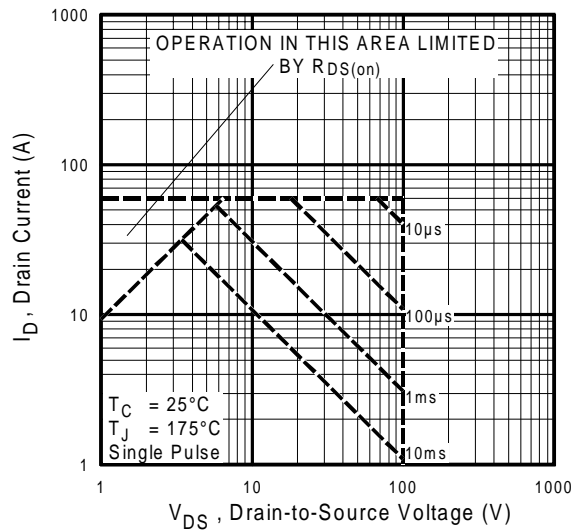


Fig 8. Maximum Safe Operating Area

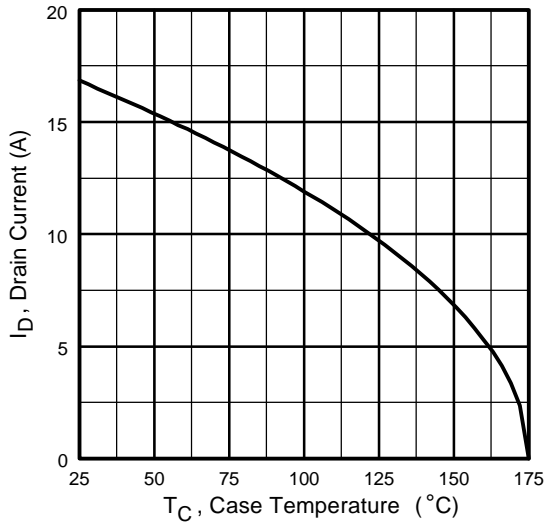


Fig 9. Maximum Drain Current Vs. Case Temperature

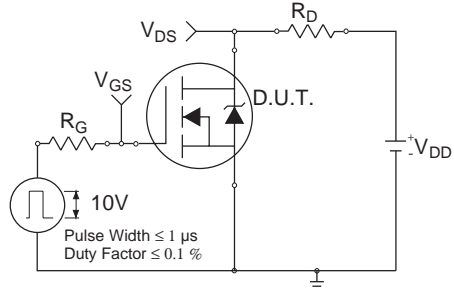


Fig 10a. Switching Time Test Circuit

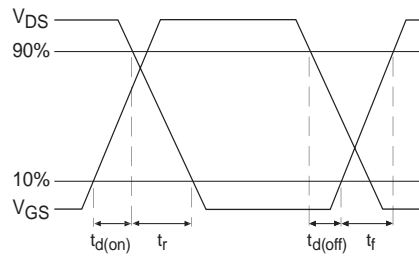


Fig 10b. Switching Time Waveforms

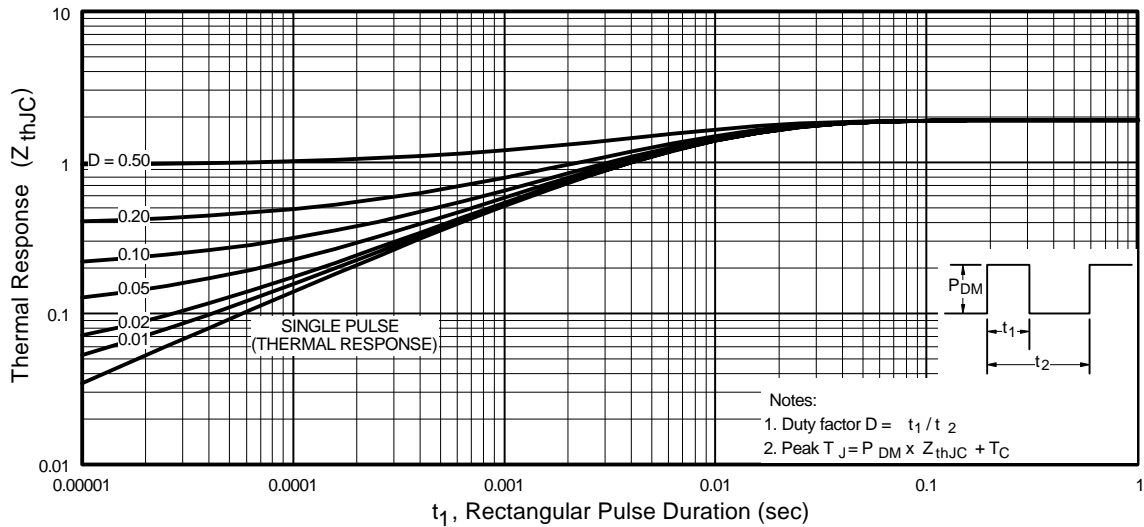


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

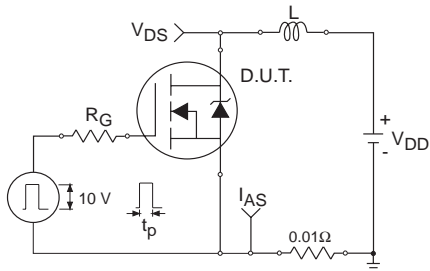


Fig 12a. Unclamped Inductive Test Circuit

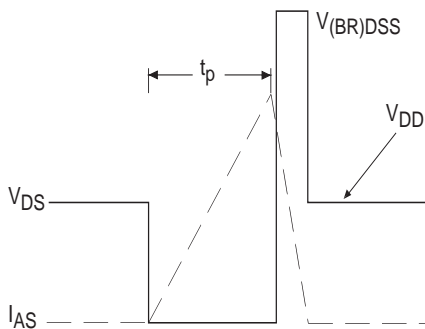


Fig 12b. Unclamped Inductive Waveforms

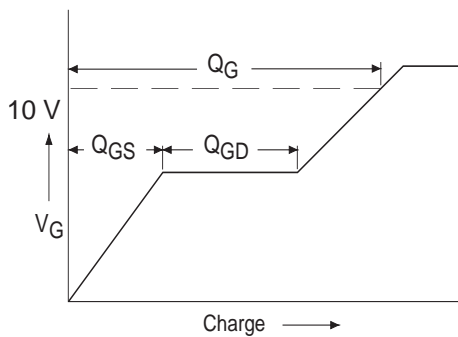


Fig 13a. Basic Gate Charge Waveform

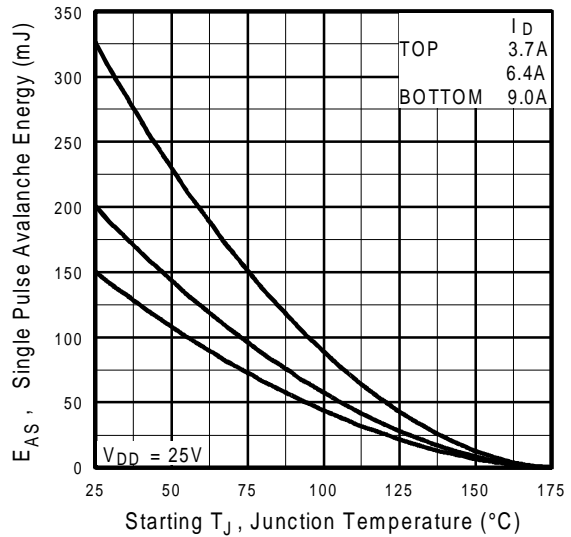


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

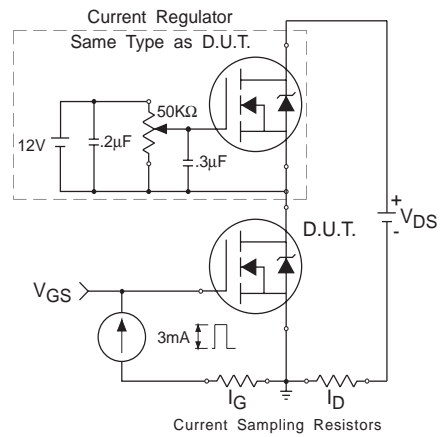
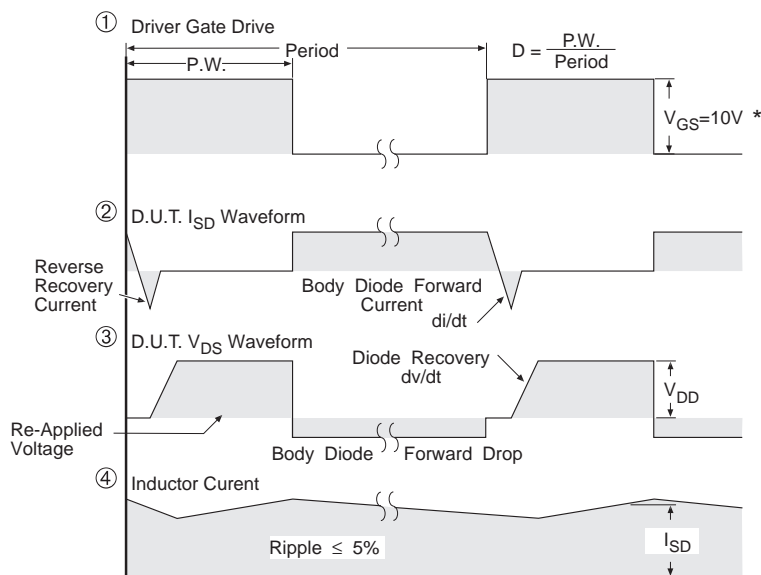
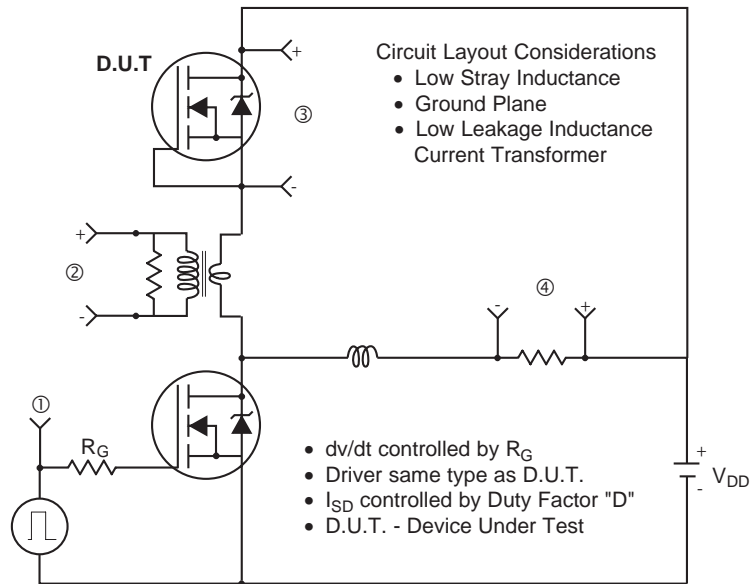


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



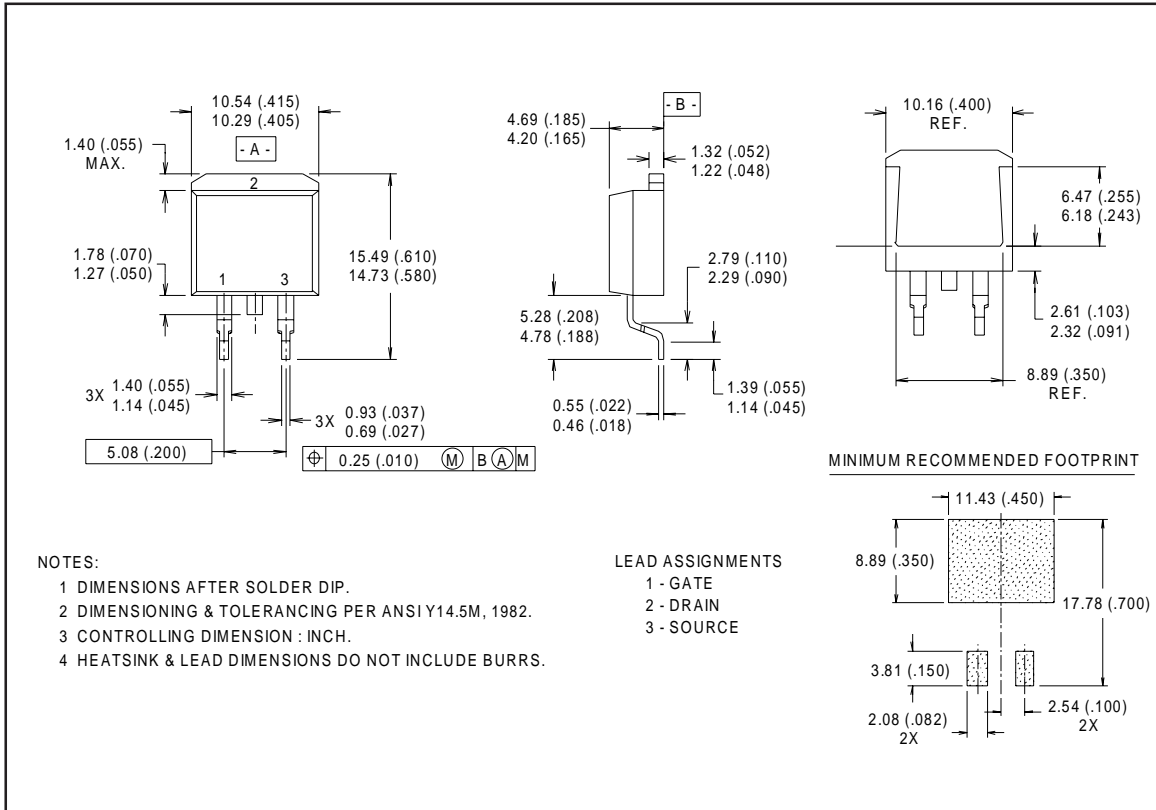
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

IRF530NS/L

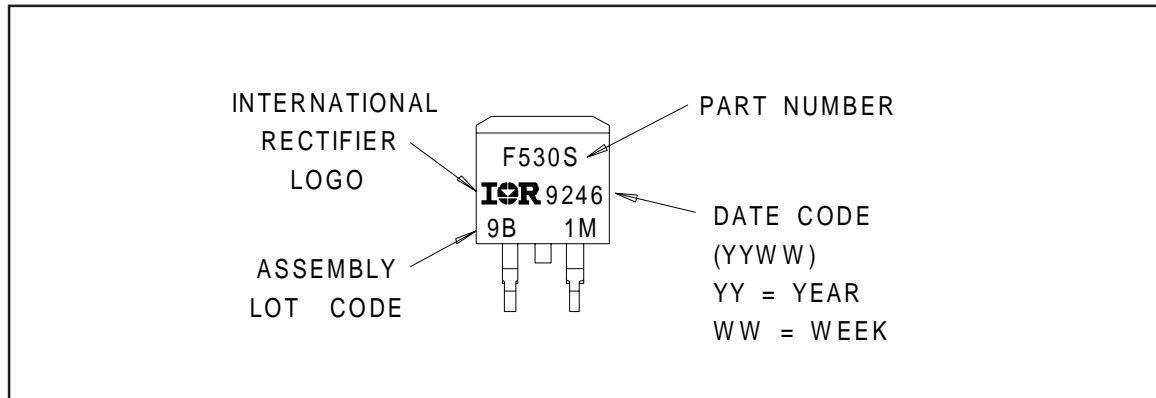
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D²Pak Package Outline



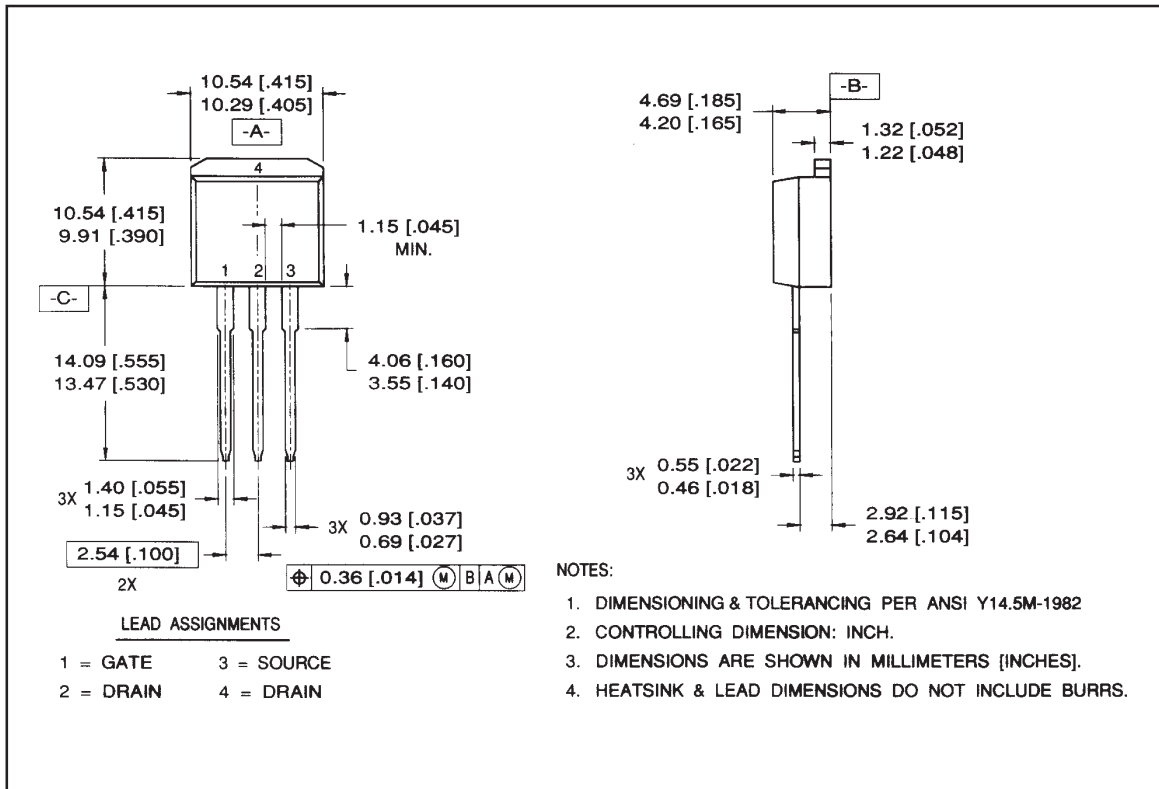
Part Marking Information

D²Pak



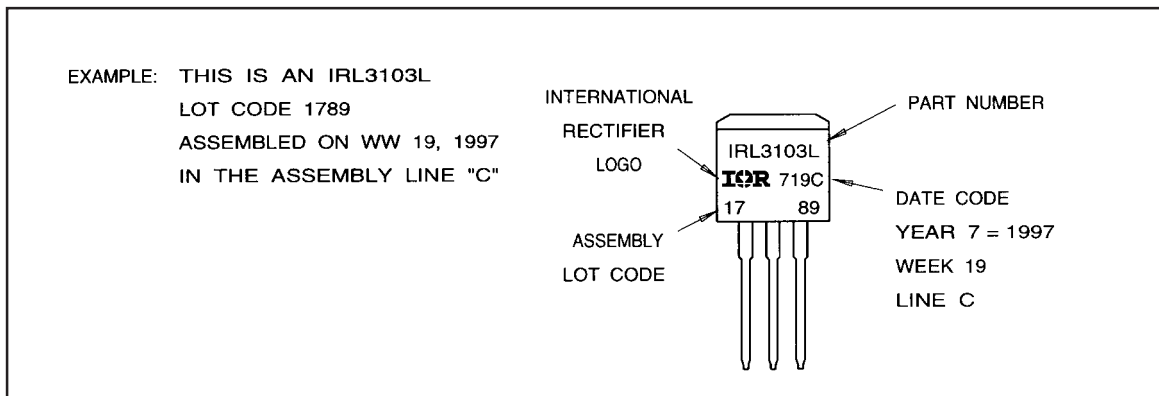
Package Outline

TO-262 Outline



Part Marking Information

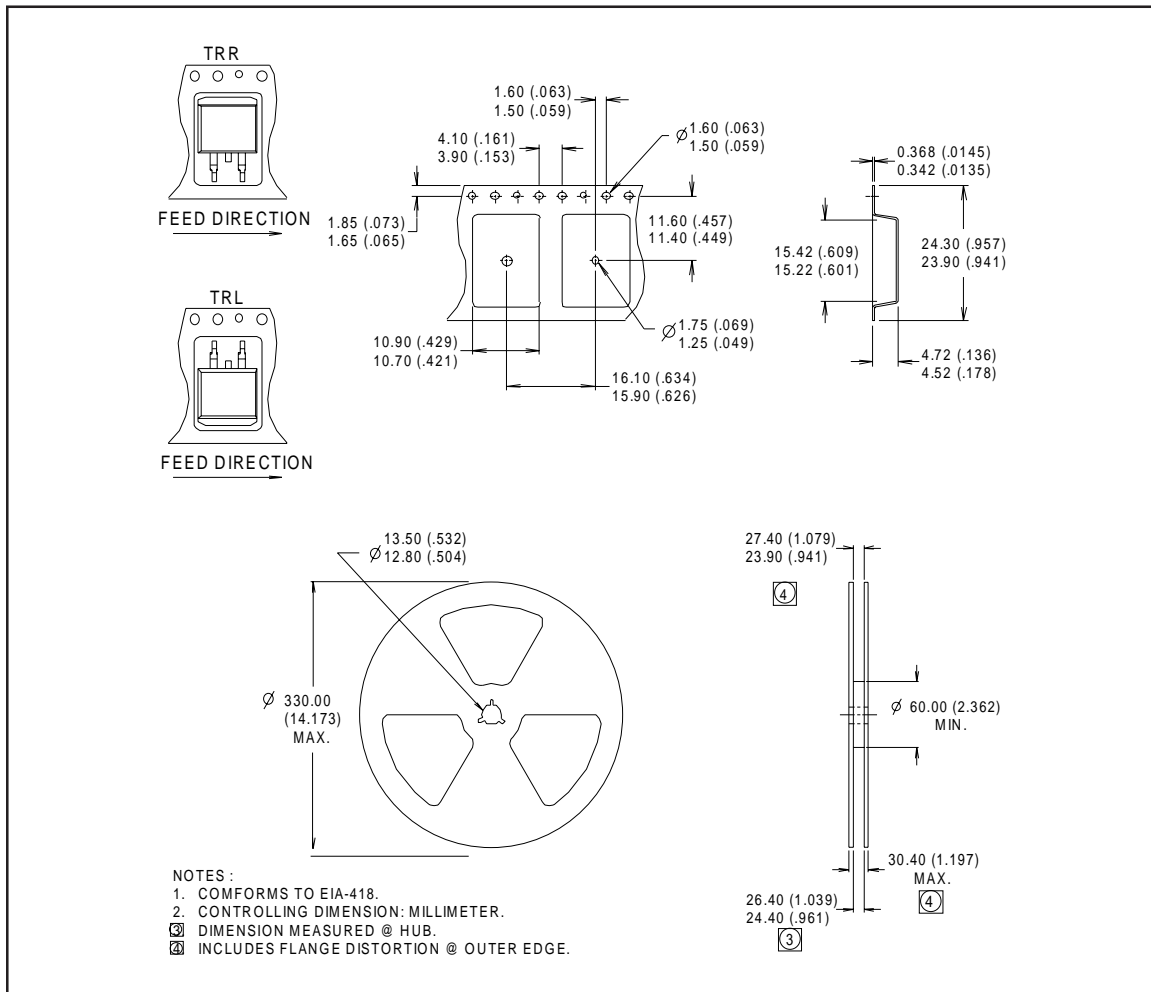
TO-262



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Tape & Reel Information D²Pak



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