

Typical Applications

- 42 Volts Automotive Electrical Systems
- Electrical Power Steering (EPS)
- Integrated Starter Alternator

Benefits

- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Automotive [Q101] Qualified

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

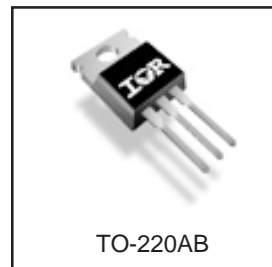
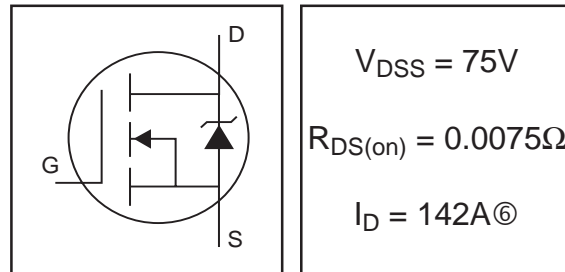
Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	142⑥	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	100⑥	
I _{DM}	Pulsed Drain Current ①	570	
P _D @ T _C = 25°C	Power Dissipation	380	W
	Linear Derating Factor	2.5	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy②	1250	mJ
I _{AR}	Avalanche Current①	See Fig.12a, 12b, 15, 16	A
E _{AR}	Repetitive Avalanche Energy②		mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.2	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

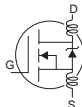
Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.40	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.50	—	
R _{θJA}	Junction-to-Ambient	—	62	

HEXFET® Power MOSFET



Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	75	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.086	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	0.0058	0.0075	Ω	V _{GS} = 10V, I _D = 85A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = 10V, I _D = 250μA
g _{fs}	Forward Transconductance	79	—	—	S	V _{DS} = 25V, I _D = 85A
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 75V, V _{GS} = 0V
		—	—	250		V _{DS} = 60V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V
Q _g	Total Gate Charge	—	210	320	nC	I _D = 85A
Q _{gs}	Gate-to-Source Charge	—	45	68		V _{DS} = 60V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	73	110		V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	22	—	ns	V _{DD} = 38V
t _r	Rise Time	—	130	—		I _D = 85A
t _{d(off)}	Turn-Off Delay Time	—	84	—		R _G = 1.8Ω
t _f	Fall Time	—	86	—		V _{GS} = 10V ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	7750	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1230	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	310	—		f = 1.0MHz, See Fig. 5
C _{oss}	Output Capacitance	—	5770	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	790	—		V _{GS} = 0V, V _{DS} = 60V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance ⑤	—	1420	—		V _{GS} = 0V, V _{DS} = 0V to 60V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	142⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	570		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 85A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	130	200	ns	T _J = 25°C, I _F = 85A
Q _{rr}	Reverse Recovery Charge	—	690	1040	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting T_J = 25°C, L = 0.21mH
R_G = 25Ω, I_{AS} = 85A, V_{GS} = 10V (See Figure 12).
- ③ I_{SD} ≤ 85A, di/dt ≤ 310A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ⑦ Limited by T_{Jmax}, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

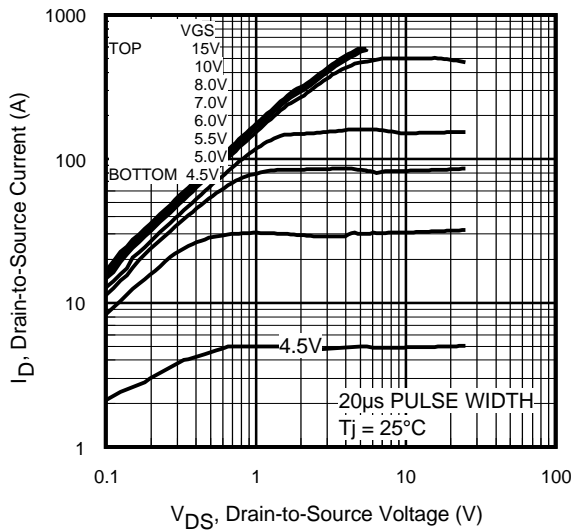


Fig 1. Typical Output Characteristics

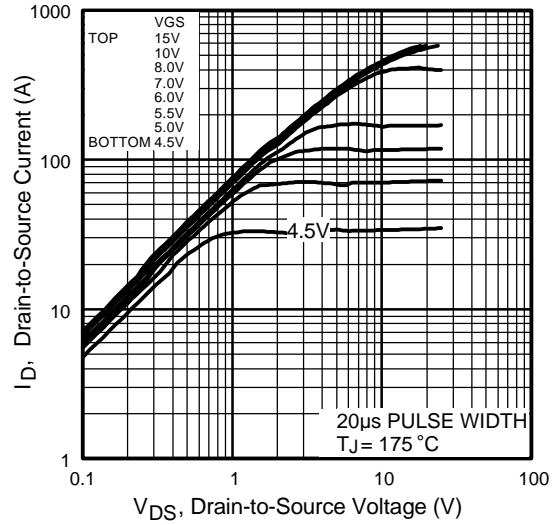


Fig 2. Typical Output Characteristics

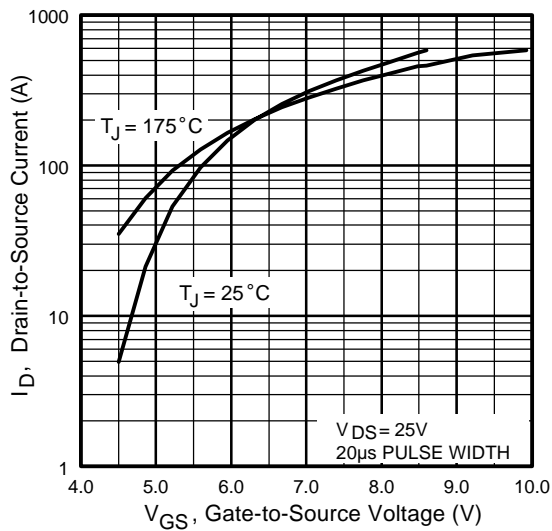


Fig 3. Typical Transfer Characteristics

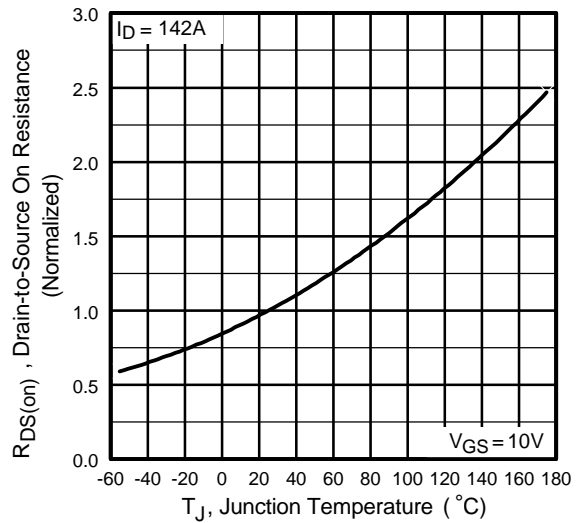


Fig 4. Normalized On-Resistance Vs. Temperature

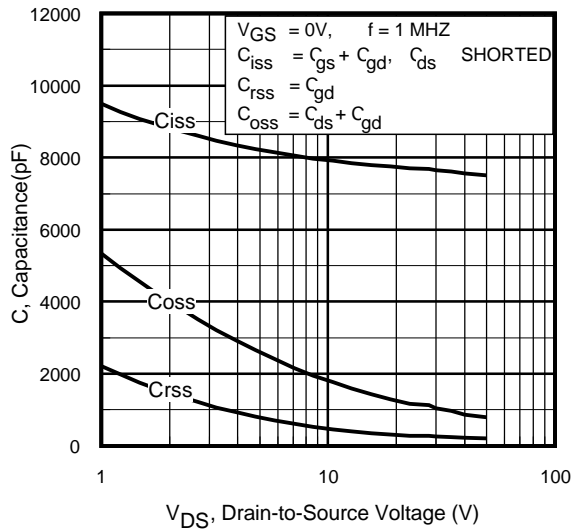


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

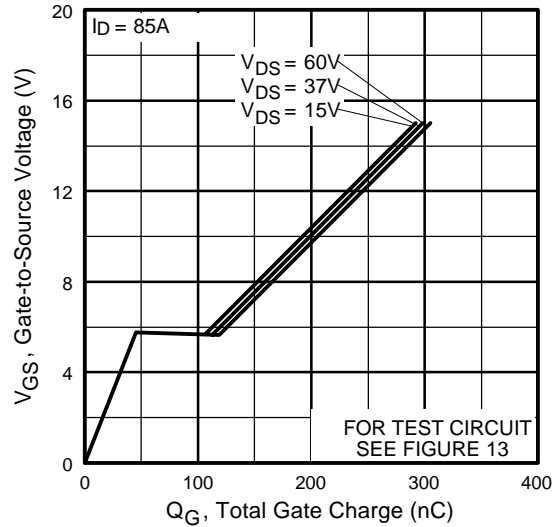


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

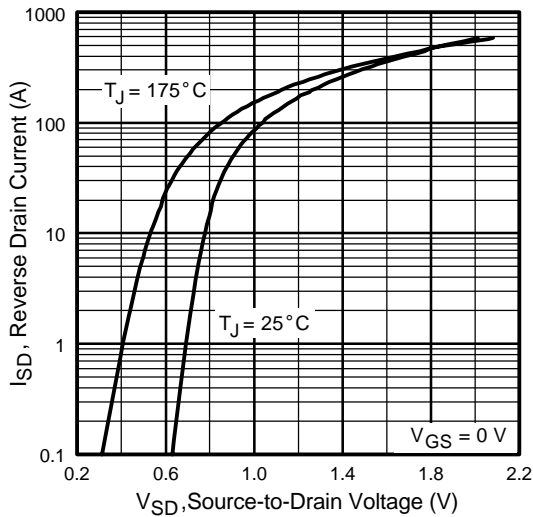


Fig 7. Typical Source-Drain Diode Forward Voltage

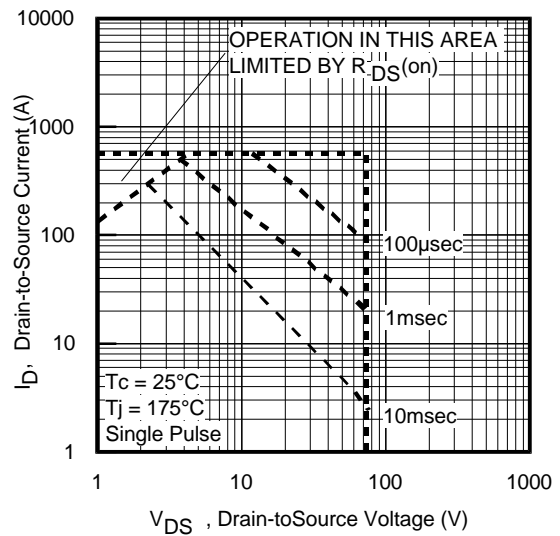


Fig 8. Maximum Safe Operating Area

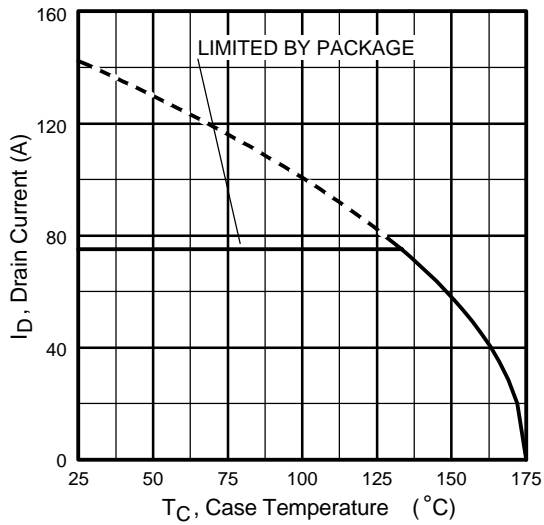


Fig 9. Maximum Drain Current Vs. Case Temperature

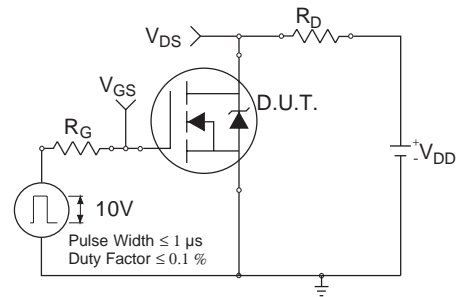


Fig 10a. Switching Time Test Circuit

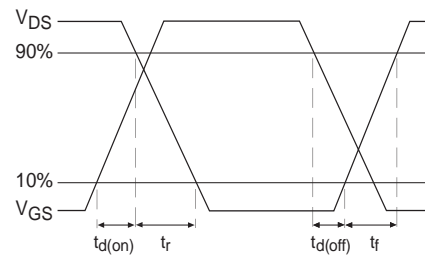


Fig 10b. Switching Time Waveforms

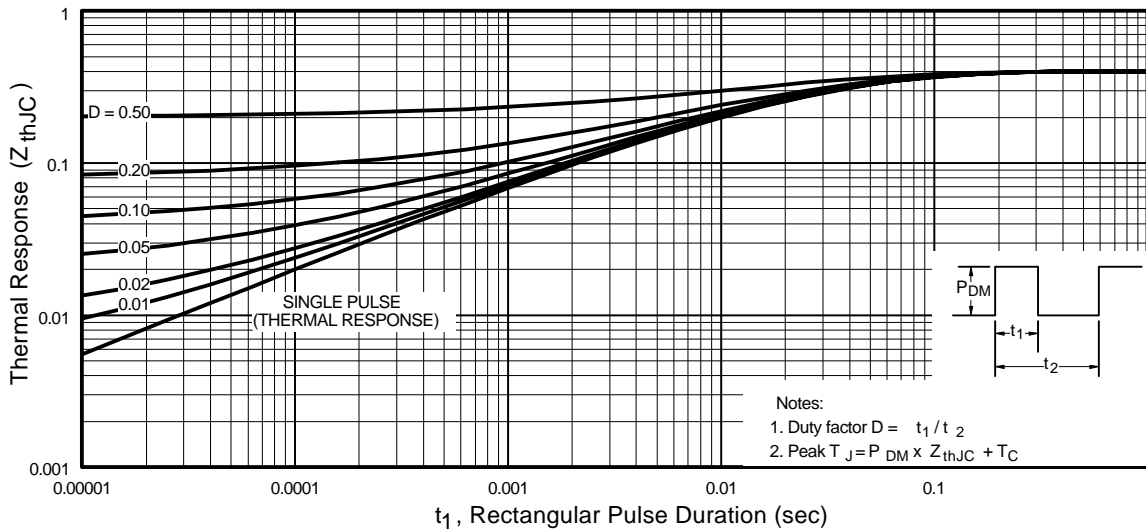


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRF1607

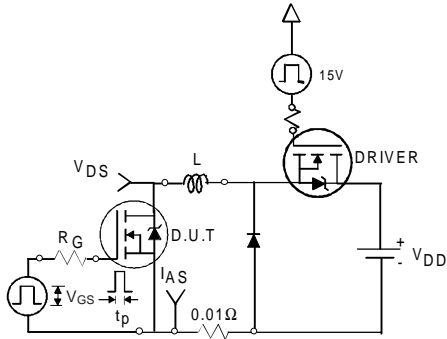


Fig 12a. Unclamped Inductive Test Circuit

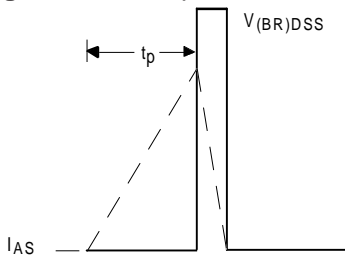


Fig 12b. Unclamped Inductive Waveforms

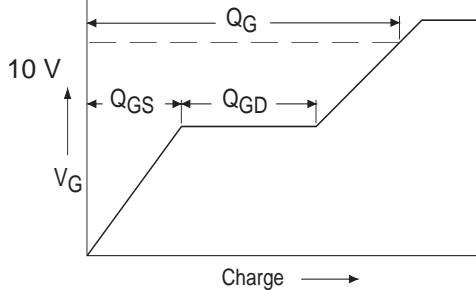


Fig 13a. Basic Gate Charge Waveform

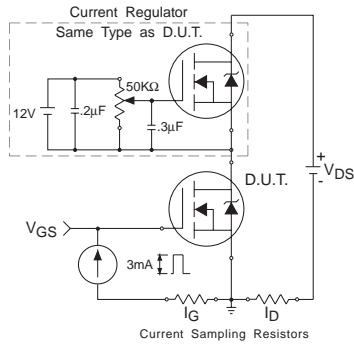


Fig 13b. Gate Charge Test Circuit

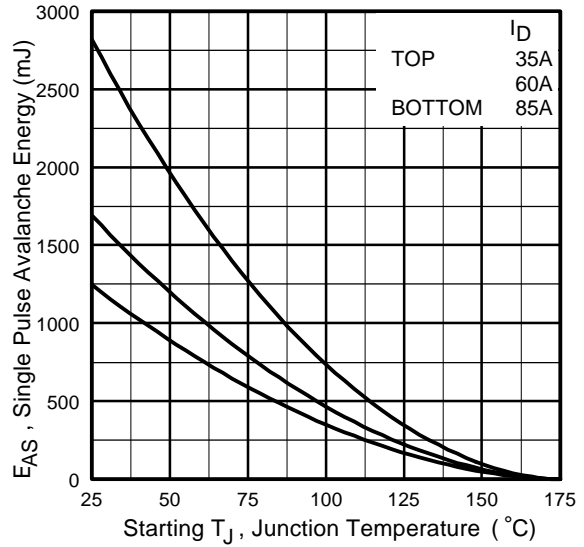


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

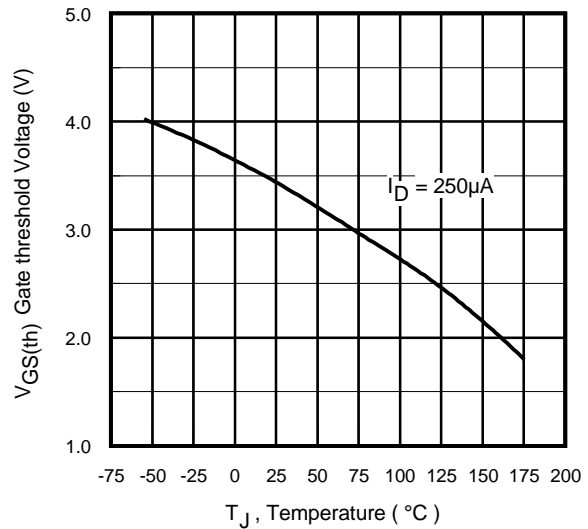


Fig 14. Threshold Voltage Vs. Temperature

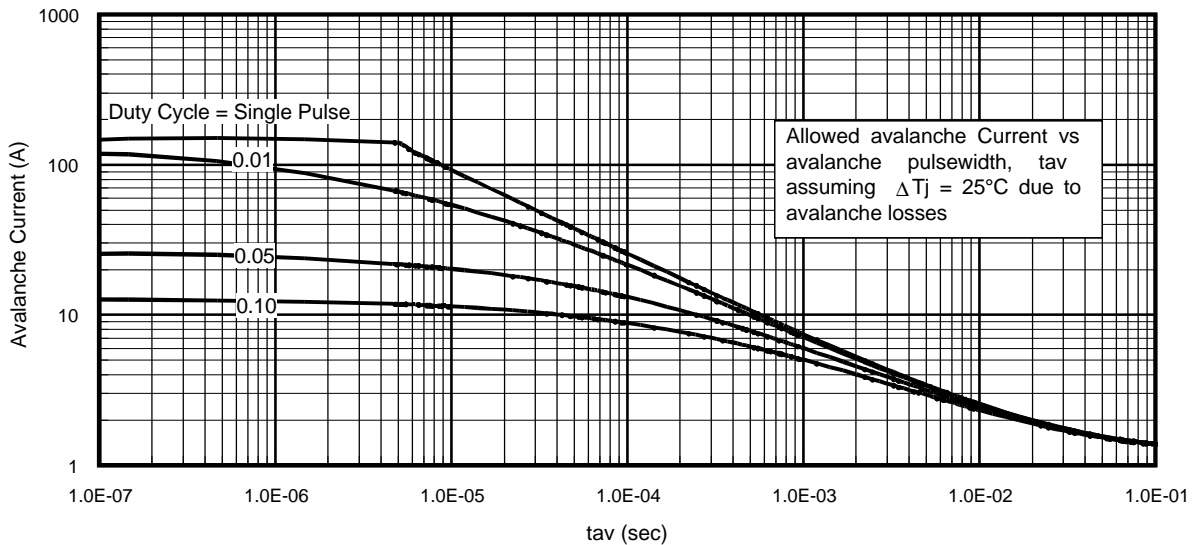


Fig 15. Typical Avalanche Current Vs.Pulsewidth

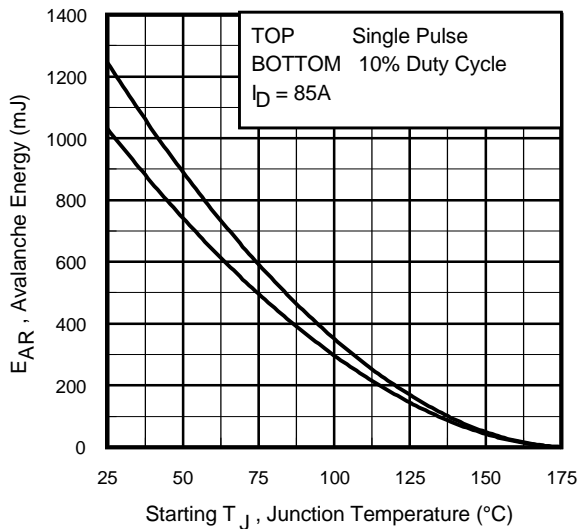


Fig 16. Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)**

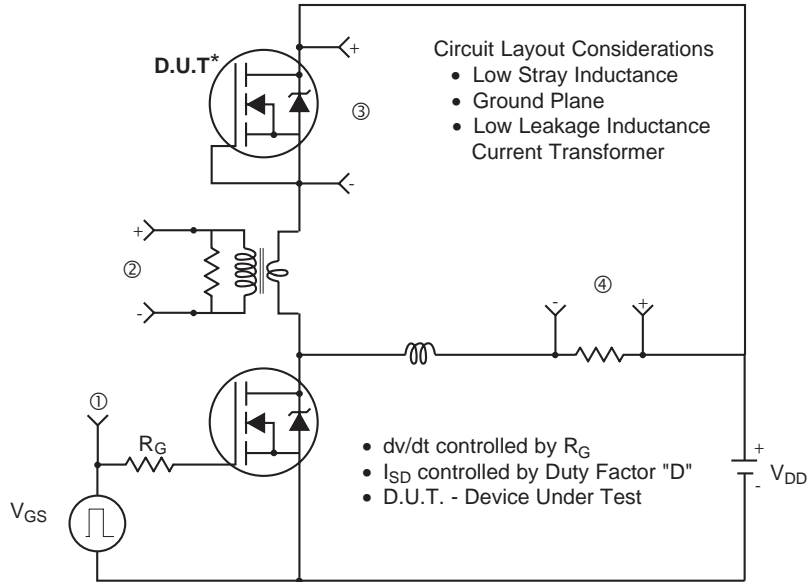
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

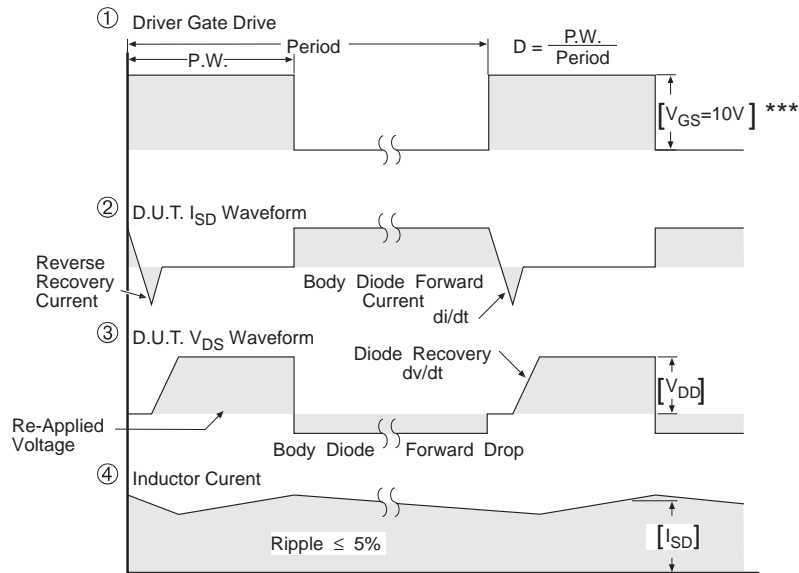
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



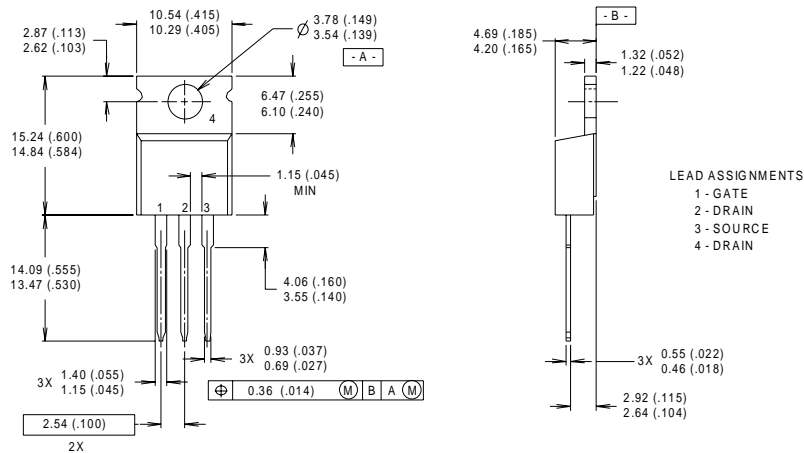
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

Package Outline

TO-220AB

Dimensions are shown in millimeters (inches)



NOTES:

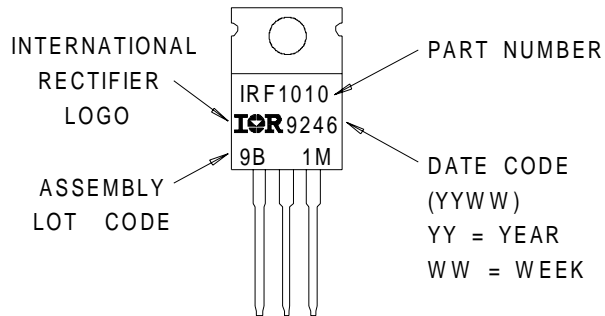
- 1 DIMENSIONING & TOLERANCING PER ANSII Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
 WITH ASSEMBLY
 LOT CODE 9B1M



Data and specifications subject to change without notice.
 This product has been designed and qualified for the Automotive [Q101] market.
 Qualification Standards can be found on IR's Web site.



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