HD14562B

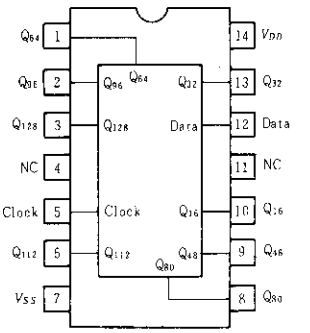
128-bit Static Shift Register

The HD14562B is a 128-bit static shift register. Data is clocked in and out of the shift register on the positive edge of the clock input. Data outputs are available every 16 bits, from 16 through bit 128.

■ FEATURES

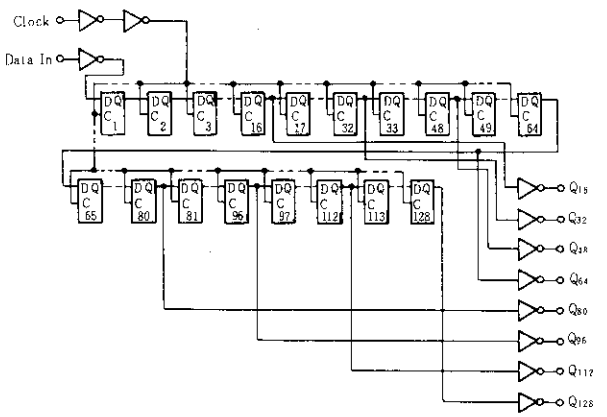
- Noise Immunity = 45% of V_{DD} typ.
- Single Supply Operation ... Positive or Negative
- Fully Static Operation
- Exceedingly Slow Input Transition Rates May Be Applied to the
- Clock Input
- 5.6MHz Operation @10V
- Cascadable to Provide Longer Shift Register Lengths ... 1.5MHz Operation @10V
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

■ PIN ARRANGEMENT

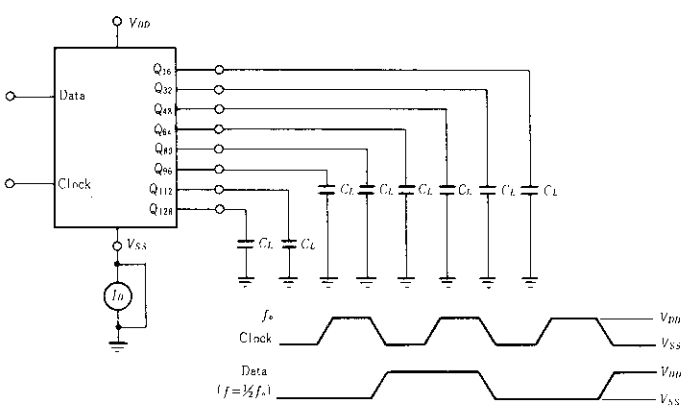


(Top View)

■ LOGIC DIAGRAM



■ POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

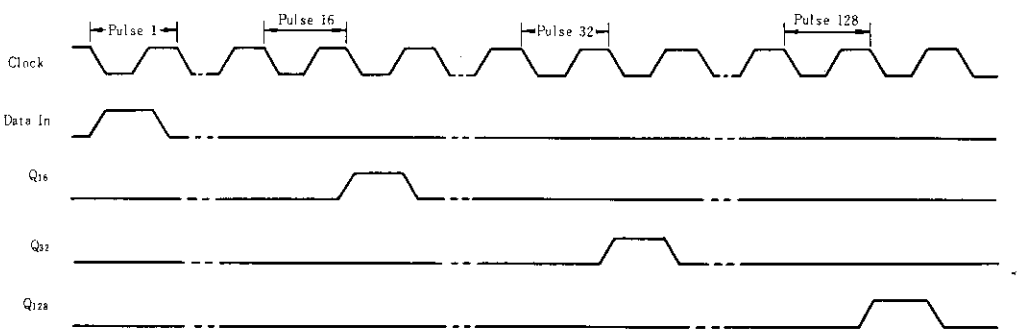


■ ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}(V)	Test Conditions	−40°C min	−40°C max	25°C min	25°C typ	25°C max	85°C min	85°C max	Unit
Output Voltage	V_{OL}	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	$V_{in}=0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out}=4.5$ or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out}=0.5$ or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	$V_{OH}=2.5$V	−1.0	—	−0.8	−1.7	—	−0.6	—	mA
		5.0	$V_{OH}=4.6$V	−0.2	—	−0.16	−0.36	—	−0.12	—	
		10	$V_{OH}=9.5$V	−0.5	—	−0.4	−0.9	—	−0.3	—	
		15	$V_{OH}=13.5$V	−1.4	—	−1.2	−3.5	—	−1.0	—	
	I_{OL}	5.0	$V_{OL}=0.4$V	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL}=0.5$V	1.3	—	1.1	2.25	—	0.9	—	
		15	$V_{OL}=1.5$V	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}		$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	50	—	0.010	50	—	375	μA
		10		—	100	—	0.020	100	—	750	
		15		—	200	—	0.030	200	—	1500	
Total Supply Current*	I_T	5.0	Dynamic+I_{DD}, per Gate C_L=50pF, f= 1 kHz	—	—	—	1.94	—	—	—	μA
		10		—	—	—	3.81	—	—	—	
		15		—	—	—	5.52	—	—	—	

* To calculate total supply current at frequency other than 1kHz.
@$V_{DD}=5.0$V $I_T=(1.94\,\mu A/kHz)f+I_{DD}$, @$V_{DD}=10$V $I_T=(3.81\,\mu A/kHz)f+I_{DD}$, @$V_{DD}=15$V $I_T=(5.52\,\mu A/kHz)f+I_{DD}$

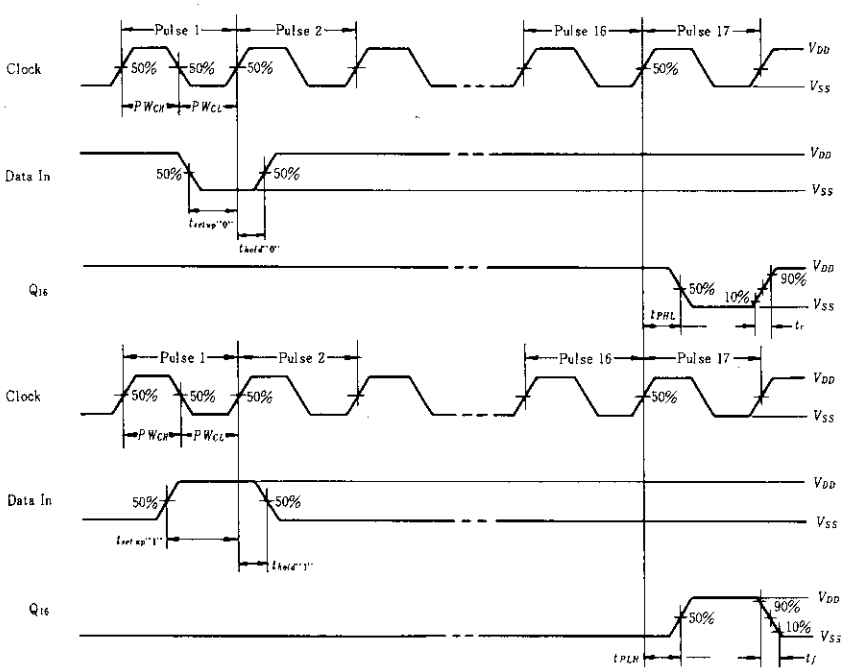
■ TIMING DIAGRAM



■ SWITCHING CHARACTERISTICS (C_L = 50pF, Ta = 25°C)

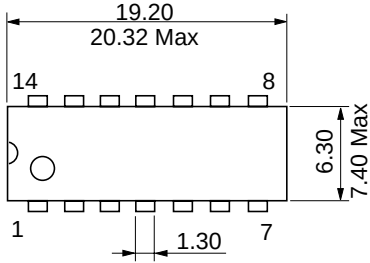
Characteristic	Symbol	V_{DD}(V)	min	typ	max	Unit
Output Rise Time	t_r	5.0	—	180	400	ns
		10	—	90	200	
		15	—	65	160	
Output Fall Time	t_f	5.0	—	100	200	ns
		10	—	50	100	
		15	—	37	80	
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0	—	600	1500	ns
		10	—	250	660	
		15	—	170	500	
Clock Pulse Width	PW_C	5.0	900	300	—	ns
		10	330	110	—	
		15	250	75	—	
Clock Frequency	PRF	5.0	—	1.9	0.8	MHz
		10	—	5.6	1.5	
		15	—	8.0	2.0	
Setup Time	t_{setup} "1"	5.0	−20	−170	—	ns
		10	−10	−64	—	
		15	0	−60	—	
	t_{setup} "0"	5.0	−20	−91	—	ns
		10	−10	−58	—	
		15	0	−40	—	
Hold Time	t_{hold} "1"	5.0	350	263	—	ns
		10	165	109	—	
		15	155	100	—	
	t_{hold} "0"	5.0	350	267	—	ns
		10	200	140	—	
		15	140	93	—	

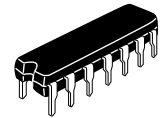
●AC Test Waveform

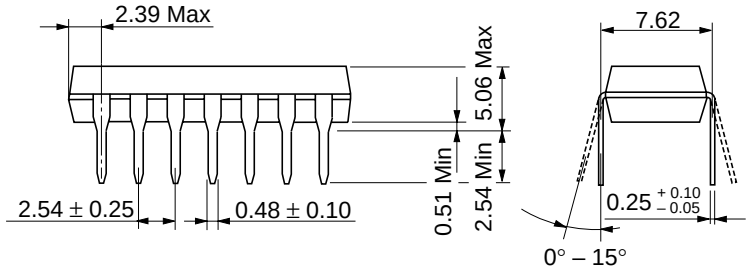


Note) The remaining Data-Bit Outputs (Q_{32}, Q_{48}, Q_{64}, Q_{80}, Q_{96}, Q_{112} and Q_{128}) will occur at Clock Pulse 32, 48, 64, 80, 96, 112, 128 in the same relationship as Q_{16}.

Unit: mm







Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

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