

HD14522B, HD14526B

Programmable Divide-by-N 4-bit Counter

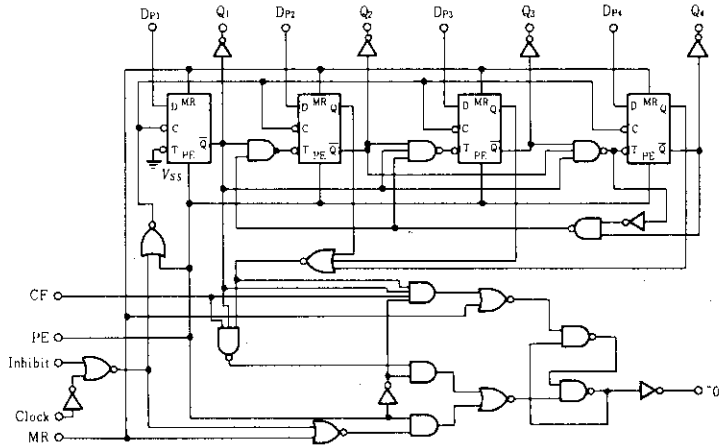
The HD14522B BCD counter and the HD14526B binary counter are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Clock Inhibit input allows disabling low power dissipation and/or high noise immunity.

FEATURES

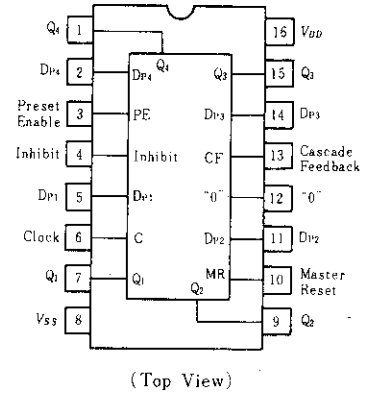
- Quiescent Current=5nA/pkg typ. @5V
- Supply Voltage Range=3 to 18V
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-clocked Design . . . Incremented on Positive transition of Clock or Negative Transition of Clock Inhibit
- 5MHz Counting Rate
- Asynchronous Preset Enable
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

LOGIC DIAGRAM

HD14522B



PIN ARRANGEMENT



TRUTH TABLE

Both Types

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
	0	0	0	Count 1
x	1	0	0	No Count
1		0	0	Count 1
x	x	1	0	Preset
x	x	x	1	Reset

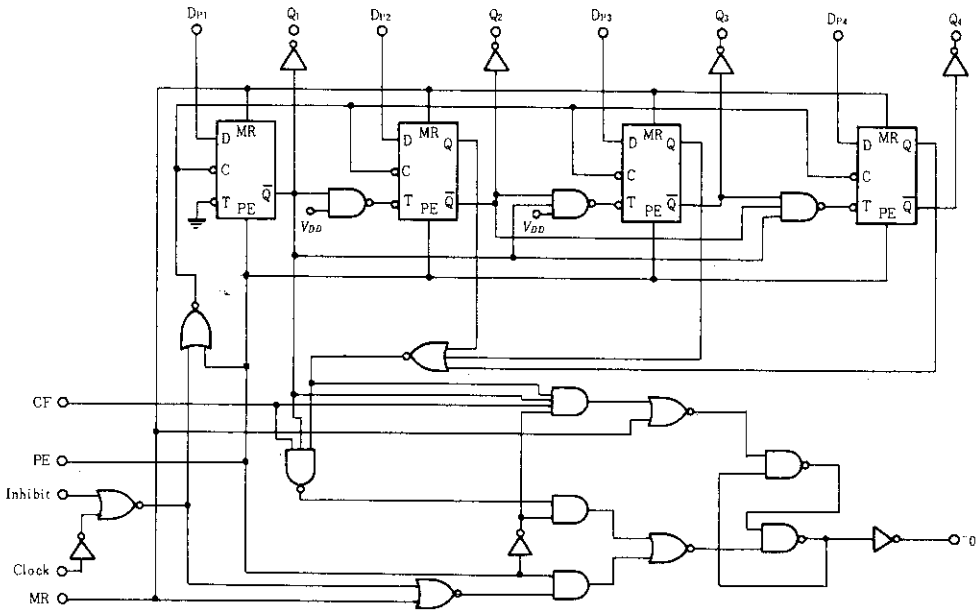
HD14522B

Count	Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

HD14526B

Count	Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

●HD14526B



■ ELECTRICAL CHARACTERISTICS

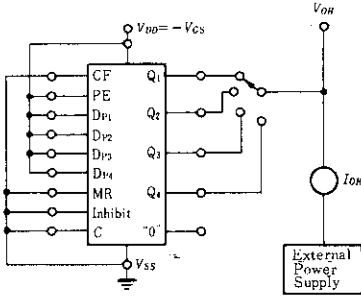
Characteristic	Symbol	V _{DD} (V)	Test Conditions	-40°C		25°C			85°C		Unit
				min	max	min	typ	max	min	max	
Output Voltage	V _{OL}	5.0	V _{in} = V _{DD} or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V _{OH}	5.0	V _{in} = 0 or V _{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V _{IL}	5.0	V _{ext} = 4.5 or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
		10	V _{ext} = 9.0 or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
		15	V _{ext} = 13.5 or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	V _{IH}	5.0	V _{ext} = 0.5 or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
		10	V _{ext} = 1.0 or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
		15	V _{ext} = 1.5 or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I _{OH}	5.0	V _{OH} = 2.5V	-1.0	—	-0.8	-1.7	—	-0.6	—	mA
		5.0	V _{OH} = 4.6V	-0.2	—	-0.16	-0.36	—	-0.12	—	
		10	V _{OH} = 9.5V	-0.5	—	-0.4	-0.9	—	-0.3	—	
		15	V _{OH} = 13.5V	-1.4	—	-1.2	-3.5	—	-1.0	—	
	I _{OL}	5.0	V _{OL} = 0.4V	0.52	—	0.44	0.88	—	0.36	—	mA
		10	V _{OL} = 0.5V	1.3	—	1.1	2.25	—	0.9	—	
15		V _{OL} = 1.5V	3.6	—	3.0	8.8	—	2.4	—		
Input Current	I _{in}	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C _{in}	—	V _{in} = 0	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I _{DD}	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	μA
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	I _T	5.0	Dynamic + I _{DD} , per Gate C _L = 50 pF, f = 1 kHz	—	—	—	1.7	—	—	—	μA
		10		—	—	—	3.4	—	—	—	
		15		—	—	—	5.1	—	—	—	

* To calculate total supply current at frequency other than 1kHz.

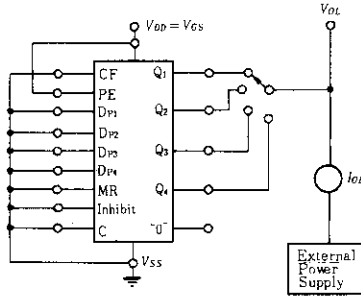
@V_{DD} = 5.0V I_T = (1.7 μA/kHz)f + I_{DD}, @V_{DD} = 10V I_T = (3.4 μA/kHz)f + I_{DD}, @V_{DD} = 15V I_T = (5.1 μA/kHz)f + I_{DD}

■ DC CHARACTERISTIC TEST CIRCUIT

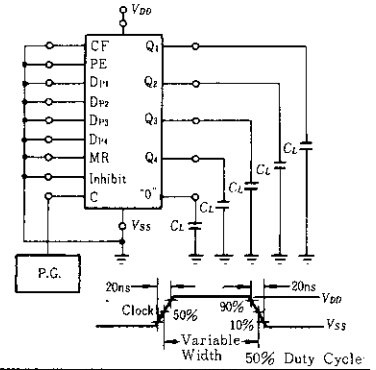
● I_{OH}



● I_{OL}



● POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

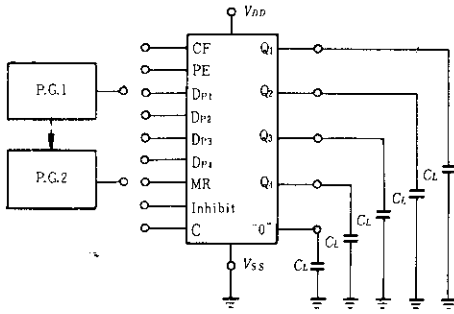


■ SWITCHING CHARACTERISTICS (C_L = 50 pF, T_a = 25 °C)

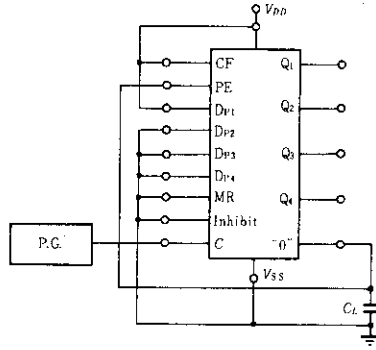
Characteristic		Symbol	V _{DD} (V)	min	typ	max	Unit
Output Rise Time		t _r	5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	160	
Output Fall Time		t _f	5.0	—	100	200	ns
			10	—	50	100	
			15	—	37	80	
Propagation Delay Time	Q Outputs	t _{PLH}	5.0	—	550	1100	ns
			10	—	230	450	
			15	—	160	340	
	"0" Outputs	t _{PHL}	5.0	—	240	500	
			10	—	120	300	
			15	—	90	225	
Clock Pulse Width		PW _C	5.0	300	100	—	ns
			10	150	50	—	
			15	115	40	—	
Clock Frequency		PRF	5.0	—	2.0	1.0	MHz
			10	—	5.0	2.5	
			15	—	6.6	3.0	
Maximum Clock or Inhibit Rise and Fall Time		t _r , t _f	5.0	—	—	15	μs
			10	—	—	15	
			15	—	—	15	
Hold Time		t _{hold}	5.0	150	75	—	ns
			10	75	25	—	
			15	60	20	—	
Minimum Preset Enable Pulse Width		PW _{PE}	5.0	300	100	—	ns
			10	150	50	—	
			15	115	40	—	
Minimum Master Reset Pulse Width		PW _{MR}	5.0	350	200	—	ns
			10	300	100	—	
			15	225	75	—	

■ SWITCHING TIME TEST CIRCUIT

● Test No. 1 ~ 6

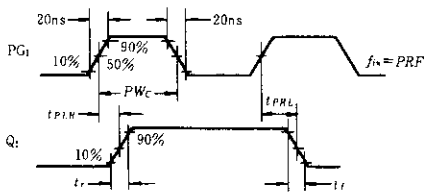


● Test No. 7

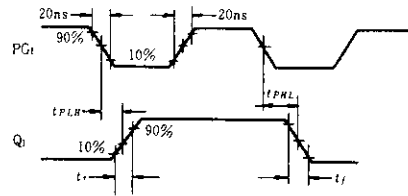


■ AC TEST METHOD AND SWITCHING WAVEFORMS

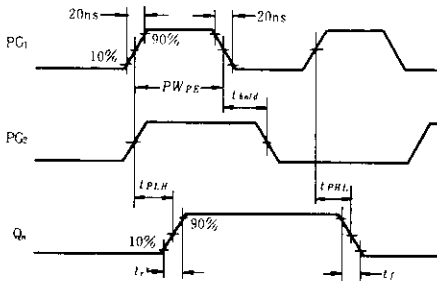
● Test No. 1



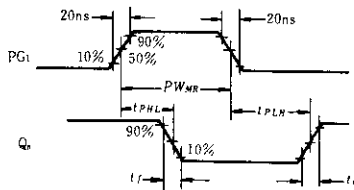
● Test No. 2



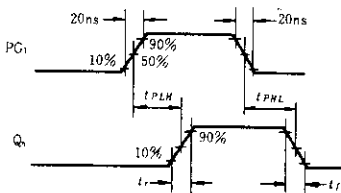
● Test No. 3



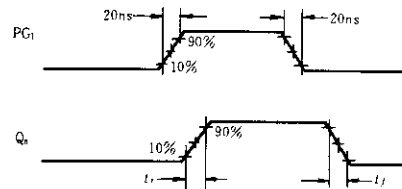
● Test No. 4



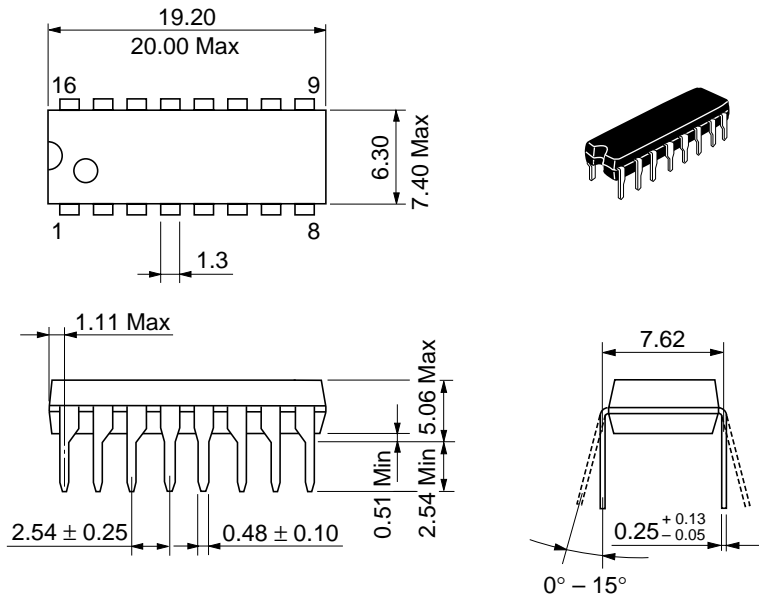
● Test No. 5 & 7



● Test No. 6



Characteristic	Test No.	Clock	Inhibit	PE	MR	D _{0n}	CF	Output
<i>t_r</i> , <i>t_f</i> , <i>t_{PLH}</i> , <i>t_{PHL}</i>	1	PG ₁	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	Q ₁
	2	V _{DD}	PG ₁	V _{SS}	V _{SS}	V _{SS}	V _{SS}	Q ₁
	3	V _{SS}	V _{SS}	PG ₁	V _{SS}	PG ₂	V _{SS}	Q _n
	4	V _{SS}	V _{SS}	V _{DD}	PG ₁	V _{DD}	V _{SS}	Q _n
	5	V _{SS}	V _{SS}	V _{DD}	V _{SS}	PG ₁	V _{SS}	Q _n
<i>PW_{MR}</i>	4	V _{SS}	V _{SS}	V _{DD}	PG ₁	V _{DD}	V _{SS}	Q _n
<i>PW_{PE}</i>	3	V _{SS}	V _{SS}	PG ₁	V _{SS}	PG ₂	V _{SS}	Q _n
<i>PW_C</i>	1	PG ₁	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	Q ₁
<i>PRF</i>	1	PG ₁	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	Q ₁
<i>t_{hold}</i>	3	V _{SS}	V _{SS}	PG ₁	V _{SS}	PG ₂	V _{SS}	Q _n
<i>t_r</i> , <i>t_f</i>	6	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{SS}	PG ₁	"0"
<i>t_{PLH}</i> , <i>t_{PHL}</i>	7	PG	V _{SS}	See Test Circuit	V _{SS}	See Test Circuit	V _{DD}	"0"



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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