

# HD14506B

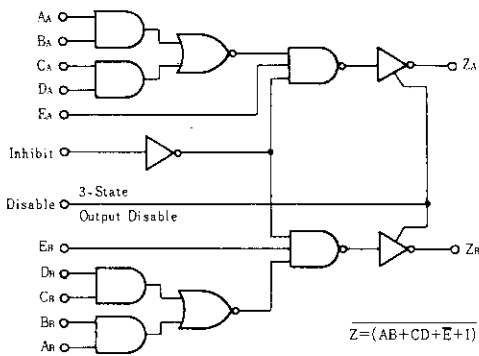
## Dual 2-wide 2-input Expandable AND-OR-INVERT Gate

The HD14506B is an expandable AND-OR-INVERT gate with inhibit and 3-state output. The expand option allows cascading with any other gate, which may be carried as far as desired as long as the propagation delay added with each gate is considered. For example, the second AOI gate in this device may be used to expand the first gate, giving an expanded 4-wide, 2-input AOI gate. This device is useful in data control and digital multiplexing applications.

### FEATURES

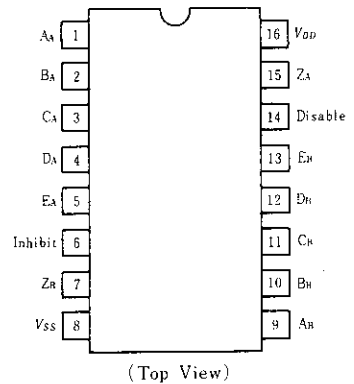
- Quiescent Current = 2nA/pkg typ. @5V
- 3-state Output
- Separate Inhibit Line
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

### LOGIC DIAGRAM



$$Z = (AB + CD + E + I)$$

### PIN ARRANGEMENT



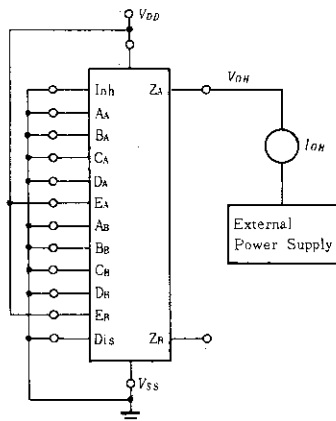
### TRUTH TABLE

A	B	C	D	E	Inhibit	Disable	Z
0	0	0	0	1	0	0	1
0	x	0	x	1	0	0	1
0	x	x	0	1	0	0	1
x	0	0	x	1	0	0	1
x	0	x	0	1	0	0	1
1	1	x	x	x	x	0	0
x	x	1	1	x	x	0	0
x	x	x	x	0	x	0	0
x	x	x	x	x	1	0	0
x	x	x	x	x	x	1	High Impedance

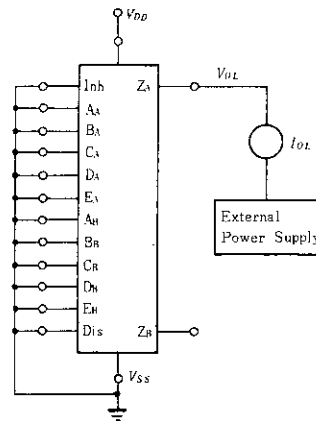
x=Don't Care

### DC CHARACTERISTIC TEST CIRCUIT

•  $I_{OH}$



•  $I_{OL}$



**■ ELECTRICAL CHARACTERISTICS**

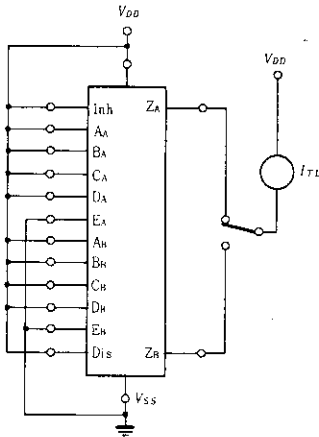
Characteristic	Symbol	$V_{DD}(V)$	Test Conditions	-40°C		25°C			85°C		Unit
				min	max	min	typ	max	min	max	
Output Voltage	$V_{OL}$	5.0	$V_{in} = V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	$V_{OH}$	5.0	$V_{in} = 0$ or $V_{DD}$	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	$V_{IL}$	5.0	$V_{out} = 4.5$ or $0.5V$	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out} = 9.0$ or $1.0V$	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out} = 13.5$ or $1.5V$	—	4.0	—	6.75	4.0	—	4.0	
	$V_{IH}$	5.0	$V_{out} = 0.5$ or $4.5V$	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out} = 1.0$ or $9.0V$	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out} = 1.5$ or $13.5V$	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	$I_{OH}$	5.0	$V_{OH} = 2.5V$	-1.0	—	-0.8	-1.7	—	-0.6	—	mA
		5.0	$V_{OH} = 4.6V$	-0.2	—	-0.16	-0.36	—	-0.12	—	
		10	$V_{OH} = 9.5V$	-0.5	—	-0.4	-0.9	—	-0.3	—	
		15	$V_{OH} = 13.5V$	-1.4	—	-1.2	-3.5	—	-1.0	—	
	$I_{OL}$	5.0	$V_{OL} = 0.4V$	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL} = 0.5V$	1.3	—	1.1	2.25	—	0.9	—	
15		$V_{OL} = 1.5V$	3.6	—	3.0	8.8	—	2.4	—		
Input Current	$I_{in}$	15		—	$\pm 0.3$	—	$\pm 0.0001$	$\pm 0.3$	—	$\pm 1.0$	$\mu A$
Input Capacitance	$C_{in}$		$V_{in} = 0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	$I_{DD}$	5.0	Zero Signal, Per Package	—	4.0	—	0.002	4.0	—	30	$\mu A$
		10		—	8.0	—	0.004	8.0	—	60	
		15		—	16	—	0.006	16	—	120	
Total Supply Current*	$I_T$	5.0	Dynamic + $I_{DD}$	—	—	—	0.6	—	—	—	$\mu A$
		10	Per Gate	—	—	—	1.1	—	—	—	
		15	$C_L = 50pF, f = 1kHz$	—	—	—	1.7	—	—	—	
Three-State Output Leakage Current	$I_{TL}$	15		—	$\pm 1.0$	—	$\pm 0.0001$	$\pm 1.0$	—	$\pm 7.5$	$\mu A$

\* To calculate total supply current at frequency other than 1kHz.

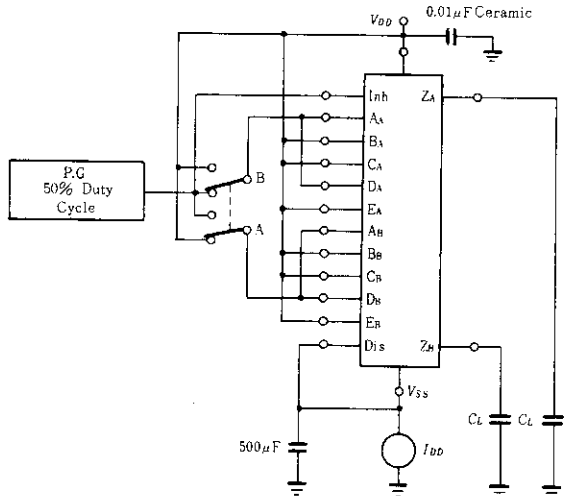
@  $V_{DD} = 5.0V$   $I_T = (0.6\mu A/kHz) f + I_{DD}$ . @  $V_{DD} = 10V$   $I_T = (1.1\mu A/kHz) f + I_{DD}$ . @  $V_{DD} = 15V$   $I_T = (1.7\mu A/kHz) f + I_{DD}$

**■ DC CHARACTERISTIC TEST CIRCUIT**

●  $I_{TL}$



**■ POWER DISSIPATION TEST CIRCUIT**

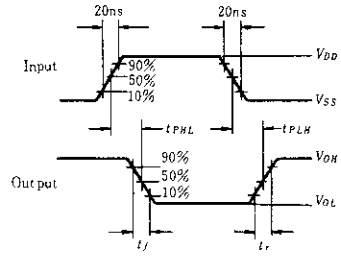
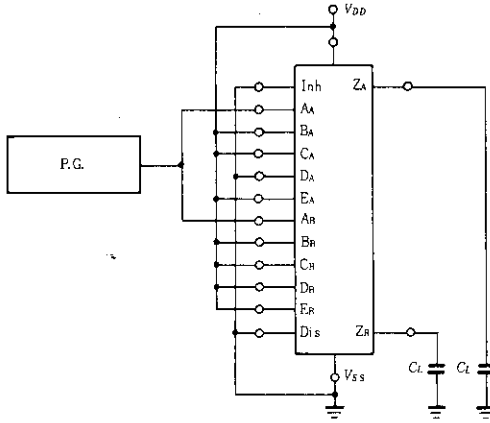


**SWITCHING CHARACTERISTICS** ( $C_L=50\text{pF}$ ,  $T_a=25^\circ\text{C}$ )

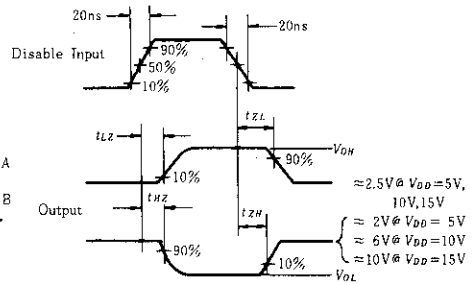
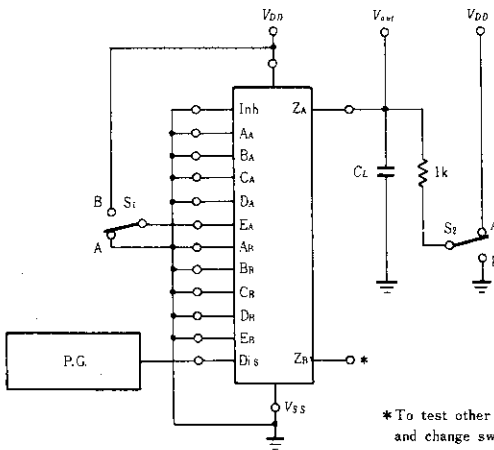
Characteristic		Symbol	$V_{DD}$ (V)	min	typ	max	Unit
Output Rise Time		$t_r$	5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	160	
Output Fall Time		$t_f$	5.0	—	100	200	ns
			10	—	50	100	
			15	—	37	80	
Propagation Delay Time	Data	$t_{PLH}$	5.0	—	295	580	ns
			10	—	110	225	
			15	—	75	180	
		$t_{PHL}$	5.0	—	270	480	ns
			10	—	95	175	
			15	—	65	140	
	Expand	$t_{PLH}$	5.0	—	180	430	ns
			10	—	75	160	
			15	—	50	125	
		$t_{PHL}$	5.0	—	200	330	ns
			10	—	80	110	
			15	—	55	90	
	Inhibit	$t_{PLH}$	5.0	—	220	500	ns
			10	—	100	225	
			15	—	65	160	
$t_{PHL}$		5.0	—	230	400	ns	
		10	—	95	175		
		15	—	60	150		
Output Disable Time	$t_{HZ}$	5.0	—	60	150	ns	
		10	—	45	110		
		15	—	35	90		
	$t_{LZ}$	5.0	—	90	225	ns	
		10	—	55	140		
		15	—	40	100		
Output Enable Time	$t_{ZH}$	5.0	—	110	300	ns	
		10	—	50	125		
		15	—	40	100		
	$t_{ZL}$	5.0	—	170	425	ns	
		10	—	70	175		
		15	—	50	125		

■ SWITCHING TIME TEST CIRCUIT

●  $t_{PLH}$ ,  $t_{PHL}$



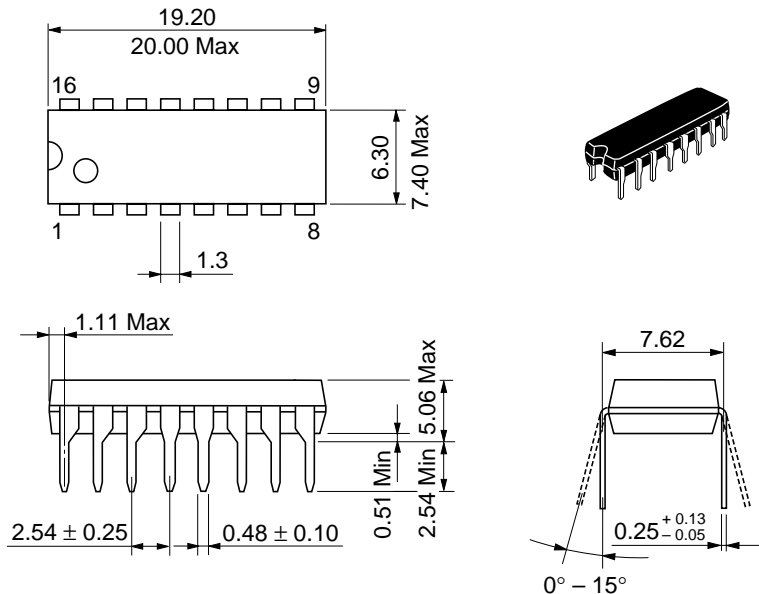
●  $t_{HZ}$ ,  $t_{LZ}$ ,  $t_{ZH}$ ,  $t_{ZL}$



\*To test other side of circuit connect to this output and change switch(S1) to other expand input (E)

Switch Positions

Test	S <sub>1</sub>	S <sub>2</sub>
$t_{LZ}$	A	A
$t_{HZ}$	B	B
$t_{ZL}$	A	A
$t_{ZH}$	B	B



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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