

HD14022B

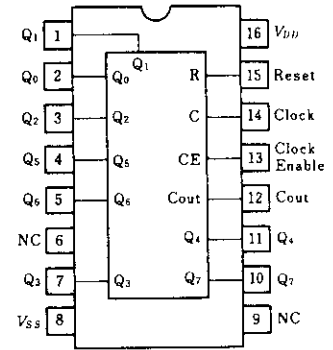
Octal Counter/Divider

The HD14022B is a four-stage Johnson octal counter with built-in code converter. High speed operation and spike-free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

FEATURES

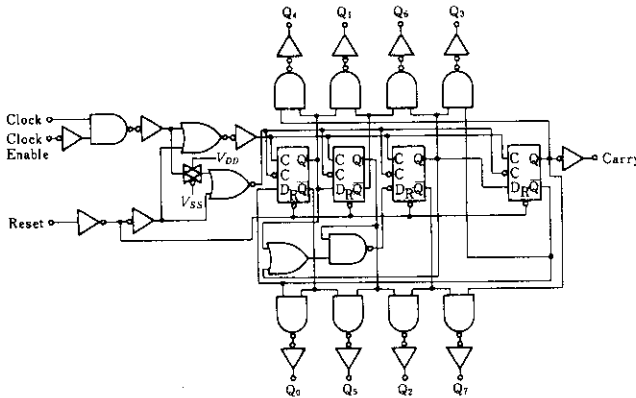
- Quiescent Current = 5nA/pkg typ. @5V
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4022B and HD14022B

PIN ARRANGEMENT



(Top View)

LOGIC DIAGRAM

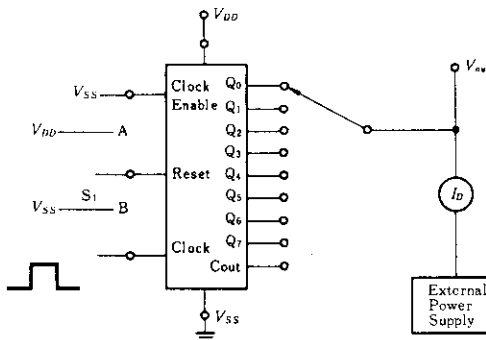


TRUTH TABLE

Clock	Clock Enable	Reset	Output n
L	x	L	n
x	H	L	n
↗	L	L	n + 1
↘	x	L	n
H	↗	L	n + 1
x	↘	L	n
x	x	H	Q ₀

x : Don't Care
 n < 4... Carry = H
 n ≥ 4... Carry = L

Typical Output Source and Output Sink Characteristics Test Circuit



	I_{OL}	I_{OH}
Outputs	(S ₁ → A)	Clock to desired Output (S ₁ to B)
Carry	Clock to Q ₅ thru Q ₇ (S ₁ to B)	S ₁ → A
V _{CS}	V _{DD}	-V _{DD}
V _{DS}	V _{ext}	V _{ext} - V _{DD}

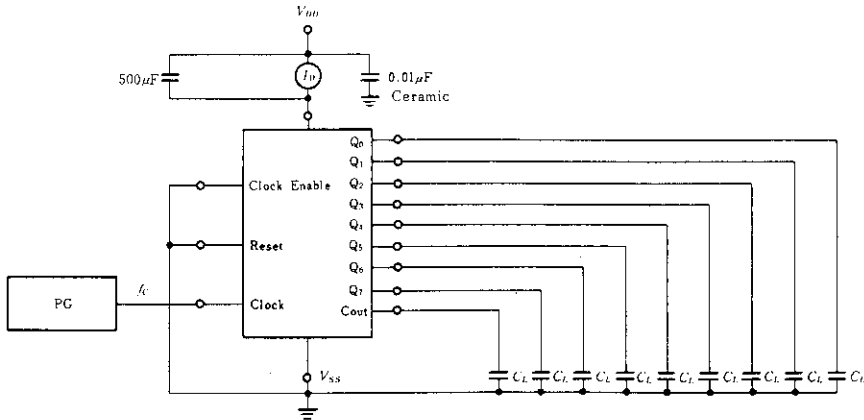
■ ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD} (V)	Test Conditions	-40°C		25°C			85°C		Unit
				min	max	min	typ	max	min	max	
Output Voltage	V _{OL}	5.0	V _{in} = V _{DD} or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V _{OH}	5.0	V _{in} = 0 or V _{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V _{IL}	5.0	V _{out} = 4.5 or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
		10	V _{out} = 9.0 or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
		15	V _{out} = 13.5 or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	V _{IH}	5.0	V _{out} = 0.5 or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
		10	V _{out} = 1.0 or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
		15	V _{out} = 1.5 or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I _{OH}	5.0	V _{OH} = 2.5V	-1.0	—	-0.8	-1.7	—	-0.6	—	mA
		5.0	V _{OH} = 4.6V	-0.2	—	-0.16	-0.36	—	-0.12	—	
		10	V _{OH} = 9.5V	-0.5	—	-0.4	-0.9	—	-0.3	—	
		15	V _{OH} = 13.5V	-1.4	—	-1.2	-3.5	—	-1.0	—	
	I _{OL}	5.0	V _{OL} = 0.4V	0.52	—	0.44	0.88	—	0.36	—	mA
		10	V _{OL} = 0.5V	1.3	—	1.1	2.25	—	0.9	—	
15		V _{OL} = 1.5V	3.6	—	3.0	8.8	—	2.4	—		
Input Current	I _n	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C _{in}		V _{in} = 0	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I _{DD}	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	μA
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	I _T	5.0	Dynamic + I _{DD} , per Gate, C _L = 50pF, f = 1 kHz	—	—	—	0.28	—	—	—	μA
		10		—	—	—	0.56	—	—	—	
		15		—	—	—	0.85	—	—	—	

* To calculate total supply current at frequency other than 1kHz.

@ V_{DD} = 5.0V I_T = (0.28μA/kHz)f + I_{DD}, @ V_{DD} = 10V I_T = (0.56μA/kHz)f + I_{DD}, @ V_{DD} = 15V I_T = (0.85μA/kHz)f + I_{DD}.

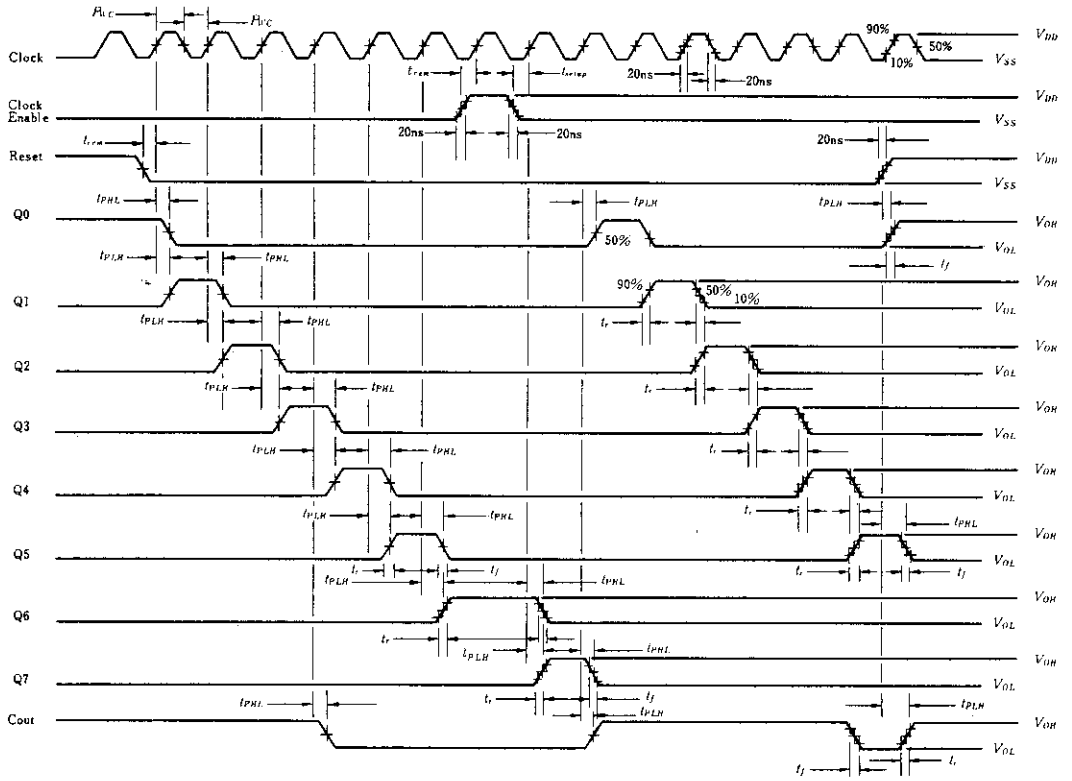
■ POWER DISSIPATION TEST CIRCUIT

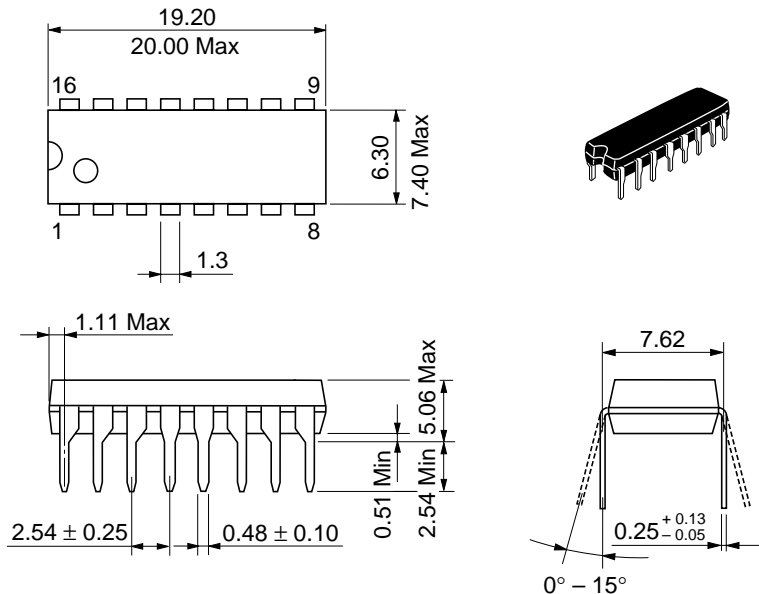


SWITCHING CHARACTERISTICS ($C_L = 50\text{pF}$, $T_a = 25^\circ\text{C}$)

Characteristic		Symbol	V_{DD} (V)	min	typ	max	Unit
Output Rise Time		t_r	5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	160	
Output Fall Time		t_f	5.0	—	100	200	ns
			10	—	50	100	
			15	—	37	80	
Propagation Delay Time	Reset to Decode Out	t_{PLH} t_{PHL}	5.0	—	500	1000	ns
			10	—	230	460	
			15	—	140	350	
	Clock to Cout		5.0	—	400	800	
			10	—	150	350	
			15	—	100	250	
	Clock to Decode Out	5.0	—	500	1000		
		10	—	230	460		
		15	—	140	350		
	Reset to Cout	t_{PLH}	5.0	—	400	800	
			10	—	150	350	
			15	—	100	250	
Clock Pulse Width	PW_C	5.0	250	100	—	ns	
		10	100	42	—		
		15	75	30	—		
Clock Frequency	PRF	5.0	—	5.0	2.0	MHz	
		10	—	12	5.0		
		15	—	16	6.7		
Reset Pulse Width	PW_R	5.0	500	200	—	ns	
		10	250	100	—		
		15	190	75	—		
Reset Removal Time	t_{rem}	5.0	750	300	—	ns	
		10	275	100	—		
		15	210	80	—		
Clock Pulse Rise and Fall Time	t_r, t_f	5.0	No Limit				
		10					
		15					
Clock Enable Setup Time	t_{setup}	5.0	700	175	—	ns	
		10	300	75	—		
		15	225	52	—		
Clock Enable Removal Time	t_{rem}	5.0	700	260	—	ns	
		10	300	100	—		
		15	225	70	—		

■ DYNAMIC SIGNAL WAVEFORMS





Hitachi Code	DP-16
JEDEC	Conforms
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Weight (reference value)	1.07 g

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