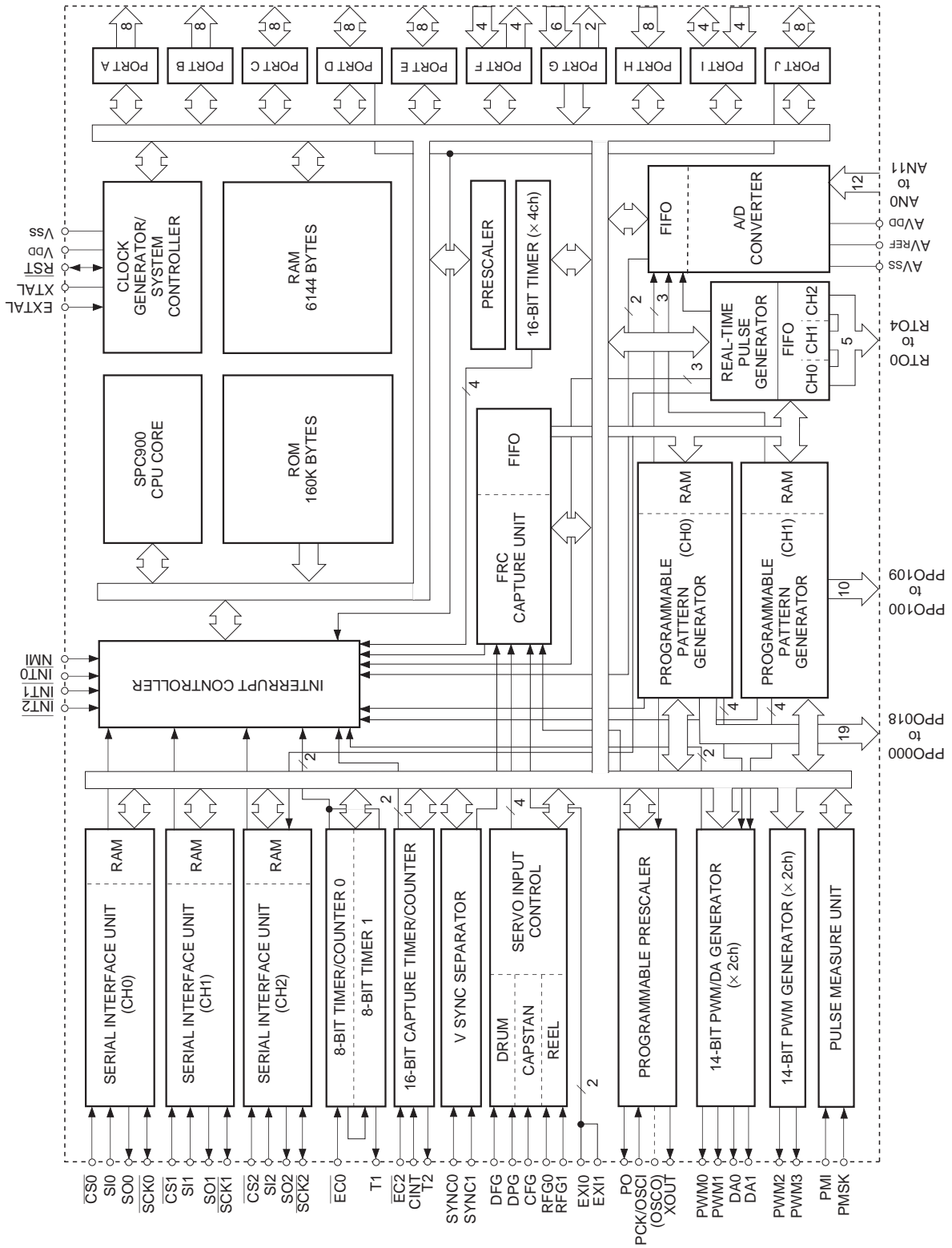
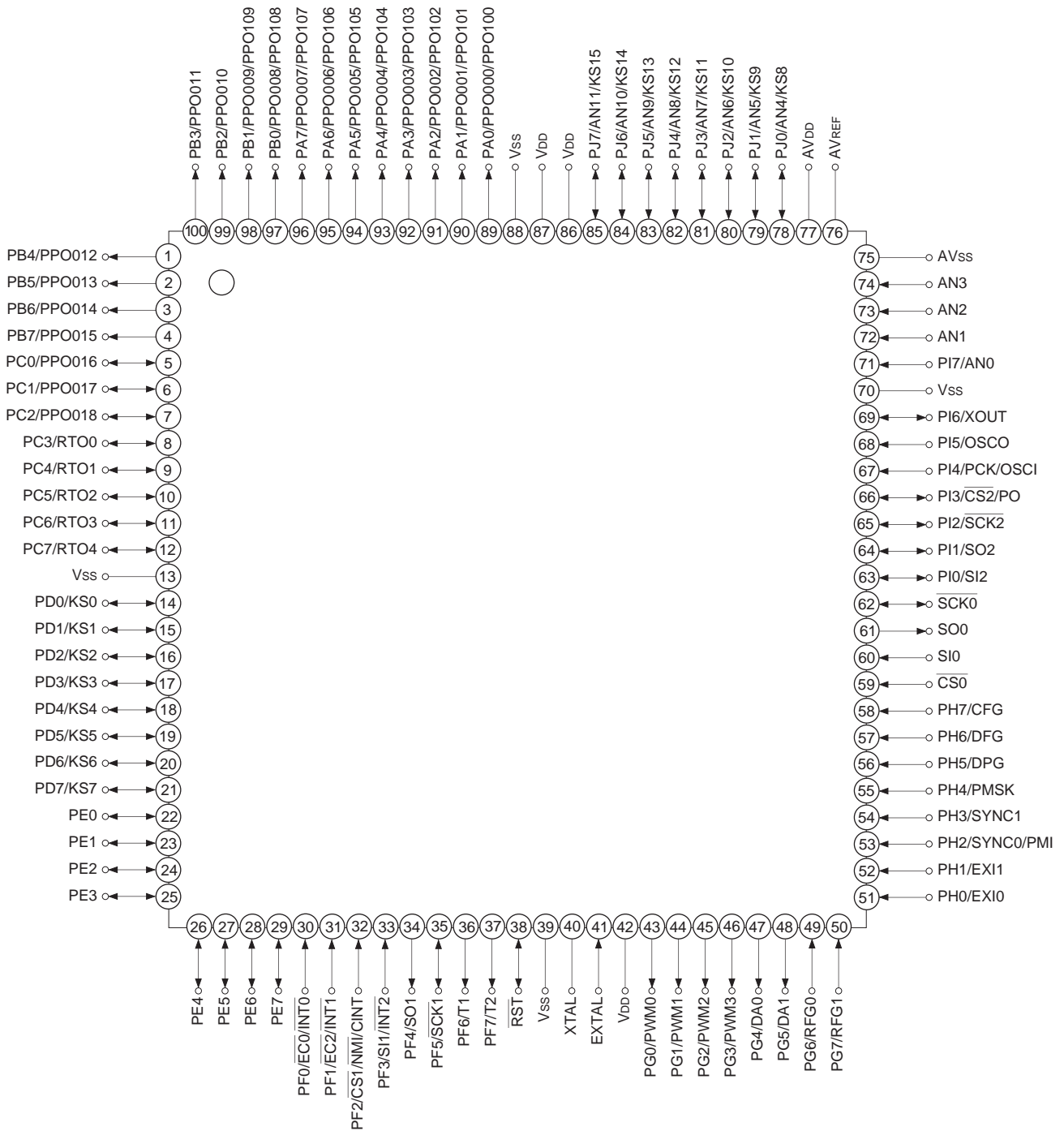




Block Diagram



Pin Configuration (Top View)



**Note)** 1. Vss (Pins 13, 39, 70 and 88) must be connected to GND.  
 2. VDD (Pins 42, 86 and 87) must be connected to VDD.

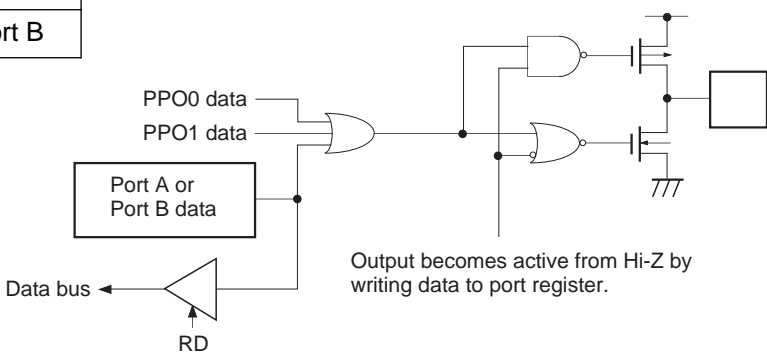
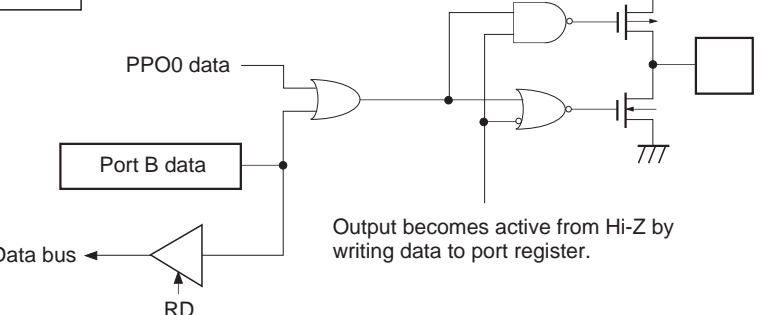
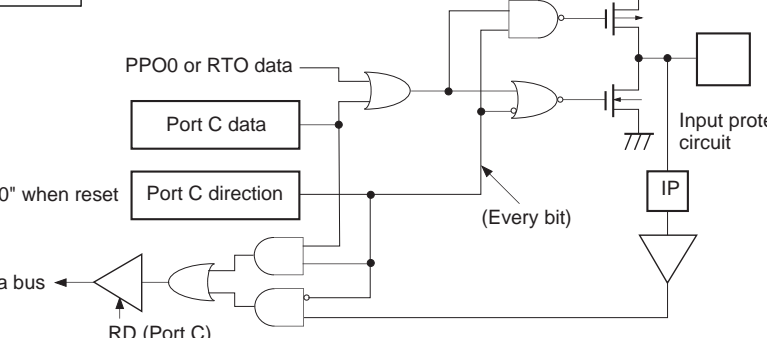
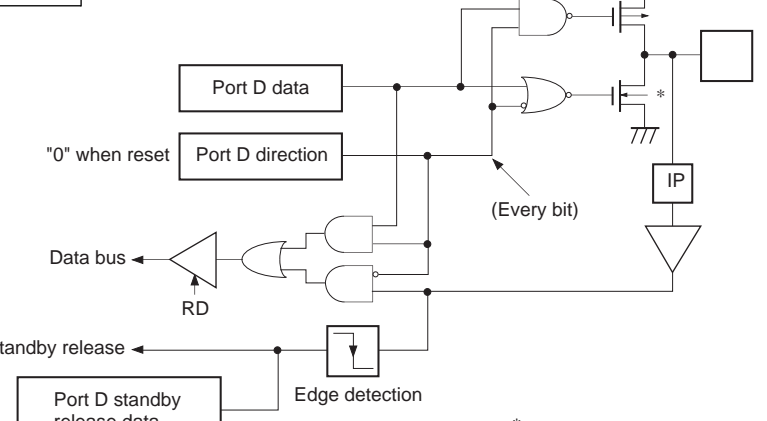
Pin Description

Symbol	I/O	Functions			
PA0/PPO000 /PPO100 to PA7/PPO007 /PPO107	Output / Real time output / Real time output	(Port A) 8-bit output port. Data is gated with PPO0 and PPO1 contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG0, PPG1) output. Functions as high-precision real-time pulse output port. (PPG0 19 pins, PPG1 10 pins)		
PB0/PPO008 /PPO108 PB1/PPO009 /PPO109	Output / Real time output / Real time output	(Port B) 8-bit output port. Data is gated with PPO0 and PPO1 contents by OR-gate and they are output. (8 pins)			
PB2/PPO010 to PB7/PPO015	Output / Real time output				
PC0/PPO016 to PC2/PPO018	Output / Real time output	(Port C) 8-bit I/O port. I/O can be specified by bit unit.			
PC3/RTO0 to PC7/RTO4	Output / Real time output	Data is gated with PPO0 or RTO contents by OR-gate and they are output. (8 pins)			Real-time pulse generator (RTG) output. Functions as high-precision real-time pulse output port. (5 pins)
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be specified by bit unit. Standby release input function can also be specified by bit unit. Can drive 12mA sink current when V <sub>DD</sub> = 5V. (8 pins)			
PE0 to PE7	I/O	(Port E) 8-bit I/O port. I/O can be specified by bit unit. Can drive 12mA sink current when V <sub>DD</sub> = 5V. (8 pins)			
$\overline{PF0}/\overline{EC0}/$ INT0	Input / Input / Input	(Port F) 8-bit port. Lower 4 bits are for input; upper 4 bits are for output. (8 pins)	External event input for timer/counter. (2 pins)	Input to request external interruption. Active at the falling edge. (2 pins)	
$\overline{PF1}/\overline{EC2}/$ INT1	Input / Input / Input				
$\overline{PF2}/\overline{CS1}/$ $\overline{NMI}/\overline{CINT}$	Input / Input / Input / Input		Serial chip select (CH1) input.	Input to request non-maskable interruption. Active at the falling edge.	External capture input for 16-bit timer/counter.
$\overline{PF3}/\overline{SI1}/\overline{INT2}$	Input / Input / Input		Serial data (CH1) input.	Input to request external interruption. Active at the falling edge.	
$\overline{PF4}/\overline{SO1}$	Output / Output		Serial data (CH1) output.		
$\overline{PF5}/\overline{SCK1}$	Output / I/O		Serial data (CH1) I/O.		
$\overline{PF6}/T1$	Output / Output		8-bit timer/counter output.		
$\overline{PF7}/T2$	Output / Output		16-bit capture timer/counter output.		

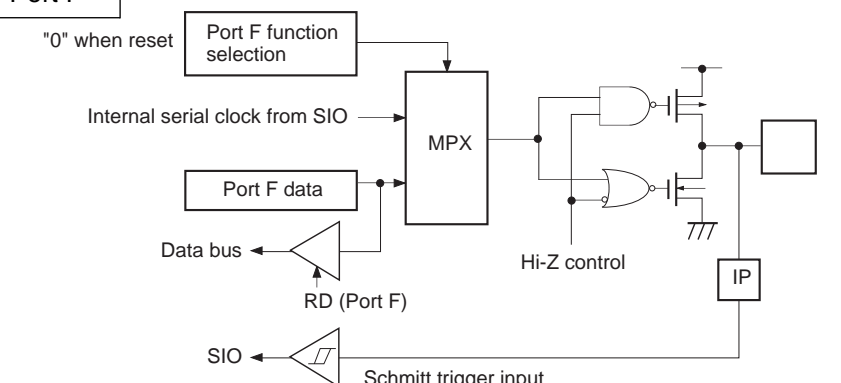
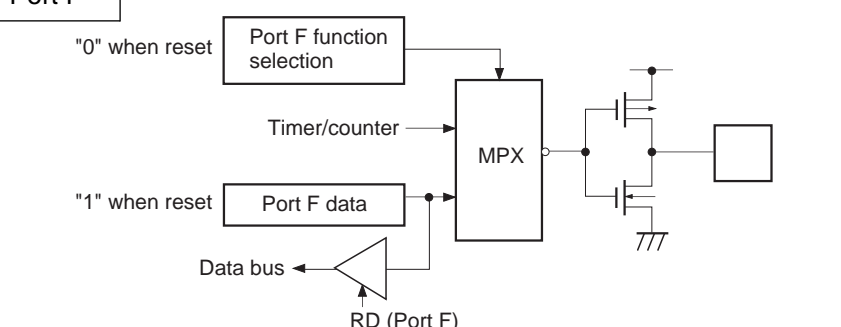
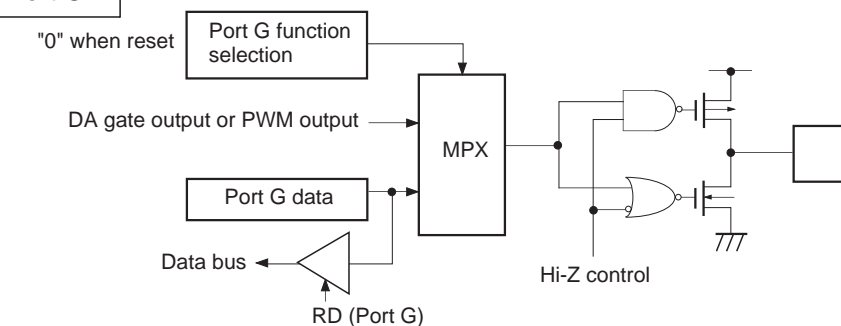
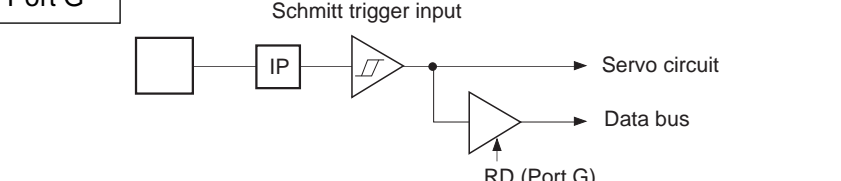
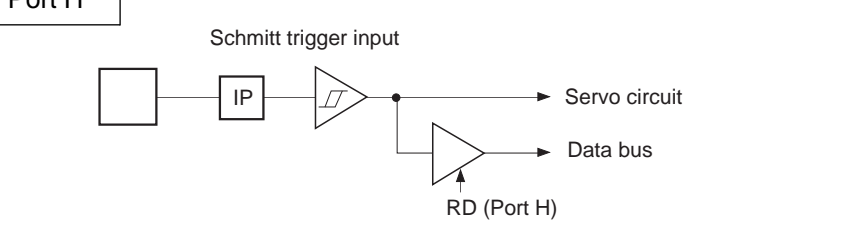
Symbol	I/O	Functions		
PG0/PWM0	Output / Output	(Port G) 8-bit port. Lower 6 bits are for output; upper 2 bits are for input. (8 pins)	14-bit PWM output. (4 pins)	
PG1/PWM1	Output / Output			
PG2/PWM2	Output / Output			
PG3/PWM3	Output / Output			
PG4/DA0	Output / Output		DA gate pulse output. (2 pins)	
PG5/DA1	Output / Output			
PG6/RFG0	Input / Input		Reel FG input. (2 pins)	
PG7/RFG1	Input / Input			
PH0/EXI0	Input / Input	(Port H) 8-bit input port. (8 pins)	External input for FRC capture unit. (2 pins)	
PH1/EXI1	Input / Input			
PH2/ SYNC0/PMI	Input / Input / Input		Composite sync signal input. (2 pins)	Pulse input for pulse cycle measurement circuit.
PH3/SYNC1	Input / Input		Mask input for pulse cycle measurement circuit.	
PH4/PMSK	Input / Input		Drum PG input.	
PH5/DPG	Input / Input		Drum FG input.	
PH6/DFG	Input / Input		Capstan FG input.	
PH7/CFG	Input / Input			
SCK0	I/O	Serial clock (CH0) I/O.		
SO0	Output	Serial data (CH0) output.		
SI0	Input	Serial data (CH0) input.		
CS0	Input	Serial chip select (CH0) input.		
PI0/SI2	I/O / Input	(Port I) 8-bit port. Lower 4 bits are for I/O; upper 4 bits are for input. Lower 4 bits can be specified by bit unit. (8 pins)	Serial data (CH2) input.	
PI1/SO2	I/O / Output		Serial data (CH2) output.	
PI2/SCK2	I/O / I/O		Serial clock (CH2) I/O.	
PI3/CS2/PO	I/O / Input / Output		Serial chip select (CH2) input.	General-purpose prescaler output.
PI4/PCK/ OSCI	Input / Input / Input		General-purpose prescaler external clock input.	Connects a crystal for general-purpose prescaler clock oscillation. (Mask option)
PI5/OSCO	Input / Output			
PI6/XOUT	Input / Output		Clock output from clock generator or general-purpose prescaler.	
PI7/AN0	Input / Input			
AN1 to AN3	Input			
PJ0/AN4 to PJ7/AN11	I/O / Input	(Port J) 8-bit I/O port. I/O can be specified by bit unit. Standby release input function can also be specified by bit unit. (8 pins)	Analog input for A/D converter. (12 pins)	

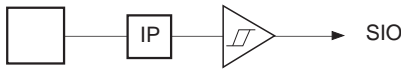
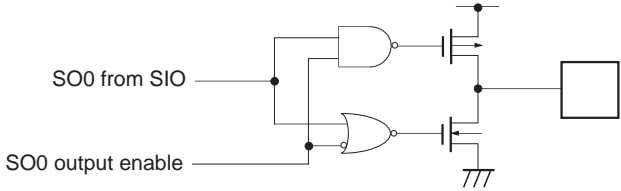
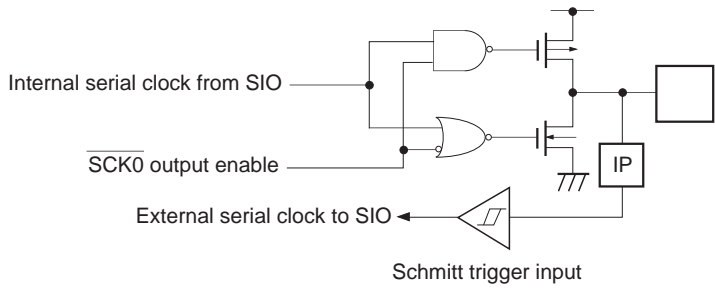
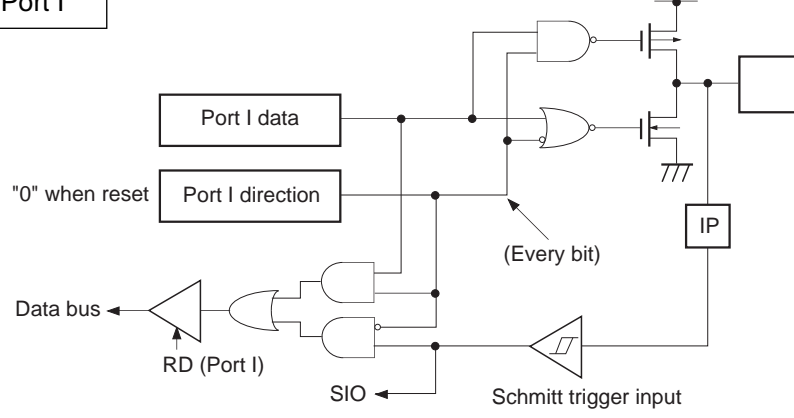
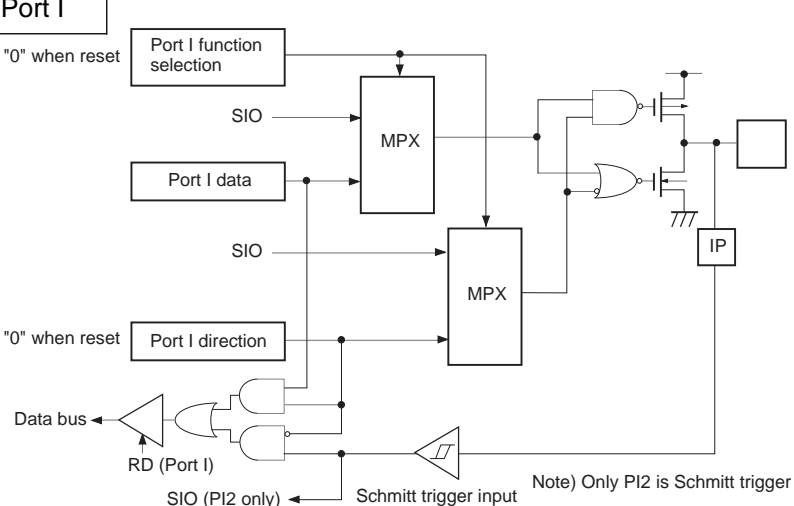
Symbol	I/O	Functions
EXTAL	Input	Connects a crystal for system clock oscillation. When the clock is supplied externally, input it to EXTAL and input an opposite phase clock to XTAL.
XTAL	Output	
$\overline{\text{RST}}$	I/O	System reset. Active at "L" level.
AV <sub>DD</sub>		Positive power supply for A/D converter.
AV <sub>REF</sub>	Input	Reference voltage input for A/D converter.
AV <sub>SS</sub>		A/D converter GND.
V <sub>DD</sub>		Positive power supply. All three V <sub>DD</sub> pins must be connected to the positive power supply.
V <sub>SS</sub>		GND. All four V <sub>SS</sub> pins must be connected to GND.

I/O Circuit Format for Pins

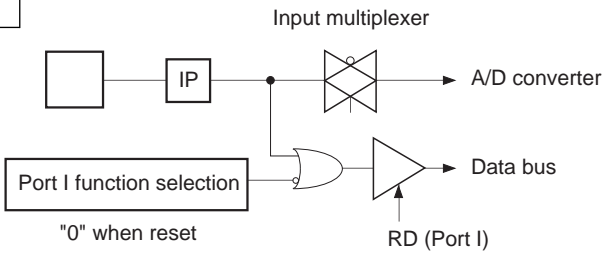
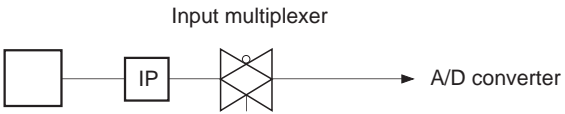
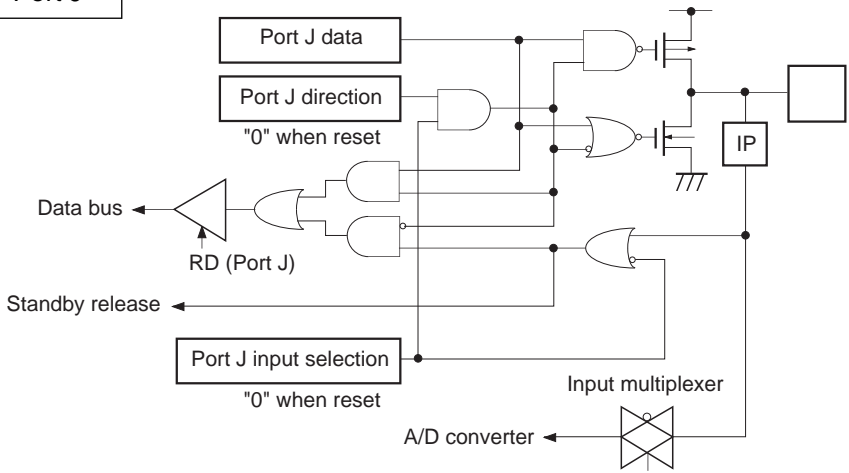
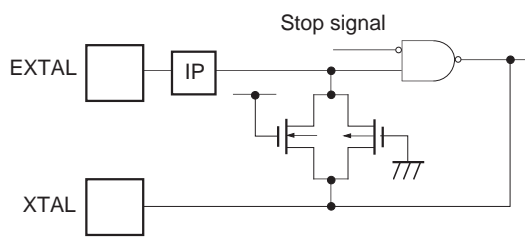
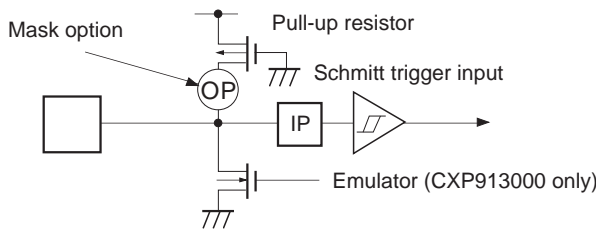
Pin	Circuit format	When reset
<p>PA0/PPO000/ PPO100 to PA7/PPO007/ PPO107</p> <p>PB0/PPO008/ PPO108 to PB1/PPO009/ PPO109</p> <p>10 pins</p>	<p>Port A Port B</p>  <p>Output becomes active from Hi-Z by writing data to port register.</p>	<p>Hi-Z</p>
<p>PB2/PPO010 to PB7/PPO015</p> <p>6 pins</p>	<p>Port B</p>  <p>Output becomes active from Hi-Z by writing data to port register.</p>	<p>Hi-Z</p>
<p>PC0/PPO016 to PC2/PPO018</p> <p>PC3/RTO0 to PC7/RTO4</p> <p>8 pins</p>	<p>Port C</p>  <p>Input protection circuit</p> <p>IP</p> <p>(Every bit)</p> <p>RD (Port C)</p>	<p>Hi-Z</p>
<p>PD0/KS0 to PD7/KS7</p> <p>8 pins</p>	<p>Port D</p>  <p>Input protection circuit</p> <p>IP</p> <p>(Every bit)</p> <p>RD</p> <p>Standby release</p> <p>Edge detection</p> <p>Port D standby release data</p> <p>* Large current drive transistor</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE0 to PE7</p> <p>8 pins</p>	<p>Port E</p> <p>* Large current drive transistor</p>	<p>Hi-Z</p>
<p>PF0/<math>\overline{\text{EC0}}</math>/INT0 PF1/<math>\overline{\text{EC2}}</math>/INT1 PF3/SI1/INT2</p> <p>3 pins</p>	<p>Port F</p> <p>Interrupt circuit and timer/counter or SIO</p> <p>Data bus</p> <p>RD (Port F)</p>	<p>Hi-Z</p>
<p>PF2/<math>\overline{\text{CS1}}</math>/ NMI/CINT</p> <p>1 pin</p>	<p>Port F</p> <p>"0" when reset</p> <p>Port F function selection</p> <p>Interrupt circuit</p> <p>Timer/counter or SIO</p> <p>Data bus</p> <p>RD (Port F)</p>	<p>Hi-Z</p>
<p>PF4/SO1</p> <p>1 pin</p>	<p>Port F</p> <p>"0" when reset</p> <p>Port F function selection</p> <p>SO1 from SIO</p> <p>MPX</p> <p>Port F data</p> <p>Data bus</p> <p>RD (Port F)</p> <p>Hi-Z control</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PF5/SCK1</p> <p>1 pin</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PF6/T1 PF7/T2</p> <p>2 pins</p>	<p>Port F</p> 	<p>"H" level</p>
<p>PG0/PWM0 PG1/PWM1 PG2/PWM2 PG3/PWM3 PG4/DA0 PG5/DA1</p> <p>6 pins</p>	<p>Port G</p> 	<p>Hi-Z</p>
<p>PG6/RFG0 PG7/RFG1</p> <p>2 pins</p>	<p>Port G</p> 	<p>Hi-Z</p>
<p>PH0/EXI0 PH1/EXI1 PH2/SYNC0/PMI PH3/SYNC1 PH4/PMSK PH5/DPG PH6/DFG PH7/CFG</p> <p>8 pins</p>	<p>Port H</p>  <p>Note) PH2/SYNC0/PMI and PH3/SYNC1 can select CMOS Schmitt trigger input or TTL Schmitt trigger input with the mask option.</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
$\overline{\text{CS0}}$ $\text{SIO}$ 2 pins	Schmitt trigger input 	Hi-Z
$\text{SO0}$ 1 pin		Hi-Z
$\overline{\text{SCK0}}$ 1 pin		Hi-Z
$\text{PI0/SI2}$ 1 pin	Port I 	Hi-Z
$\text{PI1/SO2}$ $\text{PI2/SCK2}$ 2 pins	Port I "0" when reset  <p>Note) Only PI2 is Schmitt trigger input.</p>	Hi-Z

Pin	Circuit format	When reset
<p>PI3/<math>\overline{\text{CS2}}</math>/PO</p> <p>1 pin</p>	<p>Port I</p>	<p>Hi-Z</p>
<p>PI4/PCK/OSCI</p> <p>PI5/OSCO</p> <p>2 pins</p>	<p>Port I</p> <p>Fig. 1.</p> <p>Fig. 2.</p> <p>Note) The circuit format in Fig. 1 or Fig. 2 can be selected with the mask option.</p>	<p>Oscillation</p> <p>Hi-Z</p>
<p>PI6/XOUT</p> <p>1 pin</p>	<p>Port I</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PI7/AN0</p> <p>1 pin</p>	<p>Port I</p> 	<p>Hi-Z</p>
<p>AN1 to AN3</p> <p>3 pins</p>		<p>Hi-Z</p>
<p>PJ0/AN4/KS8 to PJ7/AN11/KS15</p> <p>8 pins</p>	<p>Port J</p> 	<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Diagram shows circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop mode.</li> </ul>	<p>Oscillation</p>
<p>RST</p> <p>1 pin</p>		<p>"L" level</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	AV <sub>DD</sub>	AV <sub>SS</sub> to +7.0* <sup>1</sup>	V	
	AV <sub>SS</sub>	-0.3 to +0.3	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>2</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>2</sup>	V	
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	∑I <sub>OH</sub>	-50	mA	Total for all output pins
Low level output current	I <sub>OL</sub>	15	mA	All pins excluding large current output pins
	I <sub>OLC</sub>	20	mA	Large current output pins* <sup>3</sup>
Low level total output current	∑I <sub>OL</sub>	130	mA	Total for all output pins
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	380	mW	

\*1 AV<sub>DD</sub> and V<sub>DD</sub> must be the same voltage.

\*2 V<sub>IN</sub> and V<sub>OUT</sub> must not exceed V<sub>DD</sub> + 0.3V.

\*3 N-ch transistors of PD and PE output ports are the large current drive transistors.

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	2.7	5.5	V	Guaranteed operation range for high-speed mode (1/2 frequency dividing clock)
		2.7	5.5	V	Guaranteed operation range for low-speed mode (1/16 frequency dividing clock)
		2.5	5.5	V	Guaranteed data hold range during stop mode
Analog voltage	AV <sub>DD</sub>	2.7	5.5	V	*1
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*2
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	CMOS Schmitt trigger input*3
	V <sub>IHTS</sub>	2.2	V <sub>DD</sub>	V	TTL Schmitt trigger input*4, *7
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL*5
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*2
			0.2V <sub>DD</sub>	V	*2, *6
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	CMOS Schmitt trigger input*3
	V <sub>ILTS</sub>	0	0.8	V	TTL Schmitt trigger input*4, *7
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL
Operating temperature	Topr	-20	+75	°C	

\*1 AV<sub>DD</sub> and V<sub>DD</sub> must be the same voltage.

\*2 PC, PD, PE, PI1, PI3 to PI7, PJ for normal input port

\*3  $\overline{CS0}$ , SI0,  $\overline{SCK0}$ ,  $\overline{RST}$ , PF0/ $\overline{EC0}$ / $\overline{INT0}$ , PF1/ $\overline{EC2}$ / $\overline{INT1}$ , PF2/ $\overline{CS1}$ / $\overline{NMI}$ / $\overline{CINT}$ , PF3/SI1/ $\overline{INT2}$ , PF5/ $\overline{SCK1}$ , PG6/RFG0, PG7/RFG1, PH (PH2 and PH3 when CMOS Schmitt trigger input is selected with the mask option), PI0/SI2, PI2/ $\overline{SCK2}$ .

\*4 PH2 and PH3 (when TTL Schmitt trigger input is selected with the mask option).

\*5 Specified only during external clock input.

\*6 When the supply voltage (V<sub>DD</sub>) is within the range of 2.7 to 3.6V.

\*7 When the supply voltage (V<sub>DD</sub>) is within the range of 4.5 to 5.5V.

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit	
High level output voltage	VOH	PA to PE, PF6 to PF7, PG0 to PG5, PI0, PI3, PI6, PJ	VDD = 4.5V, IOH = -0.5mA	4.0			V	
			VDD = 4.5V, IOH = -1.2mA	3.5			V	
			VDD = 2.7V, IOH = -0.15mA	2.4			V	
			VDD = 2.7V, IOH = -0.5mA	2.0			V	
		PF4, PF5, PI1, PI2, SO0, SCK0	VDD = 4.5V, IOH = -4.0mA	3.6			V	
			VDD = 3.0V, IOH = -4.0mA	2.0			V	
Low level output voltage	VOL	PA to PC, PF4 to PF7, PG0 to PG5, PI0 to PI3, PI6, PJ, SO0, SCK0, RST*1	VDD = 4.5V, IOL = 1.8mA			0.4	V	
			VDD = 4.5V, IOL = 3.6mA			0.6	V	
			VDD = 2.7V, IOL = 1.2mA			0.3	V	
			VDD = 2.7V, IOL = 1.6mA			0.5	V	
		PD, PE	VDD = 4.5V, IOL = 12.0mA			1.5	V	
			VDD = 2.7V, IOL = 5.0mA			1.0	V	
Input current	IIHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA	
			VDD = 3.6V, VIH = 3.6V	0.3		20	μA	
	IILE		VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA	
			VDD = 3.6V, VIL = 0.3V	-0.3		-20	μA	
	IILR	RST*2	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA	
			VDD = 3.6V, VIL = 0.3V	-0.9		-200	μA	
I/O leakage current	IIZ	PA to PJ, AN1 to AN3, CS0, SI0, SO0, SCK0, RST*2	VDD = 5.5V, VI = 0, 5.5V			±10	μA	
			VDD = 3.6V, VI = 0, 3.6V			±10	μA	
Supply current*3	IDD*4	VDD, VSS	20MHz crystal oscillation (C1 = C2 = 10pF), VDD = 5V ± 10%		40	65	mA	
			20MHz crystal oscillation (C1 = C2 = 10pF), VDD = 3.3V ± 0.3V		22	40	mA	
	IDDS1*5		20MHz crystal oscillation (C1 = C2 = 10pF), VDD = 5V ± 10%, Sleep mode		8	14	mA	
			20MHz crystal oscillation (C1 = C2 = 10pF), VDD = 3.3V ± 0.3V, Sleep mode		4.5	8	mA	
	IDDS2		VDD = 5.5V, Stop mode				10	μA
			VDD = 3.6V, Stop mode				10	μA
Input capacitance	CIN	Pins other than VDD, VSS, AVDD, AVSS	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF	

- \*1  $\overline{\text{RST}}$  is specified only in evaluation mode.
- \*2 In  $\overline{\text{RST}}$ , the input current is specified when pull-up resistor is selected; the leakage current is specified when no resistor is selected.
- \*3 When all output pins are open.
- \*4 When the upper two bits (CPU clock selected) of the clock control register (CLC: 0002FEh) are set to "00" and the LSI is operated in high-speed mode (1/2 frequency dividing clock).
- \*5 When the clock generator output is not selected at PI6.

**AC Characteristics**

**(1) Clock timing**

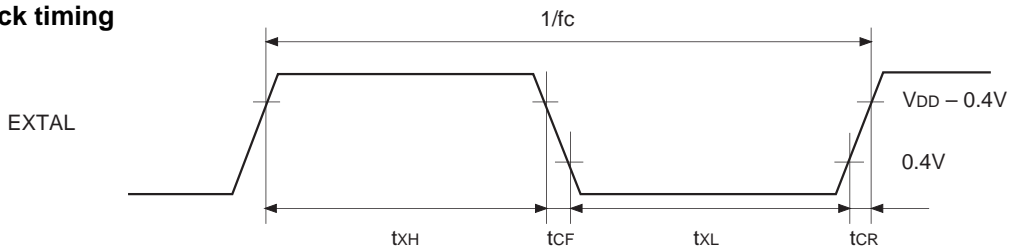
( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit	
System clock frequency	fc	XTAL, EXTAL	Fig. 1, Fig. 2	$V_{DD} = 5.0\text{V} \pm 10\%$	1	20	MHz
				$V_{DD} = 3.0\text{V} \pm 10\%$	1	20	MHz
System clock input pulse width	$t_{XH}$ , $t_{XL}$	EXTAL	Fig. 1, Fig. 2 External clock drive	$V_{DD} = 5.0\text{V} \pm 10\%$	20		ns
				$V_{DD} = 3.0\text{V} \pm 10\%$	20		ns
System clock input rise time, fall time	$t_{CR}$ , $t_{CF}$	EXTAL	Fig. 1, Fig. 2 External clock drive	$V_{DD} = 5.0\text{V} \pm 10\%$		200	ns
				$V_{DD} = 3.0\text{V} \pm 10\%$		200	ns
Event count input clock pulse width	$t_{EH}$ , $t_{EL}$	PF0/ $\overline{\text{EC0}}$ , PF1/ $\overline{\text{EC2}}$	Fig. 3	$V_{DD} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 50^{*1}$		ns
				$V_{DD} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100^{*1}$		ns
Event count input clock rise time, fall time	$t_{ER}$ , $t_{EF}$	PF0/ $\overline{\text{EC0}}$ , PF1/ $\overline{\text{EC2}}$	Fig. 3	$V_{DD} = 5.0\text{V} \pm 10\%$		20	ms
				$V_{DD} = 3.0\text{V} \pm 10\%$		20	ms

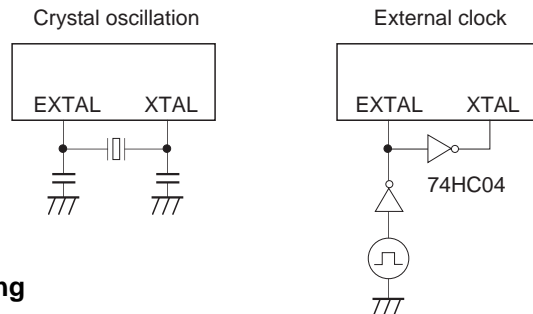
\*1  $t_{\text{sys}}$  indicates the three values below according to the upper two bits (CPU clock selected) of the clock control register (CLC: 0002FEh).

$t_{\text{sys}}$  [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

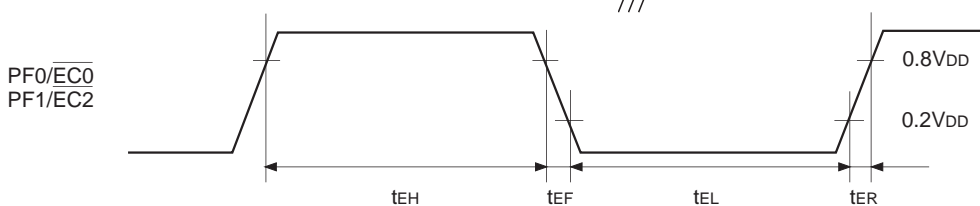
**Fig. 1. Clock timing**



**Fig. 2. Clock applied conditions**



**Fig. 3. Event count clock timing**



(2) Serial interface (CH0, CH1, CH2)

(Ta = -20 to +75°C, Vss = 0V reference)

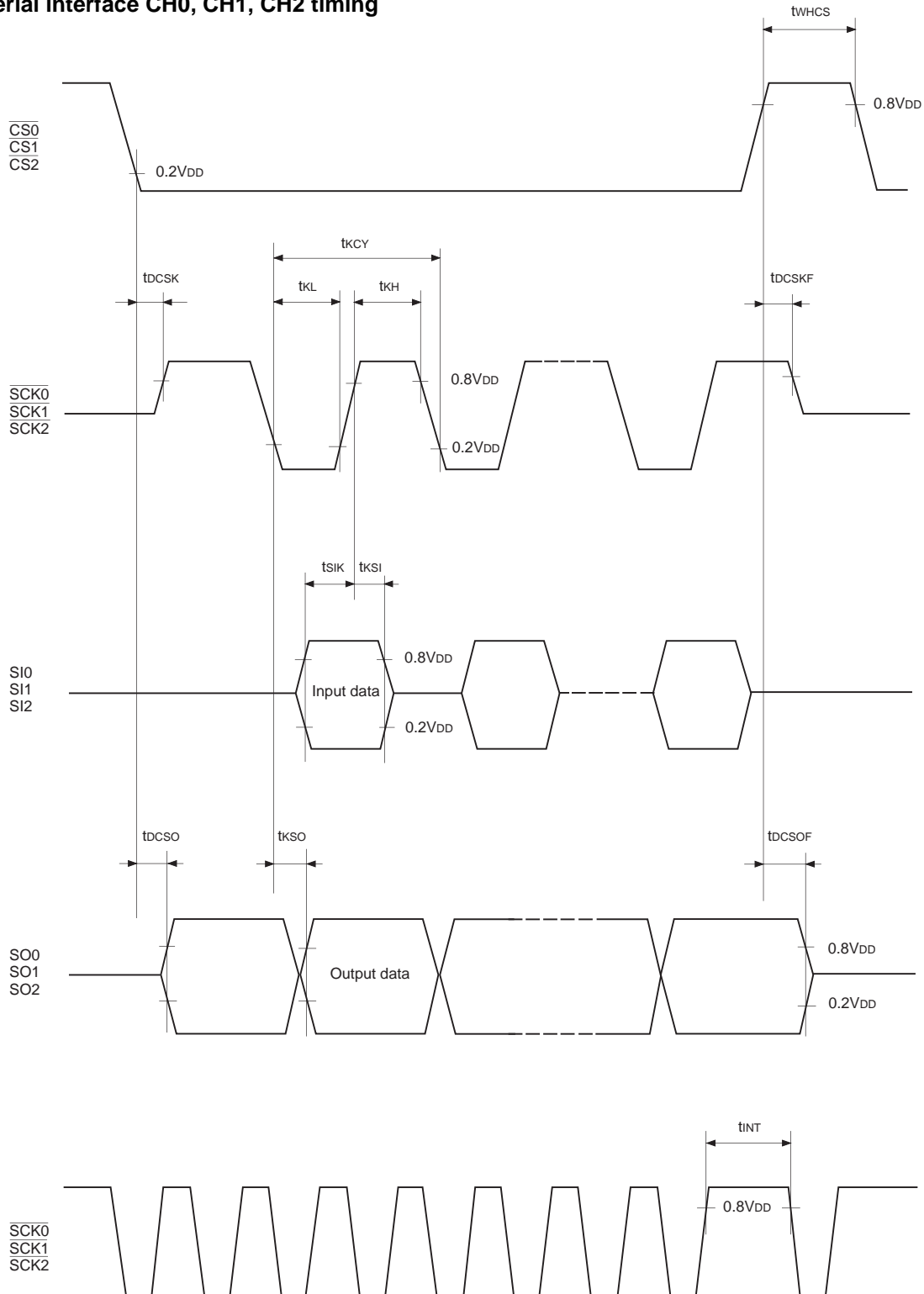
Item	Symbol	Pin	Conditions	Min	Max.	Unit
$\overline{\text{CS}} \downarrow \rightarrow \overline{\text{SCK}}$ delay time	$t_{\text{DCSK}}$	$\overline{\text{SCK0}},$ $\overline{\text{SCK1}},$ $\overline{\text{SCK2}}$	Chip select transfer mode (SCK = output mode)	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 200$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 250$	
$\overline{\text{CS}} \uparrow \rightarrow \overline{\text{SCK}}$ float delay time	$t_{\text{DCSKF}}$	SO0, SO1, SO2	Chip select transfer mode (SCK = output mode)	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 200$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 250$	
$\overline{\text{CS}} \downarrow \rightarrow \text{SO}$ delay time	$t_{\text{DCSO}}$	SO0, SO1 SO2	Chip select transfer mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 200$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 250$	
$\overline{\text{CS}} \uparrow \rightarrow \text{SO}$ float delay time	$t_{\text{DCSOF}}$	$\overline{\text{CS0}},$ $\overline{\text{CS1}},$ $\overline{\text{CS2}}$	Chip select transfer mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 200$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 250$	
$\overline{\text{CS}}$ high level width	$t_{\text{WHCS}}$	$\overline{\text{SCK0}},$ $\overline{\text{SCK1}},$ $\overline{\text{SCK2}}$	Chip select transfer mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK0}},$ $\overline{\text{SCK1}},$ $\overline{\text{SCK2}}$	Input mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$2t_{\text{sys}} + 200$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$2t_{\text{sys}} + 200$	
			Output mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	16000/fc	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	16000/fc	
$\overline{\text{SCK}}$ high, low level width	$t_{\text{KH}},$ $t_{\text{KL}}$	$\overline{\text{SCK0}},$ $\overline{\text{SCK1}},$ $\overline{\text{SCK2}}$	Input mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	
			Output mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$8000/\text{fc} - 50$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$8000/\text{fc} - 75$	
SI input setup time (for $\overline{\text{SCK}} \uparrow$ )	$t_{\text{SIK}}$	SI0, SI1, SI2	$\overline{\text{SCK}}$ input mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	100	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	100	
			$\overline{\text{SCK}}$ output mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$200 - t_{\text{sys}}$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$200 - t_{\text{sys}}$	
SI input hold time (for $\overline{\text{SCK}} \uparrow$ )	$t_{\text{KSI}}$	SI0, SI1, SI2	$\overline{\text{SCK}}$ input mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	
			$\overline{\text{SCK}}$ output mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	$t_{\text{KSO}}$	SO0, SO1, SO2	$\overline{\text{SCK}}$ input mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 150$	
			$\overline{\text{SCK}}$ output mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	50	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	100	
Minimum interval time	$t_{\text{INT}}$	$\overline{\text{SCK0}},$ $\overline{\text{SCK1}},$ $\overline{\text{SCK2}}$	$\overline{\text{SCK}}$ input mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$2t_{\text{sys}} + 100$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$2t_{\text{sys}} + 125$	
			$\overline{\text{SCK}}$ output mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$8000/\text{fc} - 50$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$8000/\text{fc} - 75$	

**Note 1)**  $t_{sys}$  indicates the three values below according to the upper two bits (CPU clock selected) of the clock control register CLC (address: 0002FEh).

$t_{sys} [ns] = 2000/f_c$  (upper two bits = "00"),  $4000/f_c$  (upper two bits = "01"),  $16000/f_c$  (upper two bits = "11")

**Note 2)** The load condition for the SCK output mode, SO output delay time is 150pF when  $V_{DD} = 5.0V \pm 10\%$  and 100pF when  $V_{DD} = 3.0V \pm 10\%$ .

**Fig. 4. Serial interface CH0, CH1, CH2 timing**



**(3) A/D converter characteristics**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = AV_{REF} = 2.7$  to  $5.5\text{V}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit	
Resolution						8	Bits	
Linearity error			$T_a = 25^\circ\text{C}$	$V_{DD} = AV_{DD} = 5.0\text{V}$		$\pm 1.5$	LSB	
				$V_{DD} = AV_{DD} = 3.0\text{V}$		$\pm 1.5$		
Zero transition voltage	$V_{ZT}^{*1}$		$T_a = 25^\circ\text{C}$	$V_{DD} = AV_{DD} = 5.0\text{V}$	-10	10	mV	
				$V_{DD} = AV_{DD} = 3.0\text{V}$	-10	5		35
Full-scale transition voltage	$V_{FT}^{*2}$		$T_a = 25^\circ\text{C}$	$V_{DD} = AV_{DD} = 5.0\text{V}$	4935	4975	mV	
				$V_{DD} = AV_{DD} = 3.0\text{V}$	2955	2985		3015
Conversion time	$t_{CONV}$			$200t_{sys}$			$\mu\text{s}$	
Sampling time	$t_{SAMP}$			$14t_{sys}$			$\mu\text{s}$	
Reference input voltage	$V_{REF}$	$AV_{REF}$		$0.9AV_{DD}$		$AV_{DD}$	V	
Analog input voltage	$V_{IAN}$	ANO to AN11		0		$AV_{REF}$	V	
$AV_{REF}$ current	$I_{REF}$	$AV_{REF}$	Operation mode	$V_{DD} = 5.5\text{V}$		0.65	mA	
				$V_{DD} = 3.6\text{V}$		0.45		0.8
	$I_{REFS}$		Sleep mode Stop mode	$V_{DD} = 5.5\text{V}$			10	$\mu\text{A}$
				$V_{DD} = 3.6\text{V}$			10	

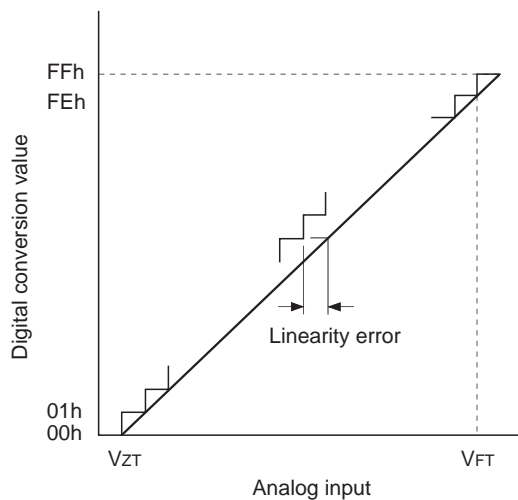
\*1  $V_{ZT}$ : Value at which the digital conversion value changes from 00h to 01h and vice versa.

\*2  $V_{FT}$ : Value at which the digital conversion value changes from FEh to FFh and vice versa.

**Note)**  $t_{sys}$  indicates the three values below according to the upper two bits (CPU clock selected) of the clock control register (CLC: 0002FEh).

$t_{sys}$  [ns] = 2000/ $f_c$  (upper two bits = "00"), 4000/ $f_c$  (upper two bits = "01"), 16000/ $f_c$  (upper two bits = "11")

**Fig. 5. Definition of A/D converter terms**



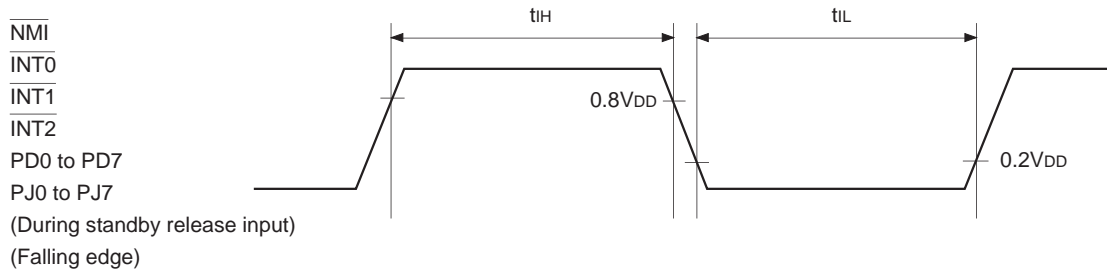
**(4) Interruption and reset input** (Ta = -20 to +75°C, VDD = 2.7 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption high, low level width	t <sub>IH</sub> , t <sub>IL</sub>	$\overline{\text{NMI}}$ $\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ PD0 to PD7		1		μs
Reset input low level width	t <sub>RSL</sub>	$\overline{\text{RST}}$		6t <sub>sys</sub> *1		μs

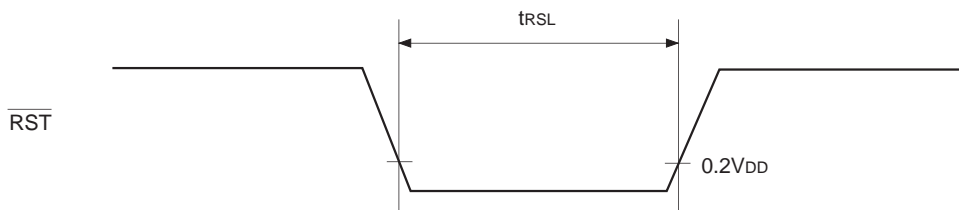
\*1 t<sub>sys</sub> indicates the three values below according to the upper two bits (CPU clock selected) of the clock control register (CLC: 0002FEh).

t<sub>sys</sub> [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

**Fig. 6. Interruption input timing**



**Fig. 7.  $\overline{\text{RST}}$  input timing**



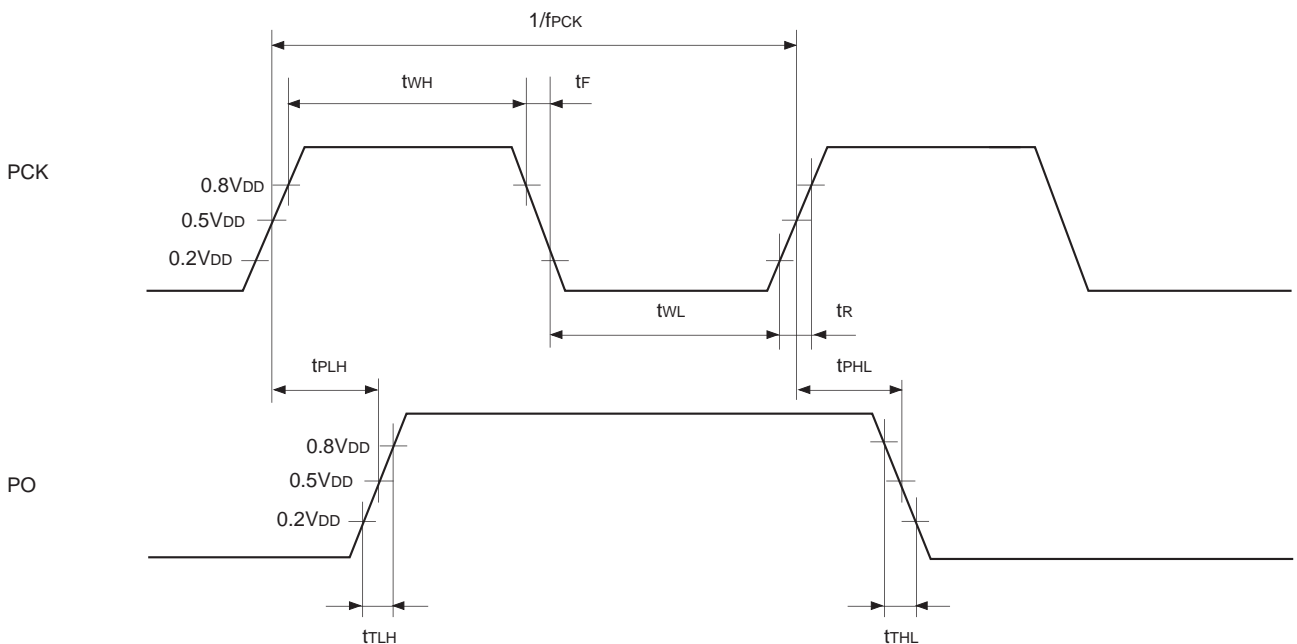
(5) General-purpose prescaler

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
External clock input frequency	f <sub>PCK</sub>	PCK	V <sub>DD</sub> = 5.0V ±10%			12	MHz
			V <sub>DD</sub> = 3.0V ± 10%			12	
External clock input pulse width	t <sub>WH</sub> , t <sub>WL</sub>	PCK	V <sub>DD</sub> = 5.0V ± 10%	33			ns
			V <sub>DD</sub> = 3.0V ± 10%	33			
External clock input rise time, fall time	t <sub>R</sub> , t <sub>F</sub>	PCK	V <sub>DD</sub> = 5.0V ± 10%			200	ns
			V <sub>DD</sub> = 3.0V ± 10%			200	
Prescaler output delay time (for PCK ↑)	t <sub>PLH</sub>	PO	External clock input PCK t <sub>R</sub> = t <sub>F</sub> = 6ns	V <sub>DD</sub> = 5.0V ± 10%	80	130	ns
				V <sub>DD</sub> = 3.0V ± 10%	130	220	
	t <sub>PHL</sub>			V <sub>DD</sub> = 5.0V ± 10%	60	100	ns
				V <sub>DD</sub> = 3.0V ± 10%	90	150	
Prescaler output rise time, fall time	t <sub>TLH</sub>	PO	External clock input PCK t <sub>R</sub> = t <sub>F</sub> = 6ns	V <sub>DD</sub> = 5.0V ± 10%	50	100	ns
				V <sub>DD</sub> = 3.0V ± 10%	100	280	
	t <sub>THL</sub>			V <sub>DD</sub> = 5.0V ± 10%	20	40	ns
				V <sub>DD</sub> = 3.0V ± 10%	40	80	

Note) PO pin load condition: 50pF

Fig. 8. General-purpose prescaler timing



(6) Other

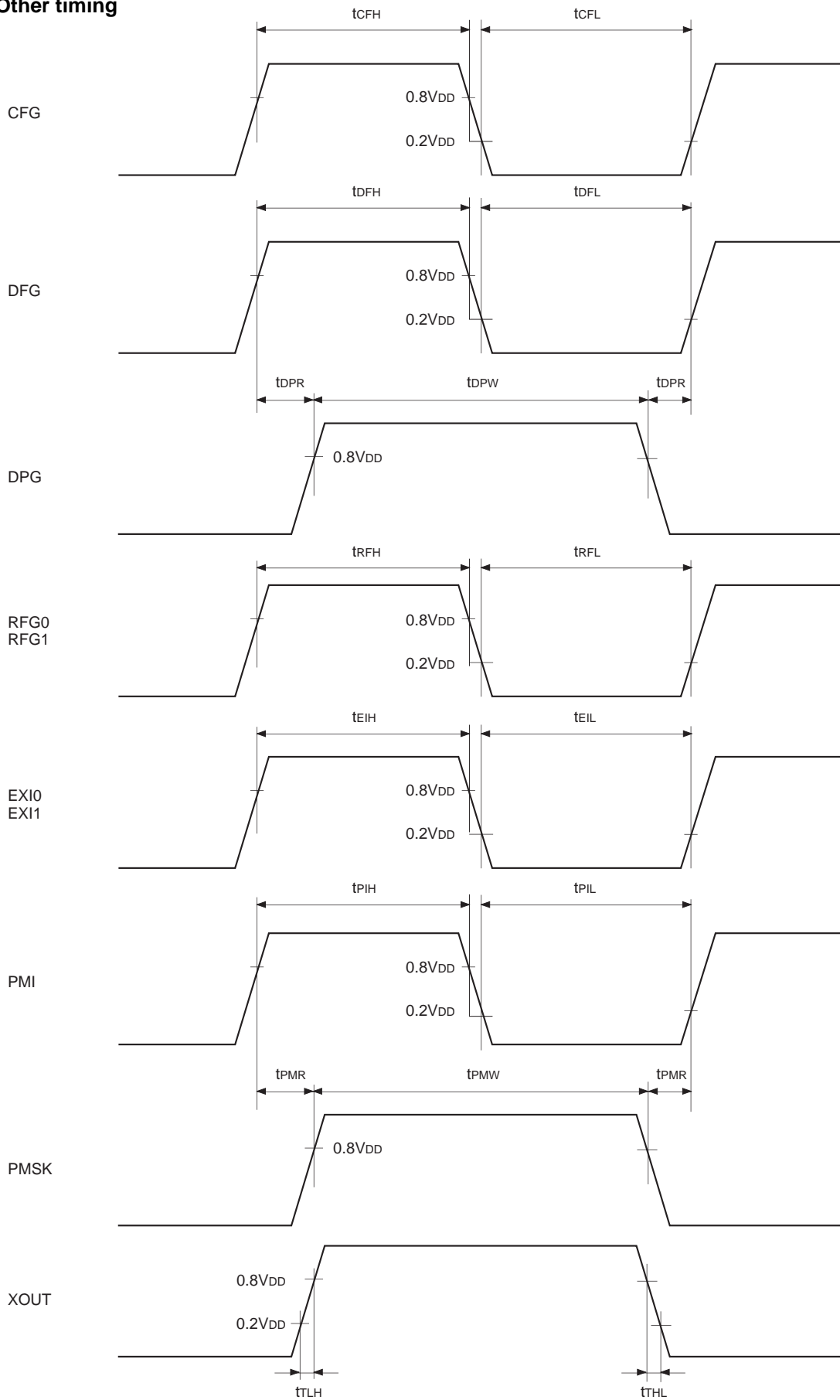
(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit	
CFG input high, low level width	t <sub>CFH</sub> , t <sub> CFL</sub>	CFG	V <sub>DD</sub> = 5.0V ± 10%	t <sub>sys</sub> +200			ns	
			V <sub>DD</sub> = 3.0V ± 10%	t <sub>sys</sub> +200				
DFG input high, low level width	t <sub>DFH</sub> , t <sub> DFL</sub>	DFG	V <sub>DD</sub> = 5.0V ± 10%	1000/fc +200			ns	
			V <sub>DD</sub> = 3.0V ± 10%	1000/fc +200				
DPG minimum pulse width	t <sub>DPW</sub>	DPG	V <sub>DD</sub> = 5.0V ± 10%	50			ns	
			V <sub>DD</sub> = 3.0V ± 10%	50				
DPG minimum removal time	t <sub>DPR</sub>	DPG	V <sub>DD</sub> = 5.0V ± 10%	50			ns	
			V <sub>DD</sub> = 3.0V ± 10%	50				
RFG input high, low level width	t <sub>RFH</sub> , t <sub> RFL</sub>	RFG0 RFG1	V <sub>DD</sub> = 5.0V ± 10%	t <sub>sys</sub> +200			ns	
			V <sub>DD</sub> = 3.0V ± 10%	t <sub>sys</sub> +200				
EXI input high, low level width	t <sub>EIH</sub> , t <sub> EIL</sub>	EXI0 EXI1	When t <sub>sys</sub> = 2000/fc	V <sub>DD</sub> = 5.0V ± 10%	t <sub>sys</sub> +200		ns	
			V <sub>DD</sub> = 3.0V ± 10%	t <sub>sys</sub> +200				
PMI input high, low level width	t <sub>PIH</sub> , t <sub> PIL</sub>	PMI	V <sub>DD</sub> = 5.0V ± 10%	t <sub>sys</sub> +200			ns	
			V <sub>DD</sub> = 3.0V ± 10%	t <sub>sys</sub> +200				
PMSK minimum pulse width	t <sub>PMW</sub>	PMSK	V <sub>DD</sub> = 5.0V ± 10%	t <sub>sys</sub> +200			ns	
			V <sub>DD</sub> = 3.0V ± 10%	t <sub>sys</sub> +200				
PMSK minimum removal time	t <sub>PMR</sub>	PMSK	V <sub>DD</sub> = 5.0V ± 10%	t <sub>sys</sub> +200			ns	
			V <sub>DD</sub> = 3.0V ± 10%	t <sub>sys</sub> +200				
XOUT output rise time, fall time	t <sub>TLH</sub>	XOUT	When the load is 50pF	V <sub>DD</sub> = 5.0V ± 10%		50	100	ns
				V <sub>DD</sub> = 3.0V ± 10%		100	280	
	t <sub>THL</sub>			V <sub>DD</sub> = 5.0V ± 10%		20	40	
	V <sub>DD</sub> = 3.0V ± 10%				40	80		

**Note)** t<sub>sys</sub> indicates the three values below according to the upper two bits (CPU clock selected) of the clock control register (CLC: 0002FEh).

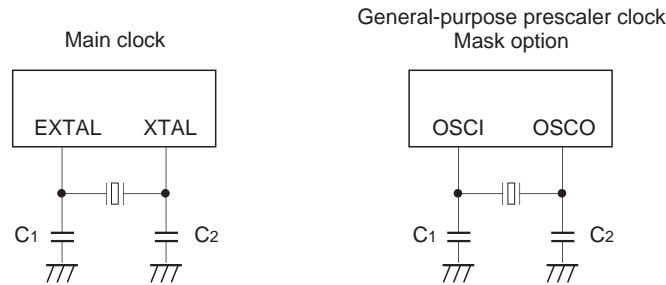
t<sub>sys</sub> [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Fig. 9. Other timing



Appendix

Fig. 10. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	Main clock		General-purpose prescaler clock	
			C1 (pF)	C2 (pF)	C1 (pF)	C2 (pF)
RIVER ELETEC CORPORATION	HC-49/U03	12	10	10	4	4
		16			/	/
		20			/	/
KINSEKI LTD.	HC-49/U (-S)	12	10	10	4	4
		16			/	/
		20			/	/

**Note 1)** Use the general-purpose prescaler clock at 12MHz or less.

**Note 2)** Crystals and capacitors should be placed near the LSI and wiring should be as short as possible.

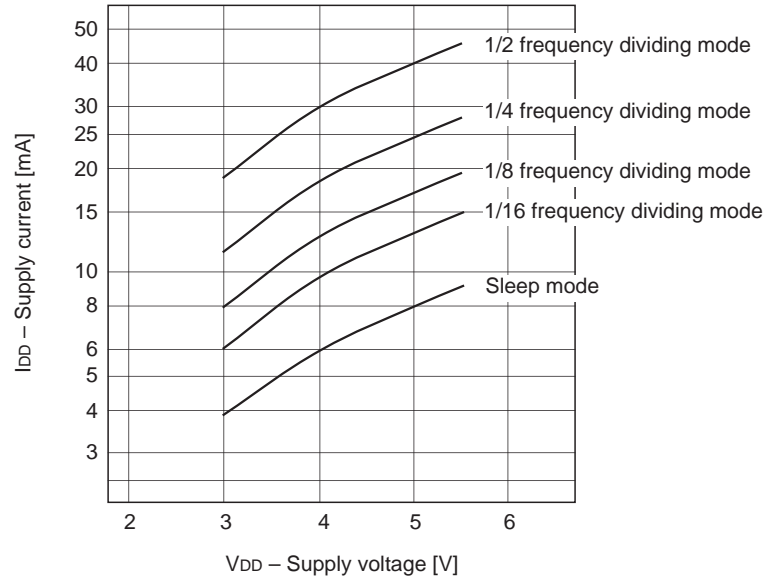
Mask option table

Item	Selection	
EXTAL system operating voltage*1	2.7 to 5.5V	4.5 to 5.5V
Reset pin pull-up resistor	Non-existent	Existent
PH2 input format	CMOS Schmitt trigger	TTL Schmitt trigger
PH3 input format	CMOS Schmitt trigger	TTL Schmitt trigger
PI4/PI5 pin format	Oscillation circuit	Input pin

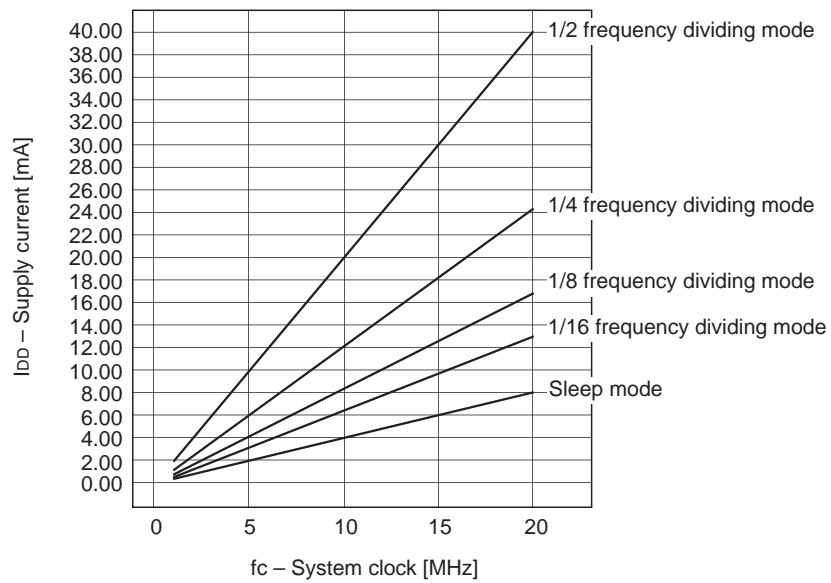
\*1 Select 4.5V to 5.5V when this LSI is used with a supply voltage range of 4.5V to 5.5V.

Example of Representative Characteristics

**I<sub>DD</sub> vs. V<sub>DD</sub>**  
 (f<sub>c</sub> = 20MHz, T<sub>a</sub> = 25°C, Typical)

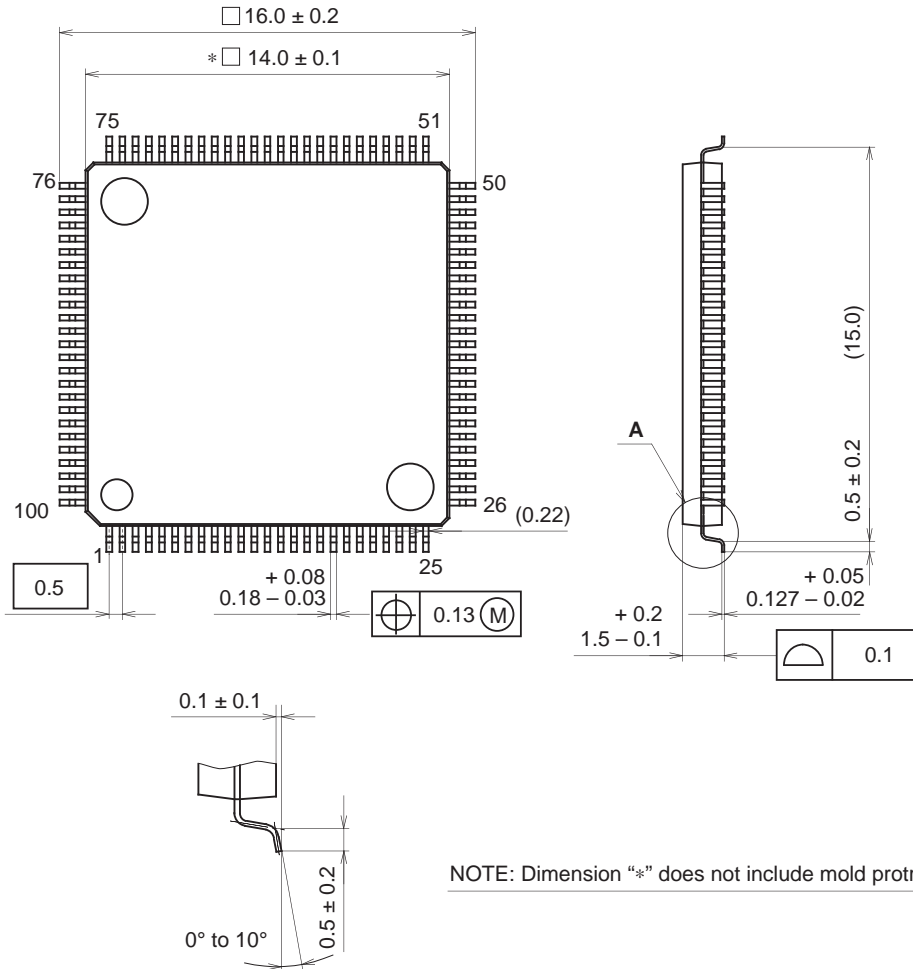


**I<sub>DD</sub> vs. f<sub>c</sub>**  
 (V<sub>DD</sub> = 5V, T<sub>a</sub> = 25°C, Typical)



Package Outline Unit: mm

100PIN LQFP (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

DETAIL A

PACKAGE STRUCTURE

SONY CODE	LQFP-100P-L01
EIAJ CODE	LQFP100-P-1414
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.8g



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