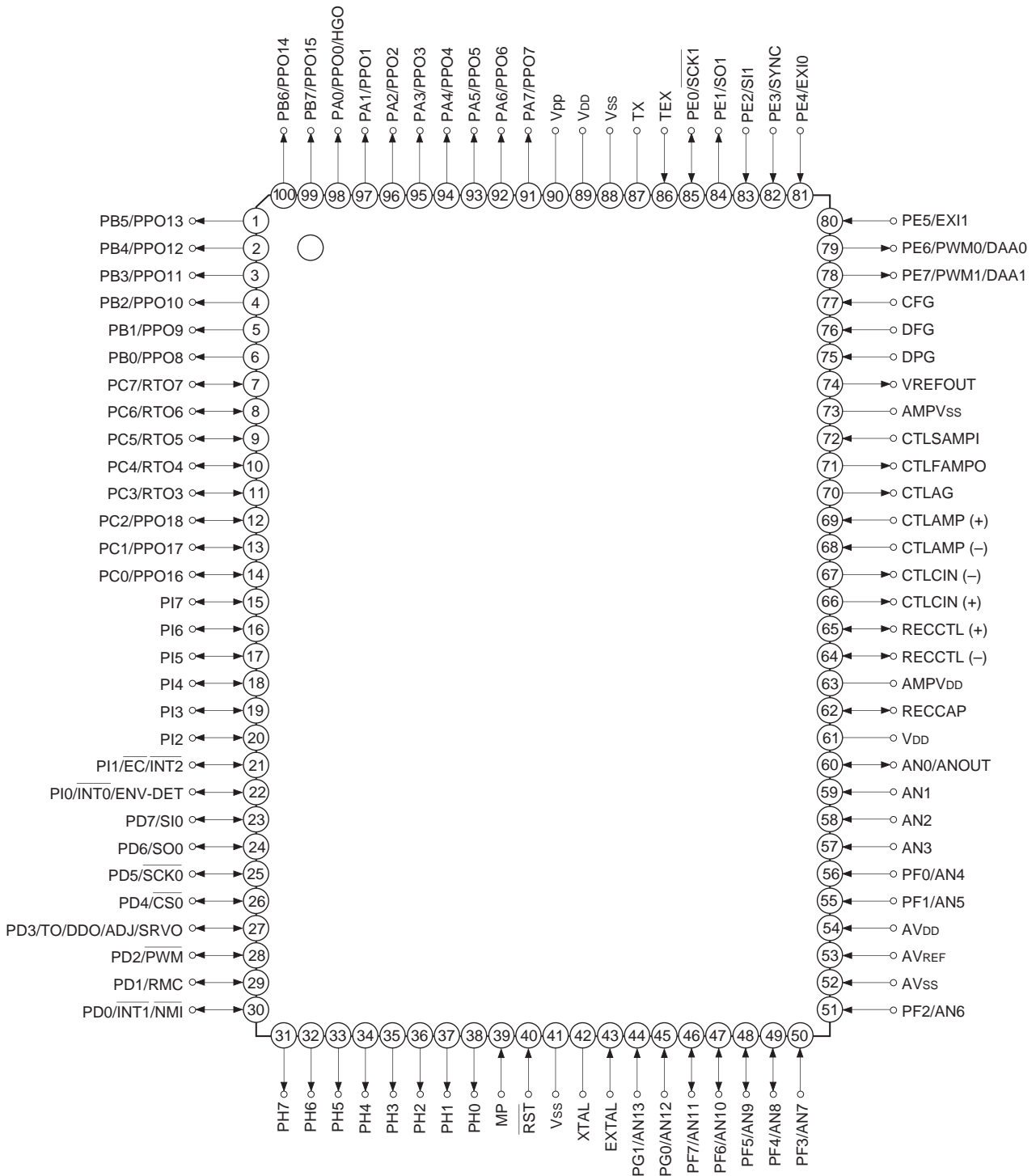


Block Diagram

Pin Assignment (Top View)



- Note**
1. Vpp (Pin 90) is always connected to VDD.
 2. VDD (Pins 61 and 89) are both connected to VDD
 3. Vss (Pins 41 and 88) are both connected to GND.
 4. MP (Pin 39) must be connected to GND.

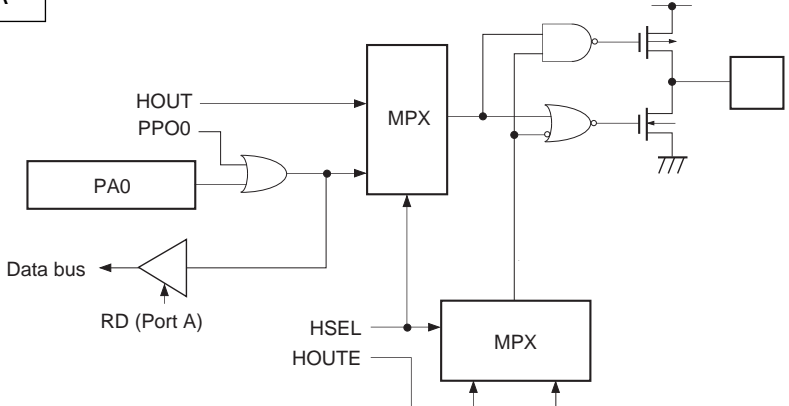
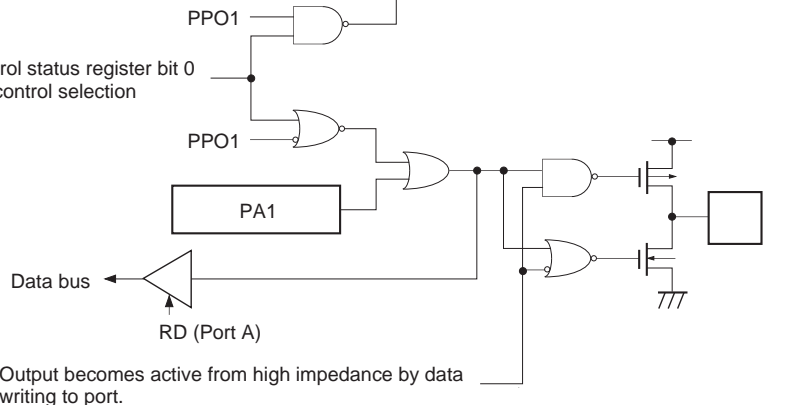
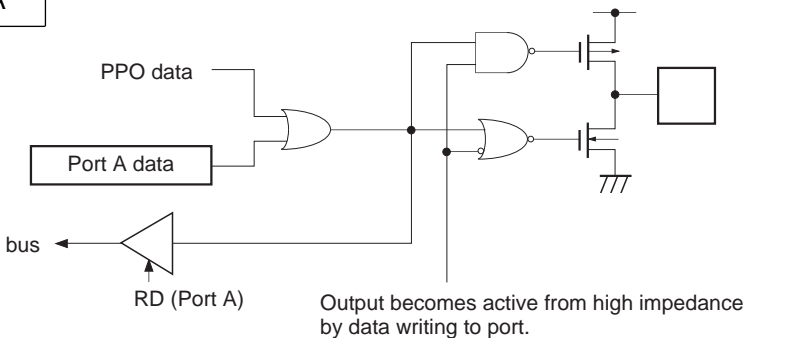
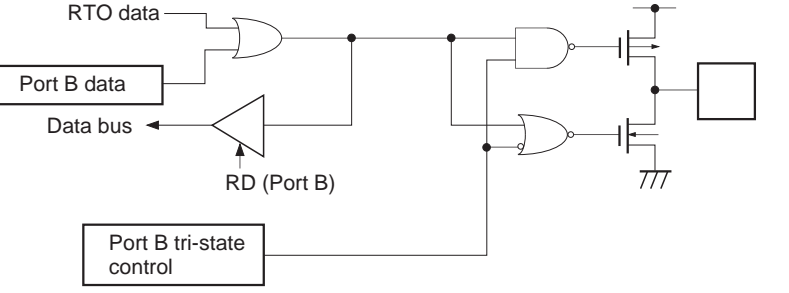
Pin Description

Symbol	I/O	Description	
PA0/PPO0 /HGO	Output/Real-time output/Output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Pseudo HSYNC output pin.
PA1/PPO1 to PA7/PPO7	Output/Real-time output		
PB0/PPO8 to PB7/PPO15	Output/Real-time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. Tri-state control is possible. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port. (19 pins) PA0 can be tri-state controlled with PPG.
PC0/PPO16 to PC2/PPO18	I/O/Real-time output	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with PPO or RT contents by OR-gate and they are output. (8 pins)	
PC3/RTO3 to PC7/RTO7	I/O/Real-time output		Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. (5 pins)
PD0/ $\overline{\text{INT1}}$ /NMI	I/O/Input/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Input pin to request external interruption and non-maskable interruption.
PD1/RMC	I/O/Input		Remote control receiving circuit input pin.
PD2/ $\overline{\text{PWM}}$	I/O/Output		14-bit PWM output pin.
PD3 /TO DDO/ADJ SRVO	I/O/Output/Output/Output/Output		Timer/counter, CTL duty detector, 32kHz oscillation adjustment and servo amplifier output pin.
PD4/ $\overline{\text{CS0}}$	I/O/Input		Serial chip select (CH0) input pin.
PD5/ $\overline{\text{SCK0}}$	I/O/I/O		Serial clock (CH0) I/O pin.
PD6/SO0	I/O/Output		Serial data (CH0) output pin.
PD7/SI0	I/O/Input		Serial data (CH0) input pin.
PE0/ $\overline{\text{SCK1}}$	Output/I/O		Serial clock (CH1) I/O pin
PE1/SO1	Output/Output		Serial data (CH1) output pin
PE2/SI1	Input/Input	Serial data (CH1) input pin	
PE3/SYNC	Input/Input	(Port E) 8-bit port. Bits 2, 3, 4 and 5 are for inputs; bits 0, 1, 6 and 7 are for outputs. (8 pins)	Composite sync signal input pin.
PE4/EXI0	Input/Input	External input pin for FRC capture unit. (2 pins)	
PE5/EXI1	Input/Input		
PE6/PWM0/DAA0	Output/Output		PWM output pin. (2 pins)
PE7/PWM1/DAA1	Output/Output		

Description	I/O	Description	
AN0/ANOUT	Input/Output	Analog circuit internal waveform output pin.	
AN1 to AN3	Input		
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are for inputs; upper 4 bits are for outputs. Lower 4 bits are standby release input pins. (8 pins)	Analog input pin for A/D converter. (14 pins)
PF4/AN8 to PF7/AN11	Output/Input		
PG0/AN12 PG1/AN13	Input/Input	(Port G) 2-bit input port. (2 pins)	
PH0 to PH7	Output	(Port H) 8-bit output port; N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)	
PI0/ $\overline{\text{INT0}}$ / ENV-DET	I/O/Input	(Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Function as standby release input can be set in a unit of single bits. (8 pins)	Input pin to request external interruption. Active when falling edge.
PI1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$	I/O/Input/Input		External event input pin for timer/counter.
PI2 to PI7	I/O		Input pin to request external interruption. Active when falling edge.
CFG	Input	Capstan FG input pin.	
DFG	Input	Drum FG input pin.	
DPG	Input	Drum PG input pin.	
RECCTL (+) RECCTL (-)	I/O	RECCTL signal output pin. (2 pins)	PBCTL signal input pin. (2 pins)
CTLCIN (+) CTLCIN (-)	Output	Connected to RECCTL (+) and RECCTL (-) with the internal switch for playback. (2 pins)	
CTLAMP (+) CTLAMP(-)	Input	Input PBCTL signal with capacitor coupled. (2 pins)	
CTLFAMPO	Output	PBCTL signal 1st amplifier output.	
CTLSAMPI	Input	PBCTL signal 2nd amplifier input.	
RECCAP	I/O	Capacitor connecting pin for the slope setting of the CTL writing trapezoidal wave.	
VREFOUT	Output	Capacitor connecting pin for the VREF level smoothing of DPG, DFG and CFG.	
CTLAG	Output	Capacitor connecting pin for the CTL and AGND smoothing.	
AMPV _{SS}		Analog signal input circuit GND pin.	
AMPV _{DD}		Analog signal input circuit power supply pin.	

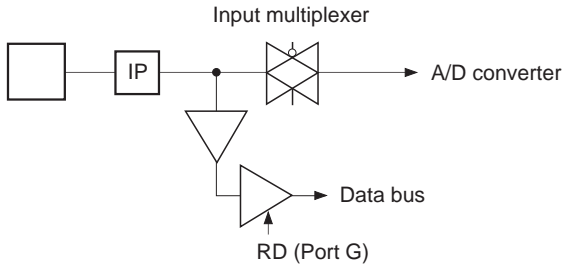
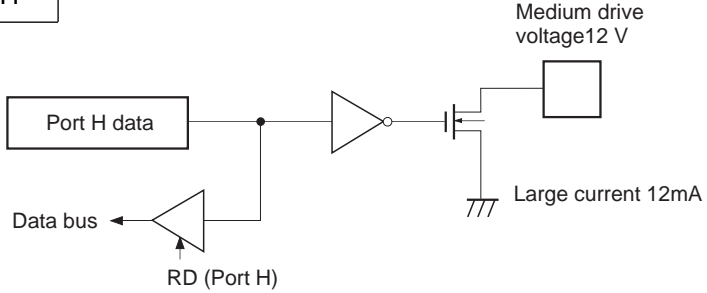
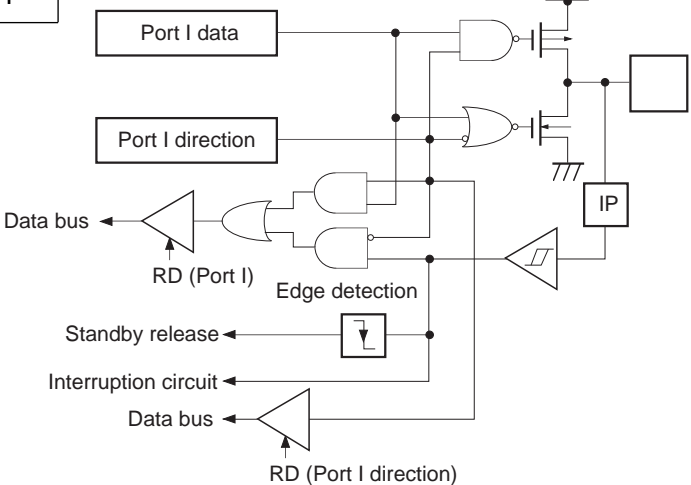
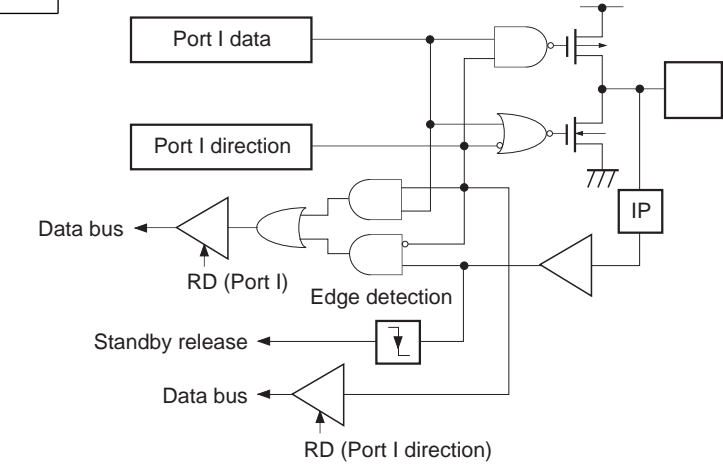
Symbol	I/O	Description
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input it to EXTAL pin and input the opposite phase clock to XTAL pin.
XTAL	Output	
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (In this time, feedback resistor is not removed.)
TX	Output	
$\overline{\text{RST}}$	Input	System reset pin; Low level active.
MP	Input	Test mode input pin. Always connect to GND.
AV _{DD}		Positive power supply pin for A/D converter.
AV _{REF}	Input	Reference voltage input pin for A/D converter.
AV _{SS}		GND pin for A/D converter.
V _{DD}		Positive power supply pin.
V _{pp}		Positive power supply for incorporated PROM writing. Connect this pin to V _{DD} for normal operation.
V _{SS}		GND pin. Connect both V _{SS} pins to GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>PA0/PPO0/ HGO 1 pin</p>	<p>Port A</p>  <p>Output becomes active from high impedance by data writing to port.</p>	<p>Hi-Z</p>
<p>PA1/PPO1 1 pin</p>	 <p>Output becomes active from high impedance by data writing to port.</p>	<p>Hi-Z</p>
<p>PA2/PPO2 to PA7/PPO7 6 pins</p>	<p>Port A</p>  <p>Output becomes active from high impedance by data writing to port.</p>	<p>Hi-Z</p>
<p>PB0/PPO8 to PB7/PPO15 8 pins</p>	<p>Port B</p>  <p>Output becomes active from high impedance by data writing to port.</p>	<p>Hi-Z</p>

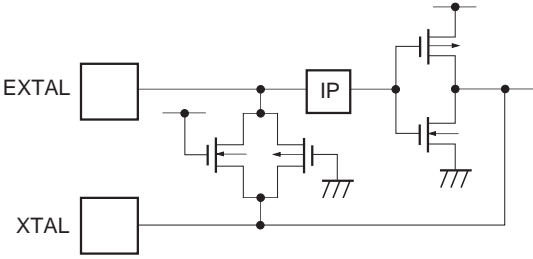
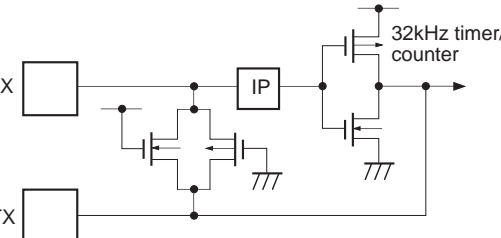
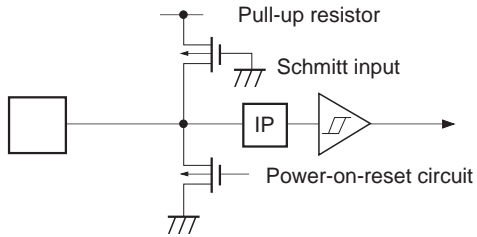
Pin	Circuit format	When reset
<p>PD5/$\overline{\text{SCK0}}$ PD6/$\overline{\text{SO0}}$</p> <p>2 pins</p>	<p>Port D</p> <p>Note) PD5 is schmitt input PD6 is inverter input</p>	<p>Hi-Z</p>
<p>PE0/$\overline{\text{SCK1}}$</p> <p>1 pin</p>	<p>Port E</p>	<p>Hi-Z</p>
<p>PE1/$\overline{\text{SO1}}$</p> <p>1 pin</p>	<p>Port E</p>	<p>Hi-Z</p>
<p>PE2/$\overline{\text{SI1}}$ PE3/$\overline{\text{SYNC}}$ PE4/$\overline{\text{EXI0}}$ PE5/$\overline{\text{EXI1}}$</p> <p>4 pins</p>	<p>Port E</p> <p>Schmitt input</p> <p>PE2...SIO CH1 PE3) PE4) Servo input PE5)</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE6/PWM0/ DAA0 PE7/PWM1/ DAA1</p> <p>2 pins</p>	<p>Port E</p>	<p>High level</p>
<p>AN0/ANOUT</p> <p>1 pin</p>	<p>Port E</p>	<p>Hi-Z</p>
<p>AN1 to AN3</p> <p>3 pin</p>		<p>Hi-Z</p>
<p>PFO/AN4 to PF3/AN7</p> <p>4 pins</p>	<p>Port F</p>	<p>Hi-Z</p>
<p>PF4/AN8 to PF7/AN11</p> <p>4 pins</p>	<p>Port F</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PG0/AN12 to PG1/AN13</p> <p>2 pins</p>	<p>Port G</p> 	<p>Hi-Z</p>
<p>PH0 to PH7</p> <p>8 pins</p>	<p>Port H</p> 	<p>Hi-Z</p>
<p>PI0/$\overline{\text{INT0}}$/EVN-DET to PI1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$</p> <p>2 pins</p>	<p>Port I</p> 	<p>Hi-Z</p>
<p>PI2 to PI7</p> <p>6 pins</p>	<p>Port I</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>CTLAMP (+) CTLAMP (-) CTLFAMPO</p> <p>3 pins</p>		<p>1/2AMPV_{DD}</p>
<p>CTLSAMPI</p> <p>1 pin</p>		<p>1/2AMPV_{DD}</p>
<p>CFG DFG DPG</p> <p>3 pins</p>		<p>1/2AMPV_{DD}</p>
<p>CTLAG VREFOUT</p> <p>2 pins</p>	<p>VREFOUT... CFG, DFG, DPG amplifiers CTLAG..... CTL amplifier</p>	<p>1/2AMPV_{DD}</p>

Pin	Circuit format	When reset
<p>RECCTL (+)</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>RECCTL (-)</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>CTLCIN (+)</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>CTLCIN (-)</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>RECCAP</p> <p>1 pin</p>		<p>Low level</p>

Pin	Circuit format	When reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed and XTAL becomes High level during stop. 	<p>Oscillation</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time, TEX pin outputs Low level and TX pin outputs High level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Schmitt input</p> <p>IP</p> <p>Power-on-reset circuit</p>	<p>Low level</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	V _{pp}	-0.3 to +13	V	Incorporated PROM
	AV _{DD}	AV _{SS} to +7.0 *1	V	
	AV _{SS}	-0.3 to +0.3	V	
	AMPV _{DD}	AMPV _{SS} to +7.0 *2	V	
	AMPV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0 *3	V	
Output voltage	V _{OUT}	-0.3 to +7.0 *3	V	
Medium drive output voltage	V _{OUTP}	-0.3 to +15.0	V	Port PH
High level output current	I _{OH}	-5	mA	
High level total output current	∑I _{OH}	-50	mA	Total of output pins
Low level output current	I _{OL}	15	mA	Other than large current output ports (value per pin)
	I _{OLC}	20	mA	Large current output port *4 (value per pin)
Low level total output current	∑I _{OL}	130	mA	Total of output pins
Operating temperature	T _{opr}	-10 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP package type

*1) AV_{DD} and V_{DD} must not exceed +0.3V.

*2) AMPV_{DD} and V_{DD} must not exceed +0.3V.

*3) V_{IN} and V_{OUT} must not exceed V_{DD} +0.3V.

*4) The large current output port is port H (PH).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clock
		3.5	5.5		Guaranteed operation range for 1/16 frequency dividing clock or during SLEEP mode
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during STOP
	V _{pp}	V _{pp} = V _{DD}			
Analog power supply	AV _{DD}	4.5	5.5	V	*1
	AMPV _{DD}	4.5	5.5	V	*2
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*3
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS schmitt input *4
	V _{IHTS}	2.2	V _{DD}	V	TTL schmitt input *5
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*6 TEX pin*7
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*3
	V _{ILS}	0	0.2V _{DD}	V	CMOS schmitt input *4
	V _{ILTS}	0	0.8	V	TTL schmitt input *5
	V _{ILEX}	-0.3	0.4	V	EXTAL pin *6 TEX pin *7
Operating temperature	Topr	-10	+75	°C	

*1) AV_{DD} and V_{DD} should be set to the same voltage.

*2) AMPV_{DD} and V_{DD} should be set to the same voltage.

*3) Normal input port (each pin of PC, PD2, PD3, PD6, PF0 to PF3, PG and PI2 to PI7), MP pin

*4) Each pin of \overline{RST} , PD0/ $\overline{INT1}$ / \overline{NMI} , PD1/ \overline{RMC} , PD4/ $\overline{CS0}$, PD5/SCK0, PD7/SI0, PE0/ $\overline{SCK1}$, PE2/SI1, PE3/SYNC, PE4/EXI0, PE5/EXI1, PI0/ $\overline{INT0}$, PI1/ \overline{EC} / $\overline{INT2}$ (For PE3/SYNC, when CMOS schmitt input is selected with mask option.)

*5) PE3/SYNC

*6) Specifies only during external clock input.

*7) Specifies only during external event input.

Electrical Characteristics

DC Characteristics ($V_{DD} = 4.5$ to $5.5V$)

($T_a = -10$ to $+75^\circ C$, $V_{SS} = 0V$ reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE0 to PE1, PE6 to PE7, PF4 to PF7, PH (VOL only)	$V_{DD} = 4.5V, I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V, I_{OH} = -1.2mA$	3.5			V
Low level output voltage	V_{OL}	PI (VOL only) \overline{RST}^{*1} (VOL only)	$V_{DD} = 4.5V, I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V, I_{OL} = 3.6mA$			0.6	V
		PD, PH	$V_{DD} = 4.5V, I_{OL} = 12.0mA$			1.5	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.5		40	μA
	I_{ILE}		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.5		-40	μA
	I_{IHT}	TEX	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.1		10	μA
	I_{ILT}		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.1		-10	μA
	I_{ILR}		\overline{RST}	$V_{DD} = 5.5V, V_{IL} = 0.4V$	-1.5		-400
I/O leakage current	I_{IZ}	PA to PG, PI, MP, AN0 to AN3,	$V_{DD} = 5.5V, V_I = 0, 5.5V$			± 10	μA
Open drain output leakage current (N-CH Tr off state)	I_{LOH}	PH	$V_{DD} = 5.5V, V_{OH} = 12V$			50	μA
Supply current*2	I_{DD1}	V_{DD}, V_{SS}	16MHz crystal oscillation ($C_1 = C_2 = 15pF$)		35	45	mA
			$V_{DD} = 5.5V^{*3}$				
	I_{DDS1}		SLEEP mode		2.0	8	mA
			$V_{DD} = 5.5V$				
	I_{DD2}		I_{DD2}	32kHz crystal oscillation ($C_1 = C_2 = 47pF$)		50	100
$V_{DD} = 3.3V$							
I_{DD2}	I_{DD2}	SLEEP mode		9	35	μA	
		$V_{DD} = 3V \pm 0.3V$					
I_{DD3}	I_{DD3}	STOP mode (EXTAL and TEX pins oscillation stop)			30	μA	
$V_{DD} = 5V \pm 0.5V$							
Input capacity	C_{IN}	PC, PD, PE0, PE2 to PE5, PF, PG, PI, RECCTL (+), RECCTL (-), CTLAMP (+), CTLAMP (-), CTLSAMPI, CFG, DFG, DPG	Clock 1MHz 0V other than the measured pins		10	20	pF

*1) \overline{RST} pin specifies the low level input voltage only when the power-on-reset circuit is selected.

*2) When entire output pins are open.

*3) When setting upper 2 bits (CPU clock selection) of clock control register (CLC: 00FEH) to "00" and operating in high speed mode (1/2 frequency dividing clock).

AC Characteristics

(1) Clock timing

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	f_c	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL} , t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise and fall times	t_{CR} , t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count clock input pulse width	t_{EH} , t_{EL}	$\overline{\text{EC}}$	Fig. 3	$t_{\text{sys}} + 200^{*1}$			ns
Event count clock input rise and fall times	t_{ER} , t_{EF}	$\overline{\text{EC}}$	Fig. 3			20	ms
System clock frequency	f_c	TEX TX	$V_{DD} = 2.7$ to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count clock input pulse width	t_{TL} , t_{TH}	TEX	Fig. 3	10			μs
Event count clock input rise and fall times	t_{TR} , t_{TF}	TEX	Fig. 3			20	ms

*1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

$t_{\text{sys}} [\text{ns}] = 2000/f_c$ (Upper 2 bits = "00"), $4000/f_c$ (Upper 2 bits = "01"), $16000/f_c$ (Upper 2 bits = "11")

Fig. 1. Clock timing

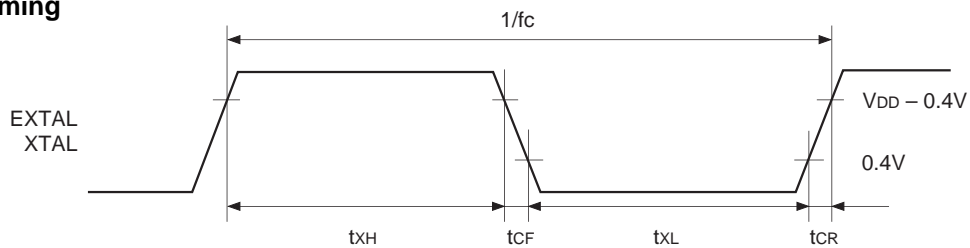


Fig. 2. Clock applied condition

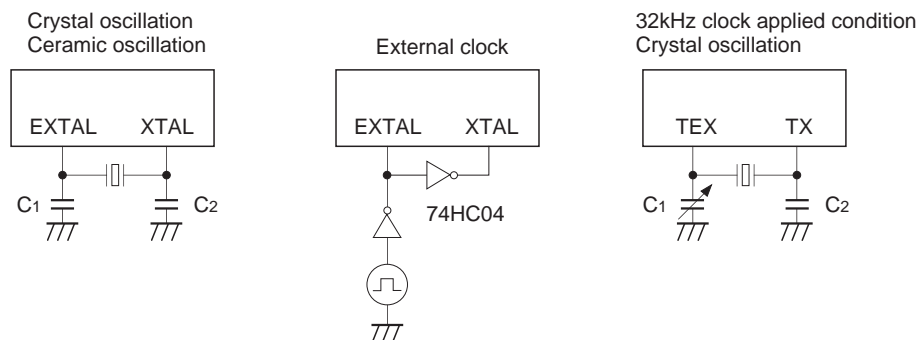
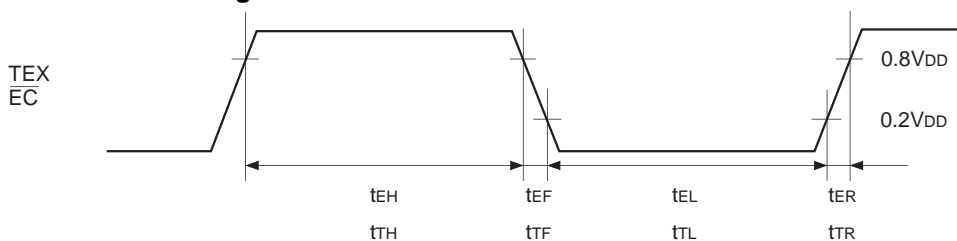


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

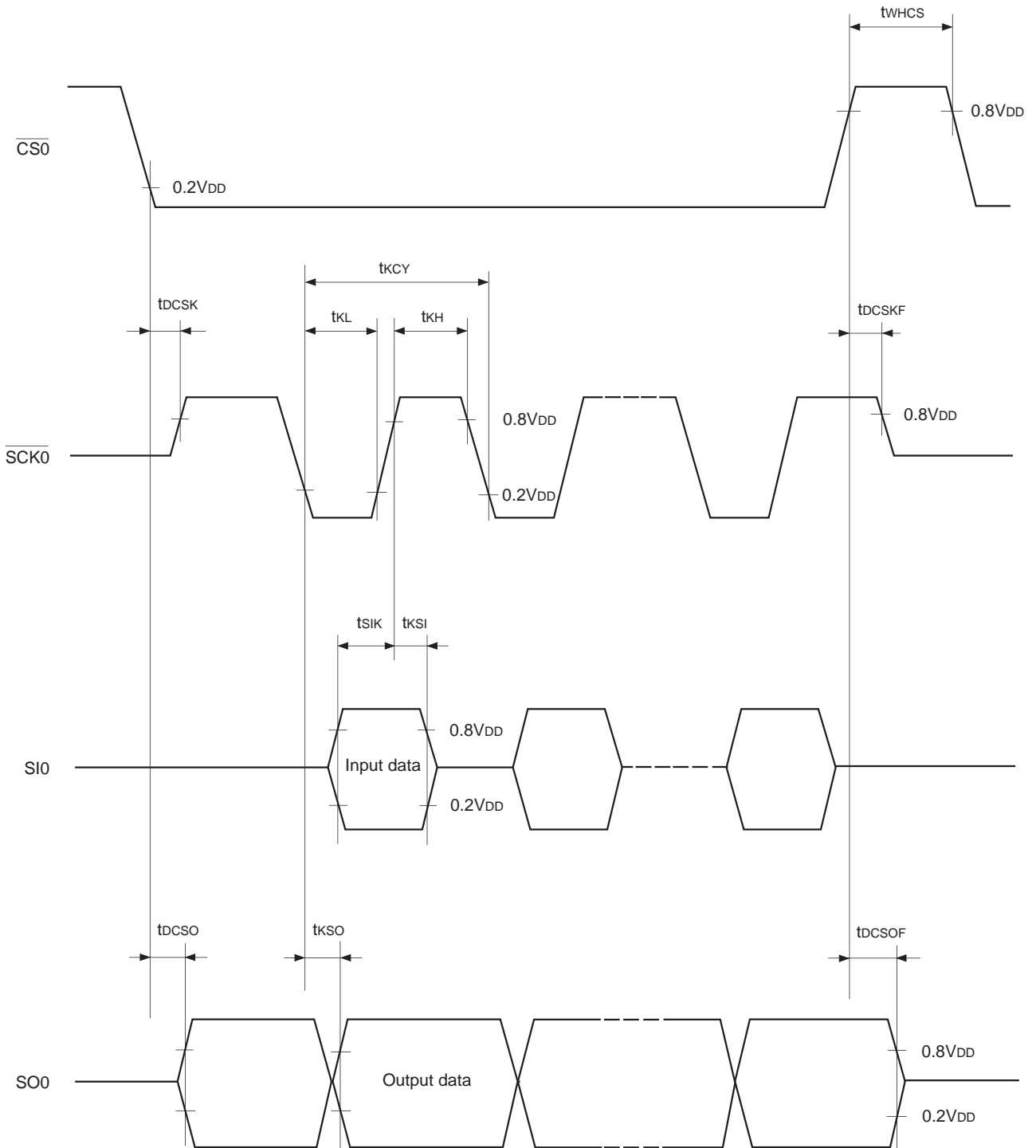
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t _{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		t _{sys} + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ floating delay time	t _{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		t _{sys} + 200	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ floating delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS0}}$ high level width	t _{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{\text{SCK0}}$ cycle time	t _{KCY}	$\overline{\text{SCK0}}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK0}}$ high and low level widths	t _{KH} t _{KL}	$\overline{\text{SCK0}}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 50		ns
SI0 input set-up time (against $\overline{\text{SCK0}} \uparrow$)	t _{SIK}	SI0	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (against $\overline{\text{SCK0}} \uparrow$)	t _{KSI}	SI0	$\overline{\text{SCK0}}$ input mode	t _{sys} + 200		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{KSO}	SO0	$\overline{\text{SCK0}}$ input mode		t _{sys} + 200	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK0}}$ output mode and SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing (CH0)



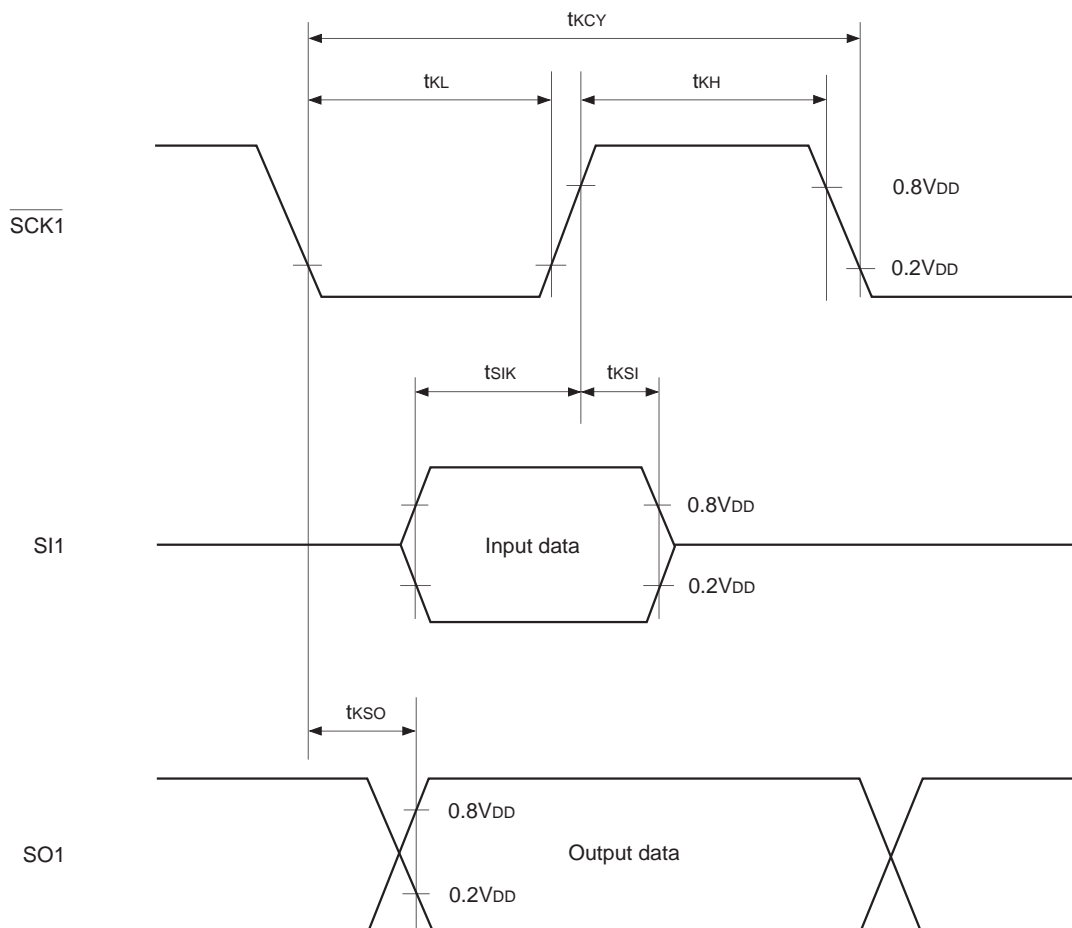
Serial transfer (CH1)

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input set-up time (against $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

Fig. 5. Serial transfer timing (CH1)

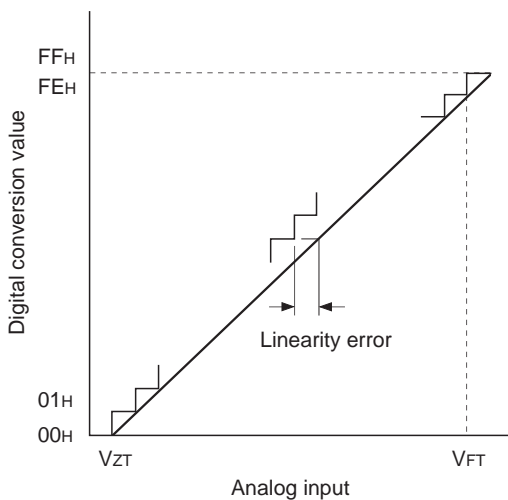


(3) A/D converter characteristics

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation $T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{DD} = AV_{SS} = 0\text{V}$			± 1	LSB
Absolute error						± 2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}^{*1}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*1}$			μs
Reference input voltage	V_{REF}	AV_{REF}		$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN7$		0		AV_{REF}	V
AVREF current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
			SLEEP mode STOP mode 32kHz operation mode			10	μA

Fig. 6. Definitions of A/D converter terms



*1) f_{ADC} indicates the below values due to the contents of bit 0 (ADCCK) of the ADC operation clock selection register (MSC: 01FFH), bits 7 (PCK1) and 6 (PCK0) of the clock control register (address: 00FEH).

PCK1, PCK0	ADCCK	
	0 ($\phi/2$ selection)	1 (ϕ selection)
00 ($\phi = f_{EX}/2$)	$f_{ADC} = f_c/2$	$f_{ADC} = f_c$
01 ($\phi = f_{EX}/4$)	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ($\phi = f_{EX}/16$)	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

(4) Interruption, reset input ($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH}	$\overline{\text{INT0}}$		1		μs
	t_{IL}	$\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{NMI}}$				
Reset input low level width	t_{RSL}	$\overline{\text{RST}}$		$32/f_c$		μs

Fig. 7. Interruption input timing

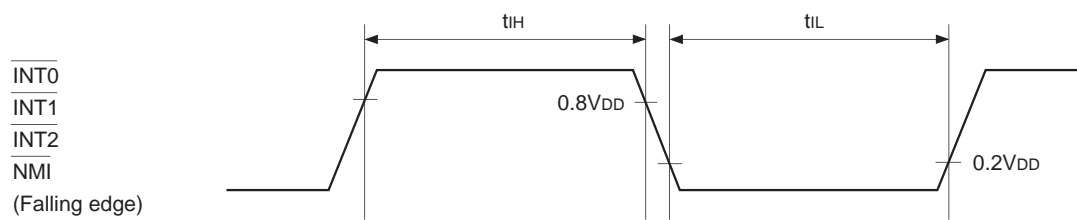
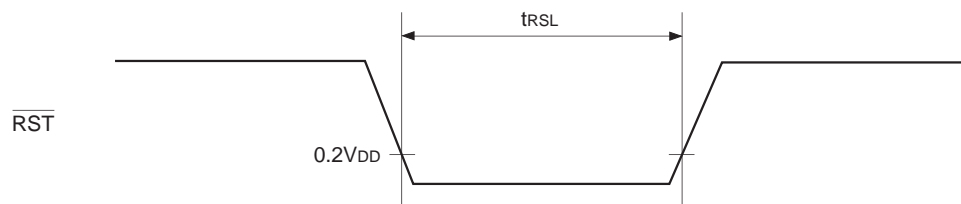


Fig. 8. Reset input timing



Analog Circuit Characteristics

(1) Amplifier circuit reference voltage characteristics

(Ta = -10 to +75°C, V_{DD} = AMPV_{DD} = 5.0V, V_{SS} = AMPV_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Reference level output voltage	V _{OR}	VREFOUT		2.2	2.4	2.6	V
		CTLAG		2.15	2.35	2.55	V
Reference level output current	I _{OR}	VREFOUT	VREFOUT = VREFOUT + 0.5V	3.50	6.5		mA
			VREFOUT = VREFOUT - 0.5V	-0.30	-0.85		mA
		CTLAG	CTLAG = CTLAG + 0.5V	2.80	5.5		mA
			CTLAG = CTLAG - 0.5V	-0.30	-0.85		mA

(2) CTL 1st amplifier characteristics

(Ta = -10 to +75°C, V_{DD} = AMPV_{DD} = 5.0V, V_{SS} = AMPV_{SS} = 0V, CTLAG reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Voltage gain *1	A _{VCTL1}	RECCTL (+) CTLFAMPO*2	Gain = 16dB RECCTL (-) = 0V	12.5	14.5	16.5	dB
			Gain = 27dB RECCTL (-) = 0V	23.5	25.5	27.5	dB
			Gain = 42dB RECCTL (-) = 0V	39.0	41.5	44.0	dB
			Gain = 58dB RECCTL (-) = 0V	54.5	57.0	59.5	dB
Offset voltage	V _{OSCTL1}		CTLAMP (+) and CTLAMP (-) = open	-40	0	+40	mV
Input resistance	R _{INCTL1}	CTLAMP (+)	Charge switch OFF CTLAMP (+) = +0.2V	26.0	44.5		kΩ
		CTLAMP (-)	Charge switch OFF CTLAMP (-) = +0.2V	1.20	2.0		kΩ
Charge switch ON resistance	R _{CCCTL1}	CTLAMP (+)	Charge switch ON CTLAMP (+) = +0.5V		560	1010	Ω
		CTLAMP (-)	Charge switch ON CTLAMP (-) = +0.5V		560	1010	Ω
RECCTL and CTLCIN connection switch ON resistance	R _{READ}	RECCTL (+) CTLCIN (+)	During CTL read operation, CTLCIN (+) - RECCTL (+) = 0.2V	315	400	770	Ω
		RECCTL (-) CTLCIN (-)	During CTL read operation, CTLCIN (-) - RECCTL (-) = 0.2V	315	400	770	Ω
CTLCIN 0V fix switch ON resistance	R _{WRITE}	CTLCIN (+)	During CTL write operation, CTLCIN (+) = AMPV _{SS} + 0.2V		250	310	Ω
		CTLCIN (-)	During CTL write operation, CTLCIN (-) = AMPV _{SS} + 0.2V		250	310	Ω

*1) When CTLCIN (+), CTLAMP (+) pins and CTLCIN (-), CTLAMP (-) pins are AC coupled, and then the signal is input from RECCTL (+) pin.

*2) The result after measuring the CTLFAMPO output waveform or voltage gain.

Note) The gain increases by approximately 1.5dB when the AC coupling capacitor (47μF) is connected to CTLAMP (+) and CTLAMP (-) pins, and the signal is input from CTLAMP (+) and CTLAMP (-) pins.

(3) CTL 2nd amplifier characteristics

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = \text{AMPV}_{DD} = 5.0\text{V}$, $V_{SS} = \text{AMPV}_{SS} = 0\text{V}$, CTLAG reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Voltage gain*1, *2	A _{VCTL2}	CTLSAMPI	Gain = 5dB	4.8	5.8	6.8	dB
			Gain = 11dB	10.4	11.5	12.6	dB
			Gain = 16dB	15.3	16.5	17.7	dB
			Gain = 20dB	19.3	20.5	21.7	dB
LPF cut-off frequency *1, 2	f _{CCTL}		f _{dc} - 3dB	15.0	25.0	40.0	kHz
Offset voltage *2	V _{OSCTL2}		CTLSAMPI = open	-50	0	+50	mV
Comparator level *2	V _{CCTL}		Comparator level = +100mV _{0-p}	70.0	100	130	mV _{0-p}
			Comparator level = +250mV _{0-p}	215	245	275	mV _{0-p}
			Comparator level = +400mV _{0-p}	370	400	430	mV _{0-p}
			Comparator level = -100mV _{0-p}	-70.0	-100	-130	mV _{0-p}
		Comparator level = -250mV _{0-p}	-220	-250	-280	mV _{0-p}	
		Comparator level = -400mV _{0-p}	-370	-400	-430	mV _{0-p}	
		Input resistance	R _{INCTL2}	Charge switch OFF CTLSAMPI = +0.2V	10.0	18.0	
Charge switch ON resistance	R _{CCCTL2}	Charge switch ON CTLSAMPI = +0.5V		770	1140	Ω	

*1) When the signal is input with the AC coupling capacitor (47 μ F) connected to CTLSAMPI pin.

*2) The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

(4) CTLAMP characteristics (1st amplifier + 2nd amplifier)

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = \text{AMPV}_{DD} = 5.0\text{V}$, $V_{SS} = \text{AMPV}_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Voltage gain *1	A _{VCTL}	RECCTL (+)	CTL 1st amplifier gain = 16dB CTL 2nd amplifier gain = 20dB RECCTL (-) = 0V	31.8	35.0	38.2	dB
Input amplitude (peak value)	V _{PKCTL}		RECCTL (-) = 0V			± 300	mV _{0-p}
Input sensitivity	V _{SCTL}		CTL 1st amplifier gain = 58dB CTL 2nd amplifier gain = 20dB Comparator level = +400mV _{0-p} -400mV _{0-p}		0.08	0.10	mV _{0-p}
Input dead band	V _{NSCTL}		RECCTL (-) = 0V	0.015	0.04		mV _{0-p}

*1) As for other combinations of the amplifier gains, CTL 1st amplifier and CTL 2nd amplifier are added respectively.

Note) The result when the signal is input from RECCTL (+) pin with CTL 1st amplifier + CTL 2nd amplifier after performing AC coupling of CTLCIN (+), CTLAMP (+) pins and CTLCIN (-), CTLAMP (-) pins, and CTLFAMPO, CTLSAMPI pins.

(5) CFGAMP characteristics

(Ta = -10 to +75°C, V_{DD} = AMPV_{DD} = 5.0V, V_{SS} = AMPV_{DD} = 0V, VREFOUT reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain *1, *2	AVCFG	CFG	Gain = 0dB	-0.3	0.6	2.2	dB
			Gain = 20dB	19.2	20.8	22.4	dB
			Gain = 34dB	33.2	34.8	36.4	dB
			Gain = 38dB	37.0	38.7	40.4	dB
LPF cut-off frequency *1, *2	fCCFG		f _{DC} - 3dB	30.0	55.0	80.0	kHz
Offset voltage *2	VOFCFG		CFG = open	-50	0	+50	mV
Comparator judgment level width *2	VCCFG		Comparator schmitt width = 320mVp-p	260	320	360	mVp-p
			Comparator schmitt width = 160mVp-p	110	155	200	mVp-p
Input sensitivity *1	VSCFG		Gain = 38dB Comparator level = 320mVp-p		4.20	5.00	mVp-p
			Gain = 38dB Comparator level = 160mVp-p		2.10	2.40	mVp-p
Input dead band *1	VNSCFG		Gain = 38dB Comparator level = 320mVp-p	3.40	4.10		mVp-p
			Gain = 38dB Comparator level = 160mVp-p	1.50	2.00		mVp-p
Input resistance	RINCFG	Charge switch OFF CFG = +0.2V	5.5	8.3		kΩ	
Charge switch ON resistance	RCCFG	Charge switch ON CFG = +0.5V		455	710	Ω	
Digital output waveform duty *1, *3	DTYCFG	CFG = sine wave with 50% duty	48.0	50.0	52.0	%	
Input amplitude (peak value) *1	VPKCFG				±2.4	V _{0-p}	

*1) When the signal is input with the AC coupling capacitor (47μF) connected to CFG pin.

*2) The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

*3) The result after measuring the digital signal waveform output from the amplifier circuit.

(6) DFGAMP characteristics

(Ta = -10 to +75°C, VDD = AMPVDD = 5.0V, VSS = AMPVSS = 0V, VREFOUT reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain *1, *2	AVDFG	DFG	Gain = 0dB	-0.3	0.6	2.2	dB
			Gain = 20dB	19.2	20.8	22.4	dB
			Gain = 34dB	33.2	34.8	36.4	dB
			Gain = 38dB	37.0	38.7	40.4	dB
LPF cut-off frequency *1, *2	fCDFG		fbc - 3dB	30.0	55.0	80.0	kHz
Offset voltage *2	VOSDFG		DFG = open	-50	0	+50	mV
Comparator judgment level width *2	V_CDFG		Comparator schmitt width = 320mVp-p	260	320	360	mVp-p
			Comparator schmitt width = 160mVp-p	110	155	200	mVp-p
Input sensitivity *1	V_SDFG		Gain = 38dB Comparator level = 320mVp-p		4.20	5.00	mVp-p
			Gain = 38dB Comparator level = 160mVp-p		2.10	2.40	mVp-p
Input dead band *1	V_NSDFG		Gain = 38dB Comparator level = 320mVp-p	3.40	4.10		mVp-p
			Gain = 38dB Comparator level = 160mVp-p	1.50	2.00		mVp-p
Input resistance	R_INDFG	Charge switch OFF DFG = +0.2V	5.5	8.3		kΩ	
Charge switch ON resistance	R_CDFG	Charge switch ON DFG = +0.5V		455	710	Ω	
Digital output waveform duty *1, 3	D_TYDFG	CFG = sine wave of 50% duty	48.0	50.0	52.0	%	
Input amplitude (peak value) *1	V_PKDFG				±2.4	V _{0-p}	

*1) When the signal is input with the AC coupling capacitor (47μF) connected to DFG pin.

*2) The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

*3) The result after measuring the digital signal waveform output from the amplifier circuit.

(7) DPGAMP characteristics

(Ta = -10 to +75°C, VDD = AMPVDD = 5.0V, VSS = AMPVSS = 0V, VREFOUT reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain *1, *2	AVDPG	DPG		11.1	12.0	13.2	dB
LPF cut-off frequency *1, *2	fCDPG		fDC - 3dB	30.0	55.0	85.0	kHz
Offset voltage *2	VOsDPG		DFG = open	-35	0	+35	mV
Comparator level *2	VCDPG		Comparator level = 600mV _{0-p}	570	605	640	mV _{0-p}
			Comparator level = 400mV _{0-p}	370	400	432	mV _{0-p}
			Comparator level = 200mV _{0-p}	175	200	220	mV _{0-p}
			Comparator level = 100mV _{0-p}	72	100	125	mV _{0-p}
			Comparator level = -600mV _{0-p}	-572	-605	-643	mV _{0-p}
			Comparator level = -400mV _{0-p}	-368	-400	-438	mV _{0-p}
			Comparator level = -200mV _{0-p}	-174	-200	-223	mV _{0-p}
			Comparator level = -100mV _{0-p}	-71	-100	-124	mV _{0-p}
Input sensitivity *1	VSDPG		Comparator level = 600mV _{0-p} , 200mV _{0-p}		150	180	mV _{0-p}
			Comparator level = 400mV _{0-p} , 100mV _{0-p}		100	120	mV _{0-p}
			Comparator level = -600mV _{0-p} , -200mV _{0-p}		-155	-185	mV _{0-p}
			Comparator level = -400mV _{0-p} , -100mV _{0-p}		-109	-130	mV _{0-p}
Input dead band *1	VNSDPG		Comparator level = 600mV _{0-p} , 200mV _{0-p}	113	142		mV _{0-p}
			Comparator level = 400mV _{0-p} , 100mV _{0-p}	70	90		mV _{0-p}
			Comparator level = -600mV _{0-p} , -200mV _{0-p}	-120	-150		mV _{0-p}
			Comparator level = -400mV _{0-p} , -100mV _{0-p}	-80	-103		mV _{0-p}
Input resistance	RINDPG		Charge switch OFF DPG = +0.2V	24.0	44.5		kΩ
Charge switch ON resistance	RCDPG	Charge switch ON DPG = +0.5V		450	860	Ω	
Input amplitude (peak value) *1	VPKDPG				±2.4	V	

*1) When the signal is input with the AC coupling capacitor (47μF) connected to DPG pin.

*2) The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

(8) CTL write circuit characteristics(Ta = -10 to +75°C, V_{DD} = AMPV_{DD} = 5.0V, V_{SS} = AMPV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Output resistance	R _{OH}	RECCAP	RECCAP = AMPV _{DD} - 0.5V	450	625	1005	Ω
	R _{OL}		RECCAP = AMPV _{DD} + 0.5V	410	555	840	Ω
Output current *1	I _{OREC}	RECCTL (+) RECCTL (-)	Write current = 2.0mA	1.3	2.0	2.9	mA
			Write current = 2.5mA	1.7	2.5	3.7	mA
			Write current = 3.0mA	2.1	3.1	4.5	mA
			Write current = 3.5mA	2.6	3.6	5.2	mA
			Write current = 4.0mA	2.9	4.0	5.9	mA
			Write current = 4.5mA	3.3	4.6	6.6	mA
			Write current = 5.0mA	3.7	5.1	7.2	mA
			Write current = 5.5mA	4.0	5.6	8.0	mA
Write current = 6.0mA	4.4	6.1	8.9	mA			

*1) The current value which flows when RECCTL (+) pin and RECCTL (-) pin are shorted.

(9) Amplifier operating current characteristics(Ta = -10 to +75°C, V_{DD} = AMPV_{DD} = 5.0V, V_{SS} = AMPV_{SS} = 0V reference)

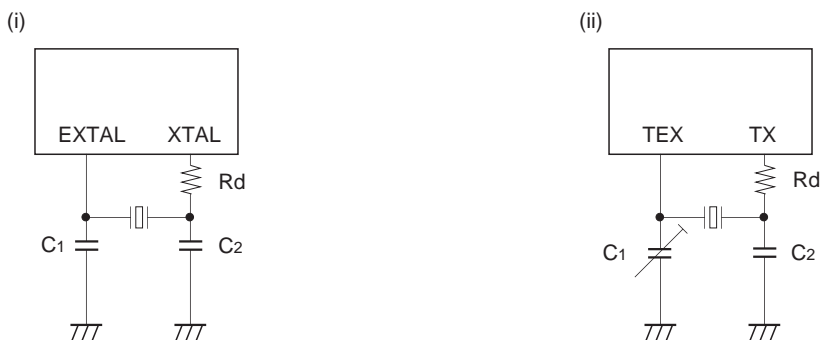
Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Amplifier operating current	I _{AMP}	AMPV _{DD}	When the amplifier is operating *1		7.6	12.0	mA
			When the amplifier is not operating			10	μA

*1) The CTL recording current is added during CTL write.

Note) The amplifier operation and NOT-operation is controlled according to the contents of amplifier power supply control register (ASWC: 05E2H) bits 5, 4, 1 and 0.

Supplement

Fig. 9. Recommended oscillation circuit



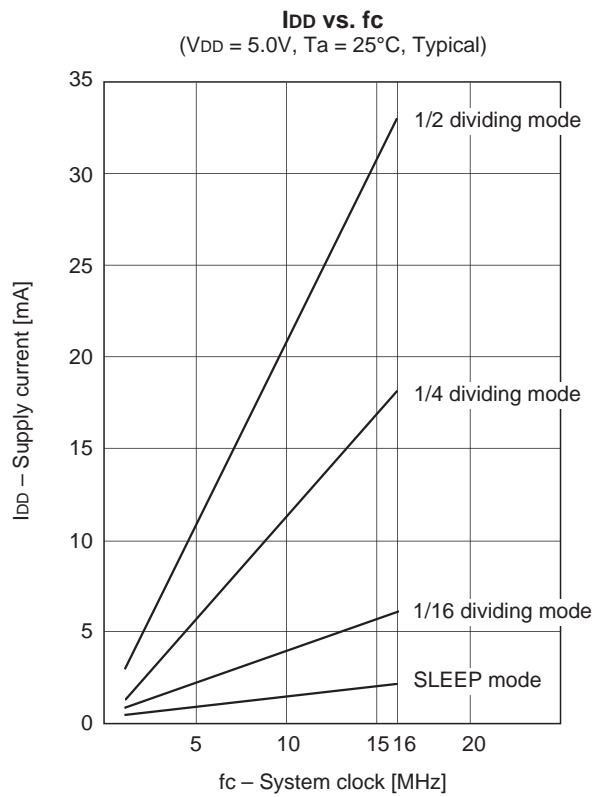
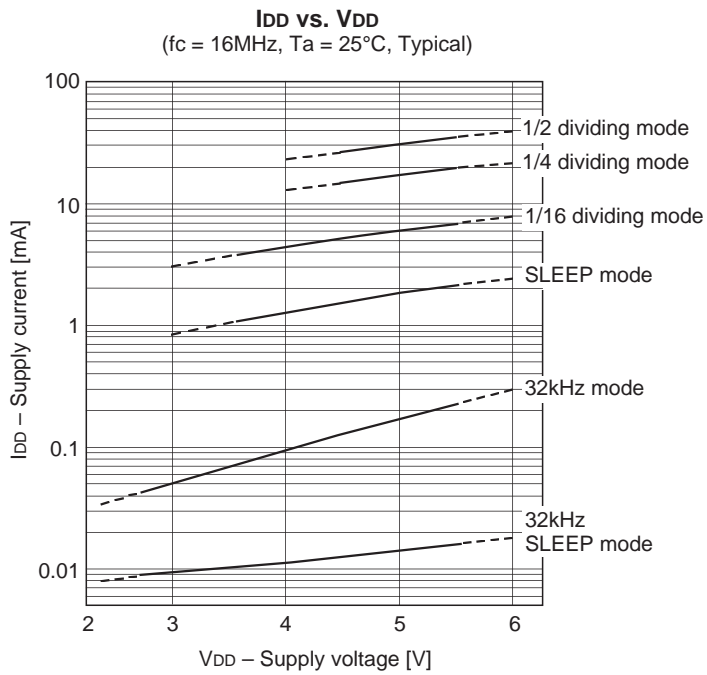
Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

Mask option table

Item	Mask product	CXP888P60Q-1-□□□	CXO888P60Q-2-□□□
Reset pin pull-up resistor	Existent/Non-existent	Existent	Existent
Input circuit format*1	CMOS schmitt/ TTL schmitt	TTL schmitt	TTL schmitt
Power-on-reset circuit	Existent (CXP88616/24) Non-existent (CXP88732/40/48, CXP88852/60)	Non-existent	Existent

*1) The input circuit format can be selected for PE3/SYNC pin.

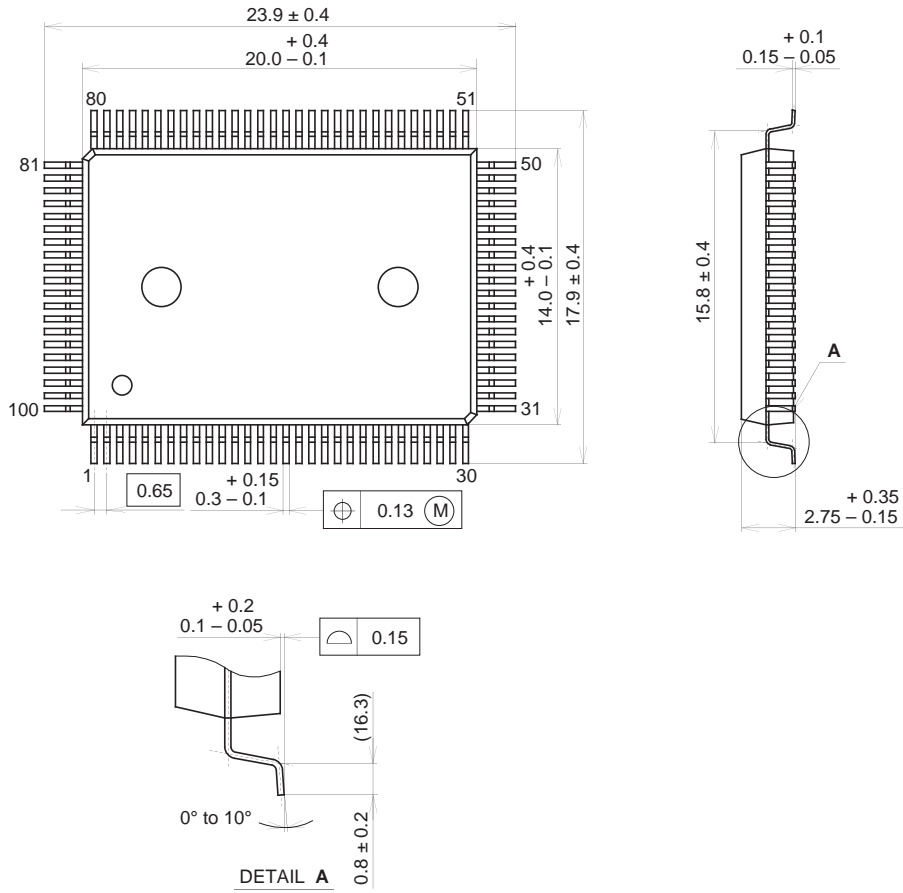
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g



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