SONY

CXP884P60

CMOS 8-bit Single Chip Microcomputer

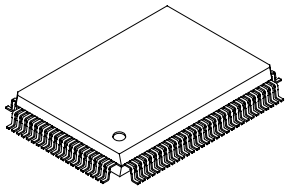
Description

The CXP884P60 is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time-base timer, high precision timing pattern generation circuit, PWM output, VISS/VASS circuit, 32kHz timer/counter, remote control receiving circuit, VSYNC separator and the measurement circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also, the CXP884P60 provides sleep/stop functions which enable to lower power consumption.

This IC is the PROM-incorporated version of the CXP88460 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

100 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

Features

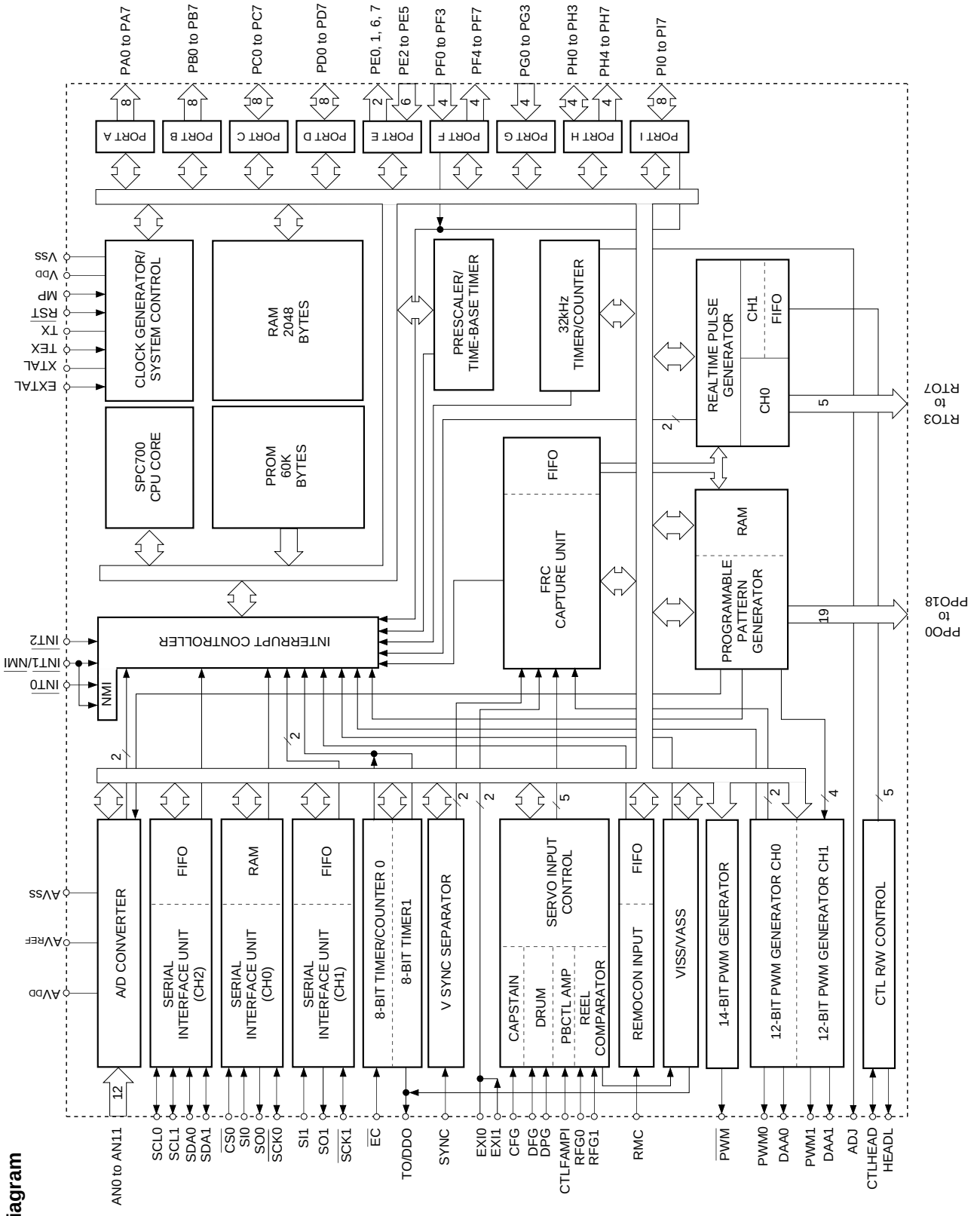
- A wide instruction set (213 instructions) which covers various types of data
  — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle 250ns at 16MHz operation
  122µs at 32kHz operation
- Incorporated PROM capacity 60K bytes
- Incorporated RAM capacity 2048 bytes
- Peripheral functions

— A/D converter	8 bits, 12 channels, successive approximation system (Conversion time of 20µs/16MHz)
— Serial interface	Incorporated 8-bit, 8-stage FIFO (Auto transfer for 1 to 8 bytes), 1 channel Incorporated buffer RAM (Auto transfer for 1 to 32 bytes), 1 channel Incorporated two-wire 8-bit and 8-stage FIFO (Auto transfer for 1 to 8 bytes), 1 channel
— Timer	8-bit timer/counter, 2 channels 19-bit time-base timer 32kHz timer/counter
— High precision timing pattern generation circuit	PPG: Maximum of 19 pins 32 stages programmable RTG: 5 pins, 1 channel 7-bit, 10-stage FIFO (RECCTL control/ATC control), 1 channel
— PWM/DA gate output	12 bits, 2 channels (Repetitive frequency 62.5kHz at 16MHz) DA gate pulse output: 13 bits, 2 channels
— Analog signal input circuit	PBCTL amplifier circuit Reel FG comparator
— CTL write/rewrite circuit	Recording current control circuit
— Servo input control	Capstan FG, Drum FG/PG, CTL, Reel FG input
— VSYNC separator	
— FRC capture unit	Incorporated 26-bit and 8-stage FIFO
— PWM output	14 bits, 1 channel
— VISS/VASS circuit	Pulse duty auto detection circuit
— Remote control receiving circuit	8-bit pulse measurement counter, 6-stage FIFO
— Tri-state output	PPG output 2 pins
— High speed head switching circuit	

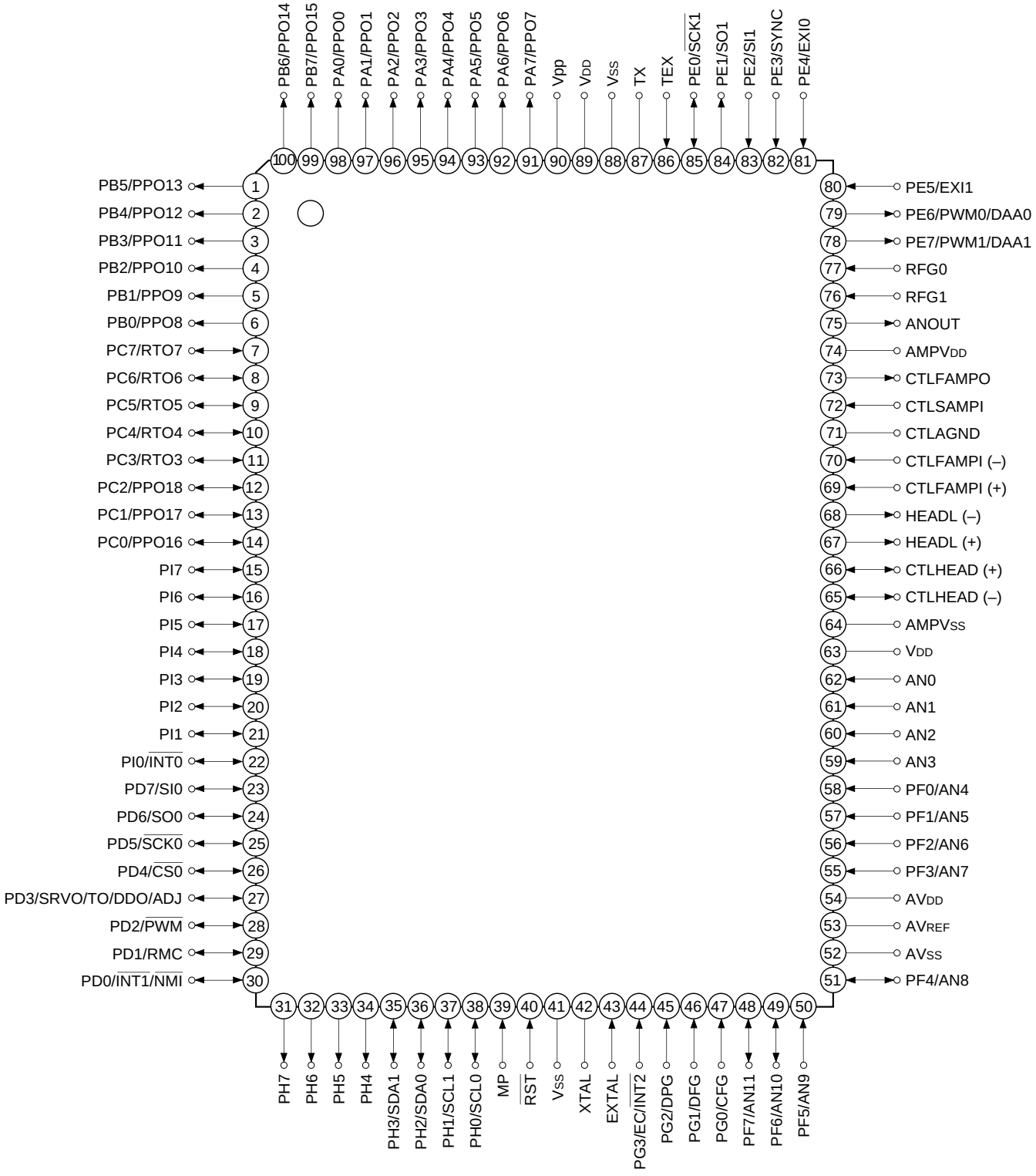
- Interruption 22 factors, 15 vectors, multi-interruption possible
- Standby mode Sleep/stop
- Package 100-pin plastic QFP
- Piggy/evaluation chip CXP88400 100-pin ceramic PQFP

E01432-PS

Block Diagram



Pin Assignment (Top View)



Note) 1. Vpp (Pin 90) is always connected to V_{DD}.
2. V_{DD} (Pins 63 and 89) are both connected to V_{DD}
3. Vss (Pins 41 and 88) are both connected to GND.
4. MP (Pin 39) is always connected to GND.

Pin Description

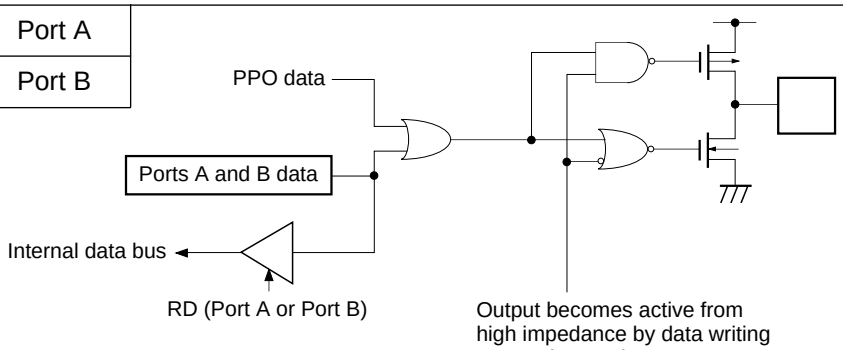
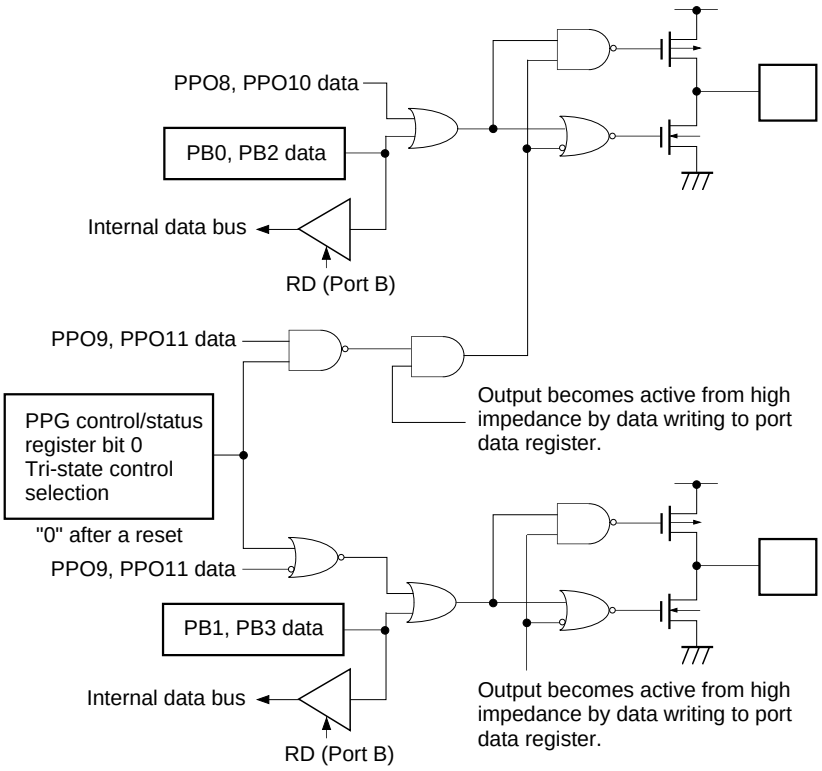
<table>
<tr><th>Symbol</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td>PA0/PPO0
to
PA7/PPO7</td><td>Output/
Real-time output</td><td>(Port A)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td><td colspan="2">Head switching output.</td></tr>
<tr><td>PB0/PPO8
to
PB7/PPO15</td><td>Output/
Real-time output</td><td>(Port B)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td><td colspan="2" rowspan="2">Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port.
(19 pins)
PB0 and PB2 can be tri-state controlled with PPG.</td></tr>
<tr><td>PC0/PPO16
to
PC2/PPO18</td><td>I/O/
Real-time output</td><td rowspan="2">(Port C)
8-bit I/O port. I/O can be specified in 1-bit units. Data is gated with PPO or RTO contents by OR-gate and they are output.
(8 pins)</td></tr>
<tr><td>PC3/RTO3
to
PC7/RTO7</td><td>I/O/
Real-time output</td><td colspan="2">Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. PC3 can be tri-state controlled with RTG.
(5 pins)</td></tr>
<tr><td>PD0/$\overline{\text{INT1}}$/
$\overline{\text{NMI}}$</td><td>I/O/Input/Input</td><td rowspan="8">(Port D)
8-bit I/O port. I/O can be specified in 1-bit units.
(8 pins)</td><td colspan="2">Input pin to request external interruption and non-maskable interruption.</td></tr>
<tr><td>PD1/RMC</td><td>I/O/Input</td><td colspan="2">Remote control receiving circuit input pin.</td></tr>
<tr><td>PD2/$\overline{\text{PWM}}$</td><td>I/O/Output</td><td colspan="2">14-bit PWM output pin.</td></tr>
<tr><td>PD3/TO
DDO/ADJ
SRVO</td><td>I/O/Output/Output/
Output/Output</td><td colspan="2">Timer/counter, CTL duty detector, 32kHz oscillation adjustment and servo amplifier output pin.</td></tr>
<tr><td>PD4/$\overline{\text{CS0}}$</td><td>I/O/Input</td><td colspan="2">Serial chip select (CH0) input pin.</td></tr>
<tr><td>PD5/$\overline{\text{SCK0}}$</td><td>I/O/I/O</td><td colspan="2">Serial clock (CH0) I/O pin.</td></tr>
<tr><td>PD6/SO0</td><td>I/O/Output</td><td colspan="2">Serial data (CH0) output pin.</td></tr>
<tr><td>PD7/SI0</td><td>I/O/Input</td><td colspan="2">Serial data (CH0) input pin.</td></tr>
<tr><td>PE0/$\overline{\text{SCK1}}$</td><td>Output/I/O</td><td rowspan="9">(Port E)
8-bit port. Bits 2, 3, 4 and 5 are for inputs; bits 0, 1, 6 and 7 are for outputs.
(8 pins)</td><td colspan="2">Serial clock (CH1) I/O pin.</td></tr>
<tr><td>PE1/SO1</td><td>Output/Output</td><td colspan="2">Serial data (CH1) output pin.</td></tr>
<tr><td>PE2/SI1</td><td>Input/Input</td><td colspan="2">Serial data (CH1) input pin.</td></tr>
<tr><td>PE3/SYNC</td><td>Input/Input</td><td colspan="2">Composite sync signal input pin.</td></tr>
<tr><td>PE4/EXI0</td><td>Input/Input</td><td colspan="2" rowspan="2">External input pin for FRC capture unit.
(2 pins)</td></tr>
<tr><td>PE5/EXI1</td><td>Input/Input</td></tr>
<tr><td>PE6/PWM0/
DAA0</td><td>Output/Output</td><td rowspan="2">PWM output pin.
(2 pins)</td><td rowspan="2">DA gate pulse output pin.
(2 pins)</td></tr>
<tr><td>PE7/PWM1/
DAA1</td><td>Output/Output</td></tr>
</table>

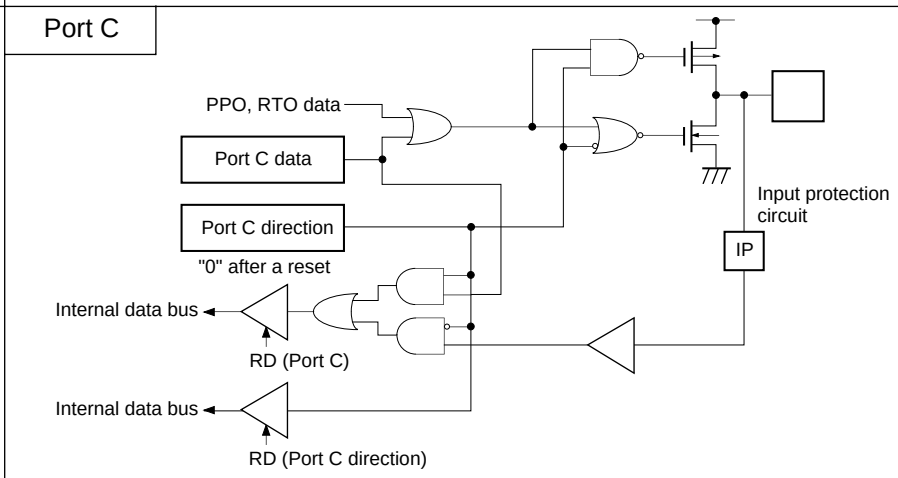
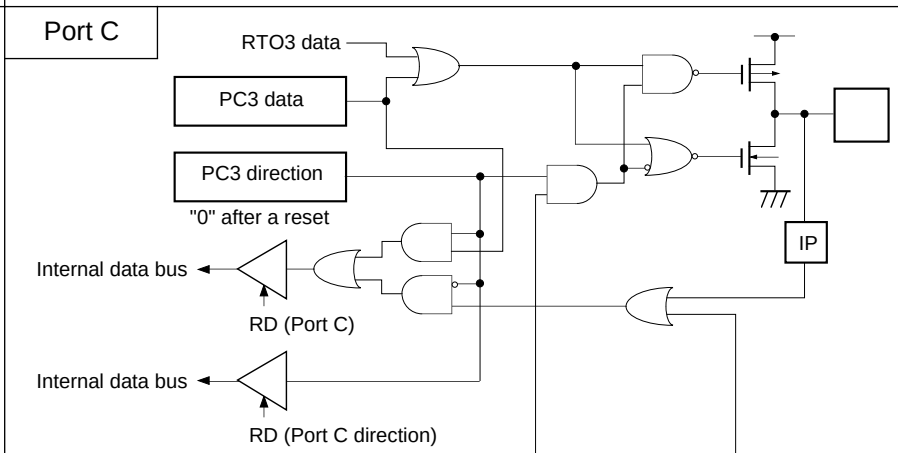
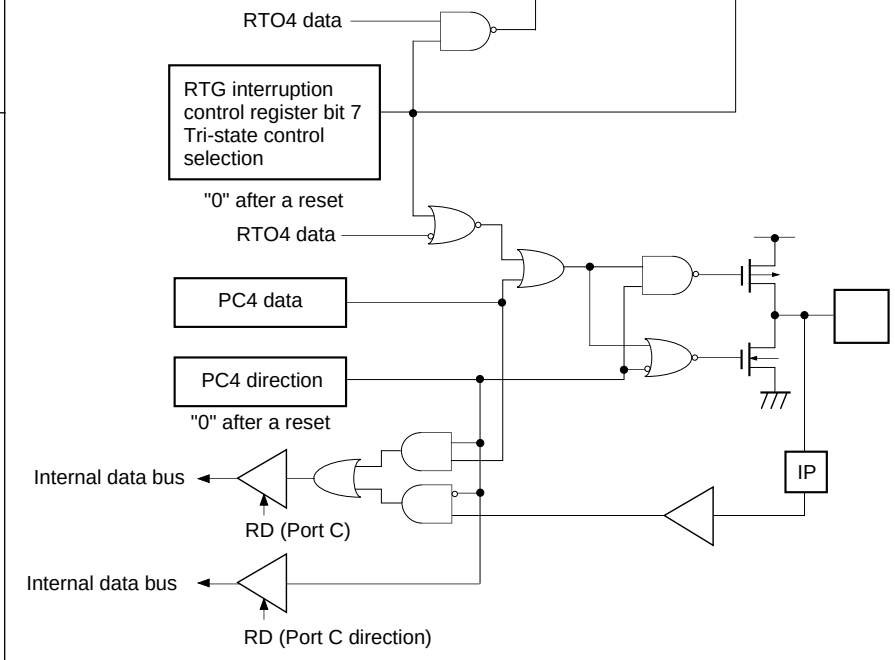
Description	I/O	Description		
AN0 to AN3	Input			
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are for inputs; upper 4 bits are for outputs. Lower 4 bits also serve as standby release input pins. (8 pins)		Analog input pin to A/D converter. (12 pins)
PF4/AN8 to PF7/AN11	Output/Input			
PG0/CFG	Input/Input	(Port G) 4-bit input port. (4 pins)	Capstan FG input pin.	
PG1/DFG			Drum FG input pin.	
PG2/DPG			Drum PG input pin.	
PG3/$\overline{EC}$/$\overline{INT2}$	Input/Input/Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PH0/SCL0 PH1/SCL1	I/O/I/O	(Port H) 8-bit I/O port. Upper four bits are for outputs. I/O can be specified in 1-bit units for lower four bits. Lower four bits are N-ch open drain outputs and which can drive 12mA sink current. Upper four bits are for outputs; N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)	Serial clock (CH2) I/O pin.	
PH2/SDA0 PH3/SDA1			Serial data (CH2) I/O pin.	
PH4 to PH7	Output			
PI0/$\overline{INT0}$	I/O/Input	(Port I) 8-bit I/O port. I/O can be specified in 1-bit units. Function as standby release input can be specified in 1-bit units. (8 pins)	Input pin to request external interruption. Active when falling edge.	
PI1 to PI7	I/O			
RFG0, RFG1	Input	Input ports. (2 pins)	Reel FG input pin.	
ANOUT	Output	Output port. (1 pin)	Internal waveform output pin of analog circuit.	
CTLFAMPO	Output	Output port. (1 pin)	PBCTL signal 1st amplifier output pin.	
CTLSAMPI	Input	Input port. (1 pin)	PBCTL signal 2nd amplifier input pin.	
CTLAGND	Output	Output port. (1 pin)	Smoothing capacitor connecting pin.	
CTLFAMPI (–) CTLFAMPI (+)	Input	Input ports. (2 pins)	Input PBCTL signal with capacitor coupled.	
HEADL (–) HEADL (+)	Output	Output ports. (2 pins)	During playback, connect to CTLHEAD (–) and CTLHEAD (+) with internal switch.	
CTLHEAD (–) CTLHEAD (+)	I/O	I/O ports. (2 pins)	During playback, input pin of PBCTL signal; during recording, output pin of PBCTL signal.	
$AMPV_{SS}$		Analog signal input circuit GND pin.		
$AMPV_{DD}$		Analog signal input circuit power supply pin.		

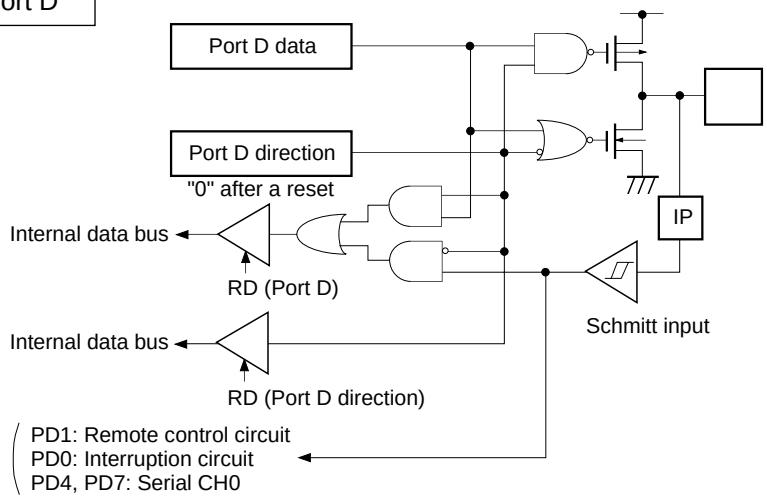
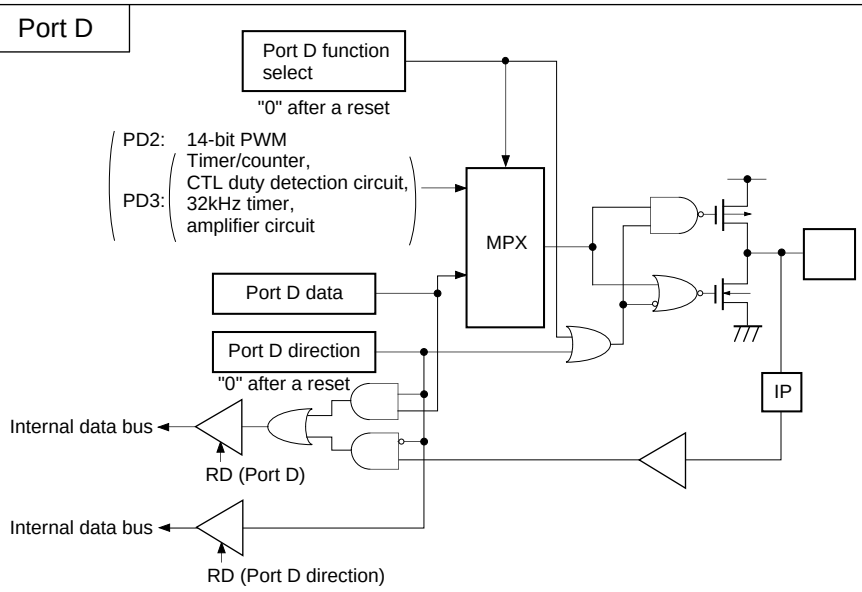
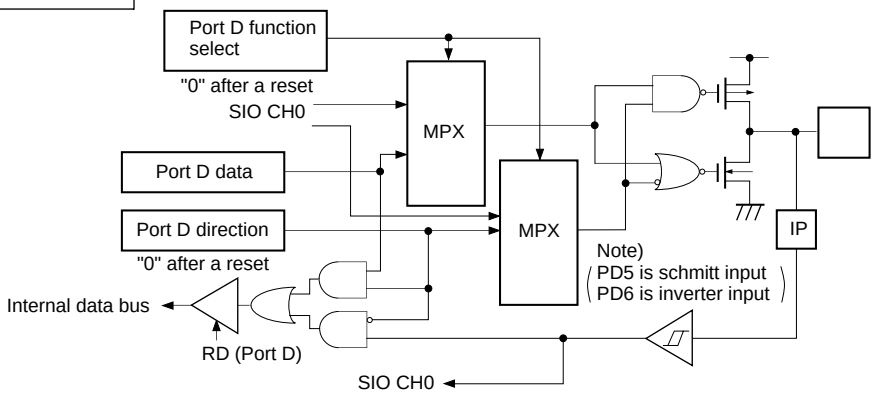
Symbol	I/O	Description
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input it to EXTAL pin and input the opposite phase clock to XTAL pin.
XTAL	Output	
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (In this time, feedback resistor is not removed.)
TX	Output	
$\overline{RST}$	Input	System reset pin; active at low level.
Vpp		Positive power supply pin for incorporated PROM write. Connect this pin to V_{DD} for normal operation.
MP	Input	Test mode input pin. Always connect to GND.
AV_{DD}		Positive power supply pin of A/D converter.
AV_{REF}	Input	Reference voltage input pin of A/D converter.
AV_{SS}		GND pin of A/D converter.
V_{DD}		Positive power supply pin.
V_{SS}		GND pin. Connect both Vss pins to GND.

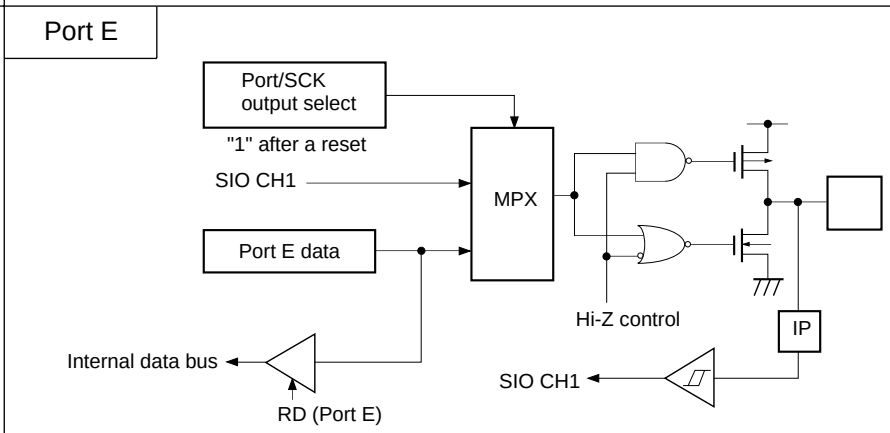
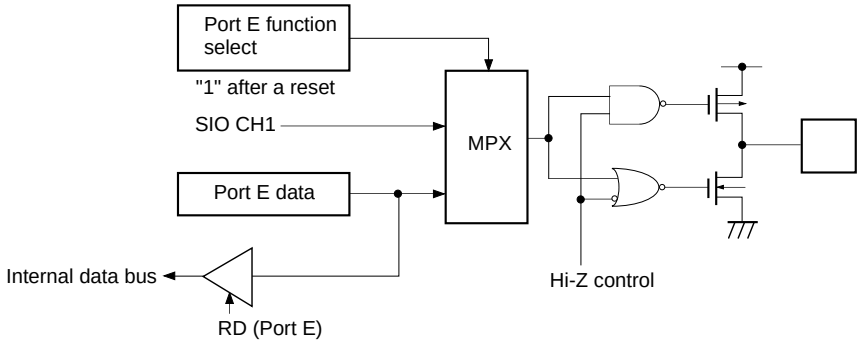
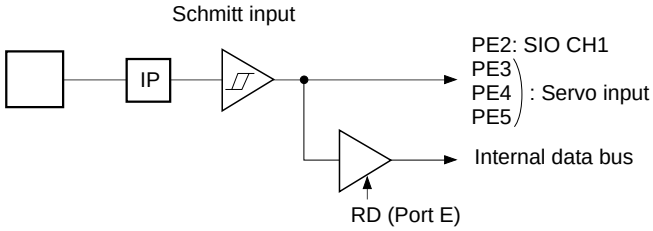
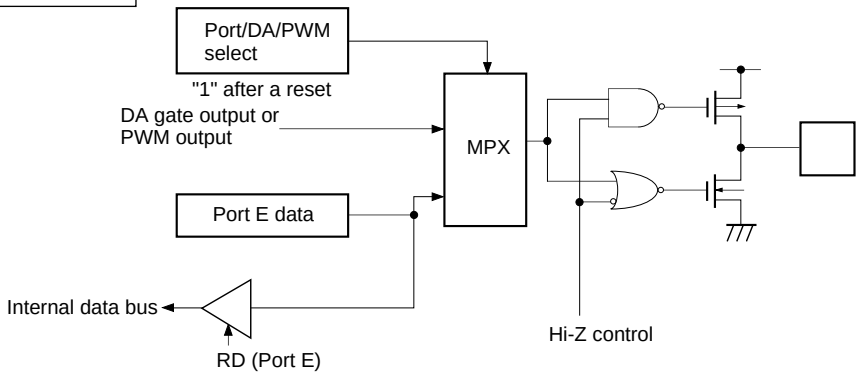
Input/Output Circuit Formats for Pins

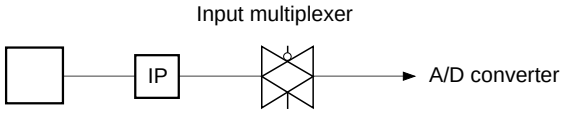
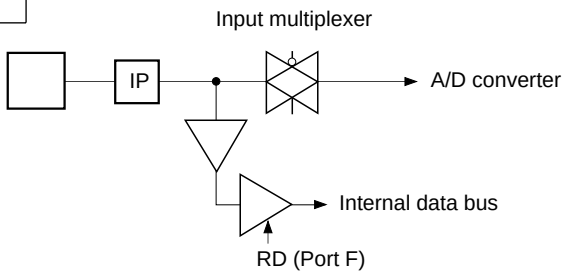
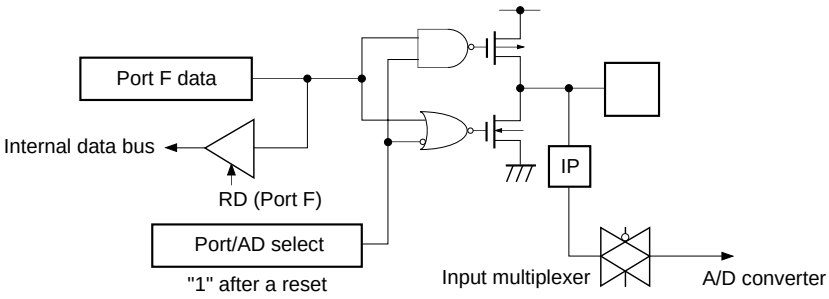
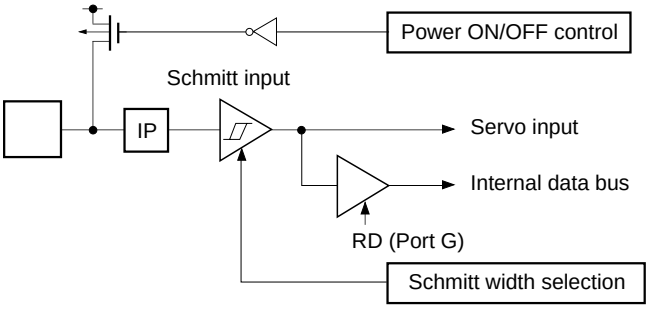
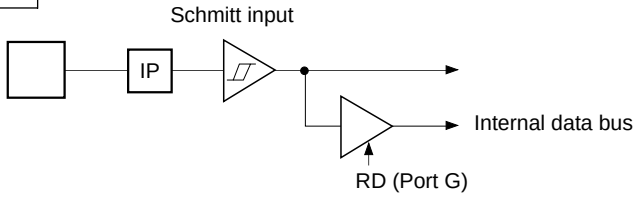
<table>
<tr><th>Pin</th><th>Circuit format</th><th>After a reset</th></tr>
<tr><td>PA0/PPO0
to
PA7/PPO7

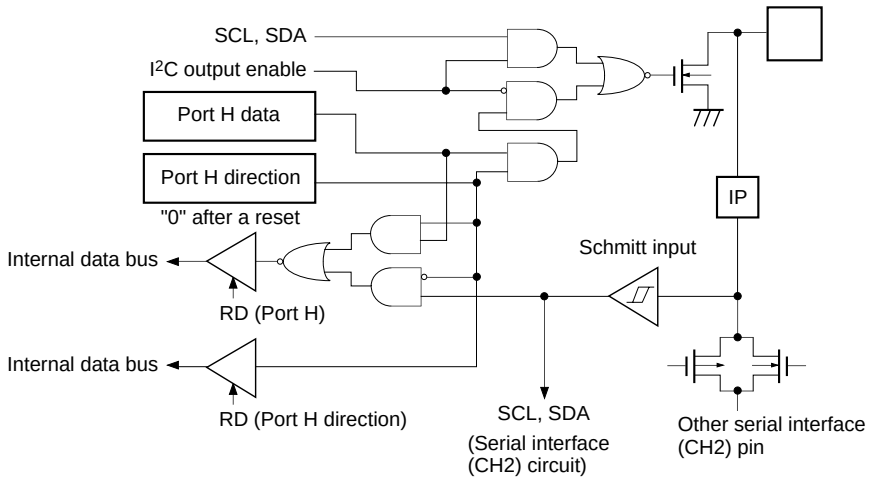
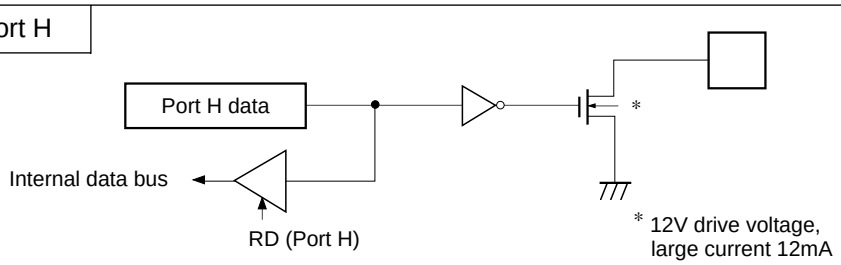
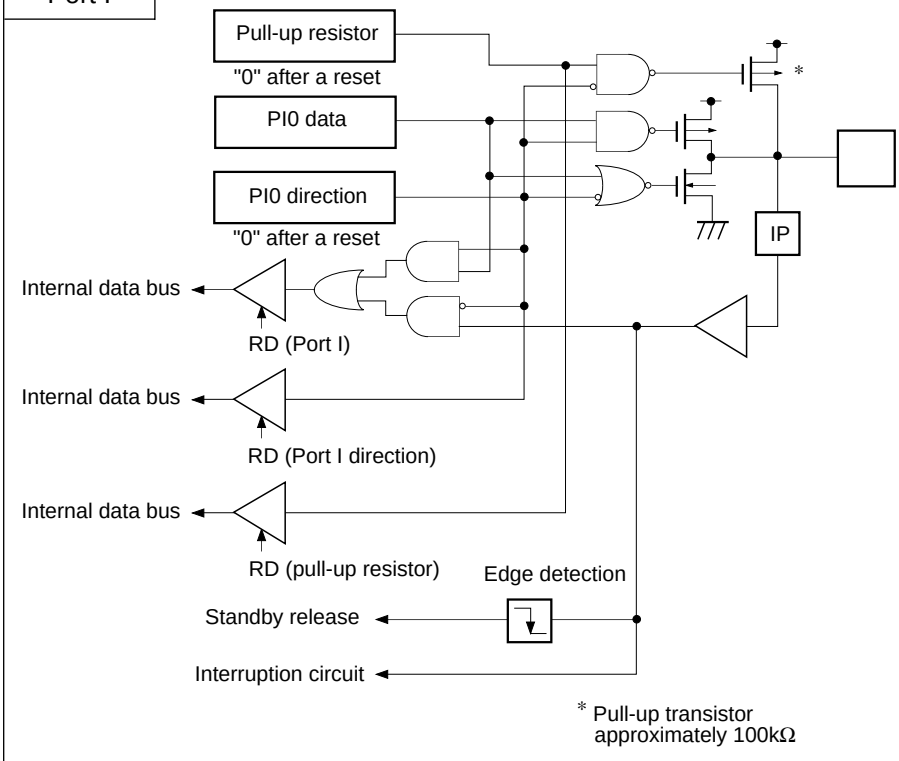
PB4/PPO12
to
PB7/PPO15</td><td>Port A
Port B
 
</td><td>Hi-Z</td></tr>
<tr><td>PB0/PPO8
PB2/PPO10</td><td rowspan="2">Port B
 
</td><td>Hi-Z</td></tr>
<tr><td>PB1/PPO9
PB3/PPO11</td><td>Hi-Z</td></tr>
</table>

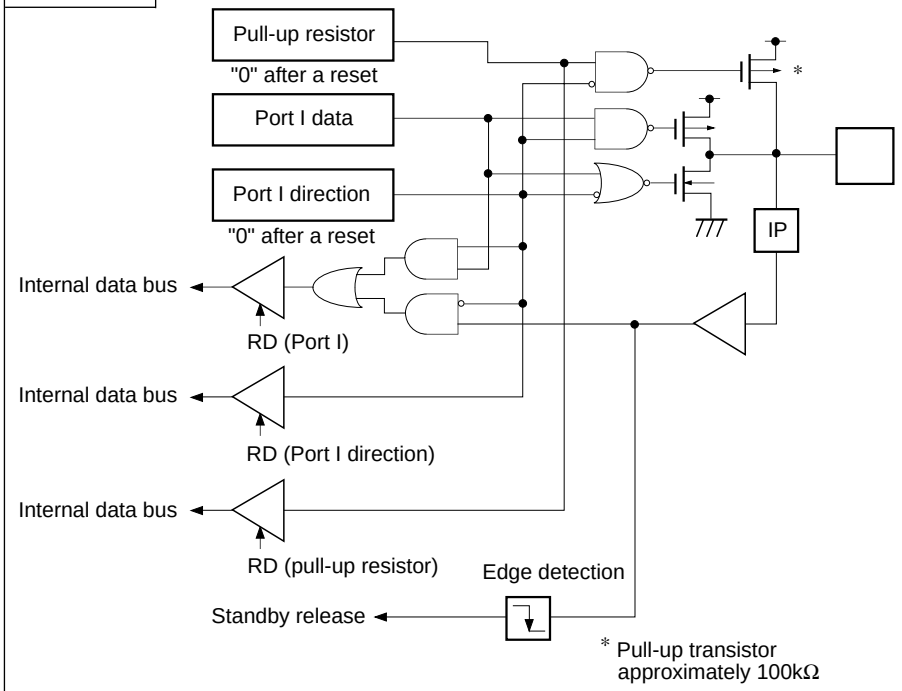
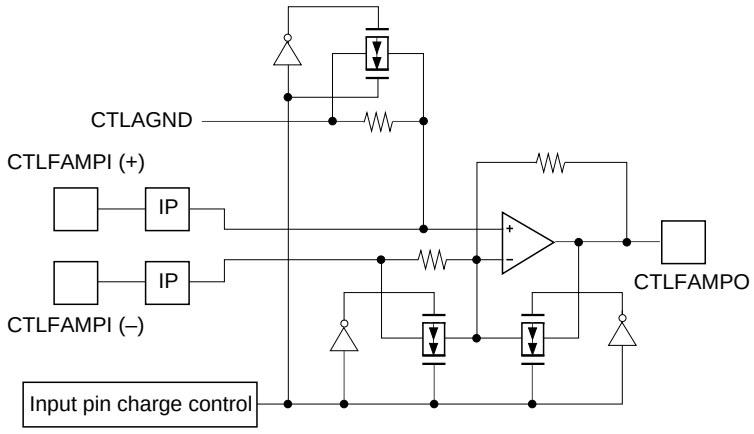
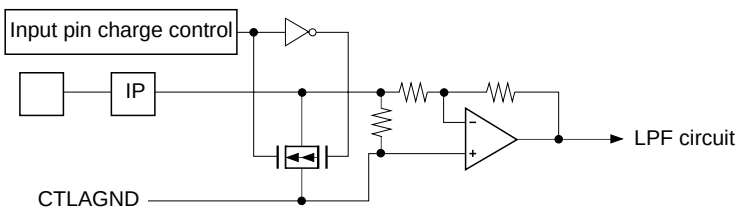
Pin	Circuit format	After a reset
PC0/PPO16 to PC2/PPO18 PC5/RTO5 to PC7/RTO7	Port C 	Hi-Z
PC3/RTO3	Port C 	Hi-Z
PC4/RTO4		Hi-Z

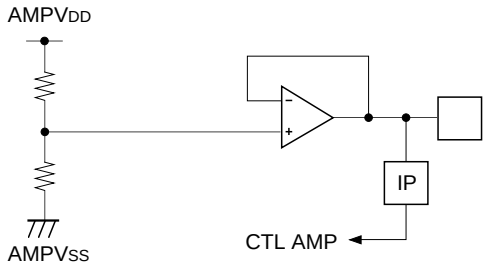
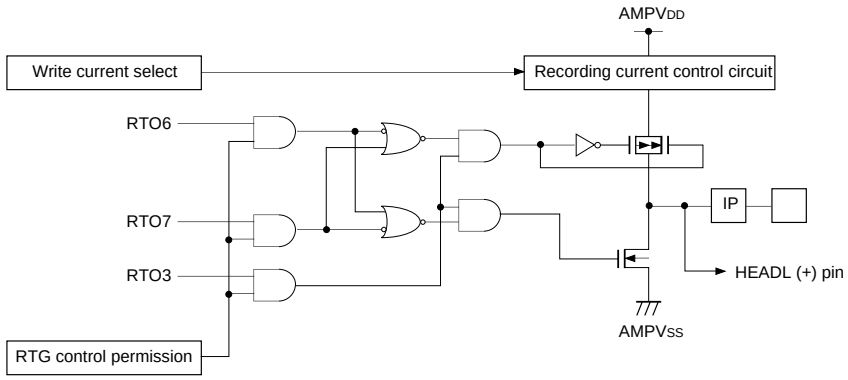
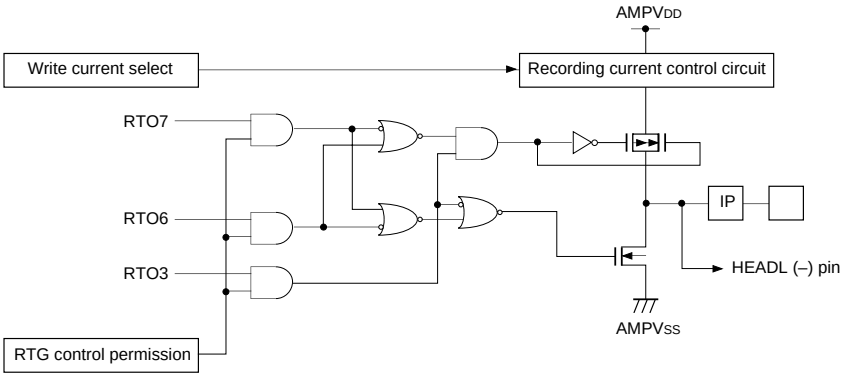
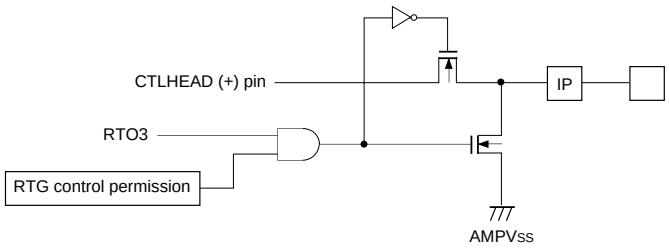
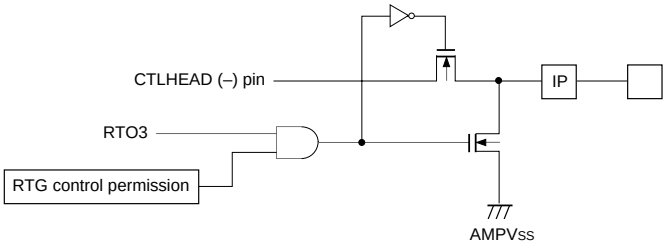
Pin	Circuit format	After a reset
PD0/$\overline{INT1}$/$\overline{NMI}$ PD1/$\overline{RMC}$ PD4/$\overline{CS0}$ PD7/SI0	Port D 	Hi-Z
PD2/$\overline{PWM}$ PD3/SRVO/ TO/DDO/ ADJ	Port D 	Hi-Z
PD5/$\overline{SCK0}$ PD6/SO0	Port D 	Hi-Z

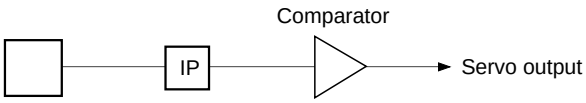
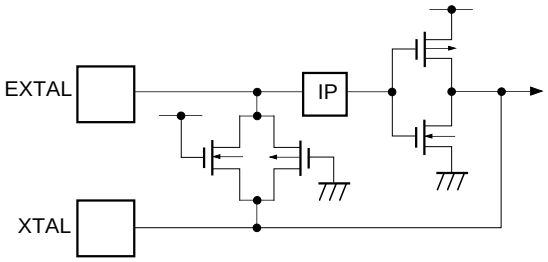
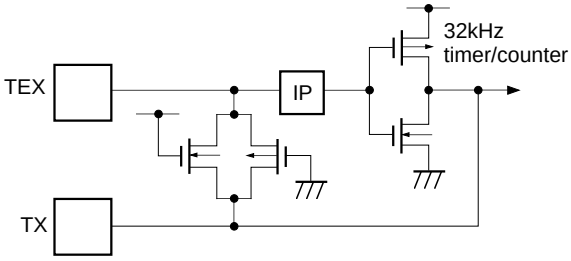
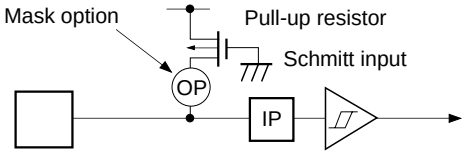
Pin	Circuit format	After a reset
PE0/$\overline{\text{SCK1}}$	Port E 	Hi-Z
PE1/SO1	Port E 	Hi-Z
PE2/SI1 PE3/SYNC PE4/EXI0 PE5/EXI1	Port E  Note) For PE3/SYNC, CMOS schmitt input or TTL schmitt input can be selected with the mask option.	Hi-Z
PE6/PWM0/ DAA0 PE7/PWM1/ DAA1	Port E 	High level

Pin	Circuit format	After a reset
AN0 to AN3		Hi-Z
PF0/AN4 to PF3/AN7	Port F 	Hi-Z
PF4/AN8 to PF7/AN11	Port F 	Hi-Z
PG0/CFG PG1/DFG PG2/DPG	Port G 	Hi-Z
PG3/$\overline{EC}$/$\overline{INT2}$	Port G 	Hi-Z

Pin	Circuit format	After a reset
PH0/SCL0 PH1/SCL1 PH2/SDA0 PH3/SDA1	Port H 	Hi-Z
PH4 to PH7	Port H 	Hi-Z
PI0/$\overline{\text{INT0}}$	Port I 	Hi-Z

Pin	Circuit format	After a reset
PI1 to PI7	Port I 	Hi-Z
CTLFAMPI (+) CTLFAMPI (–) CTLFAMPO		1/2AMPV$_{DD}$
CTLSAMPI		1/2AMPV$_{DD}$

Pin	Circuit format	After a reset
CTLAGND		1/2AMPVDD
CTLHEAD (+)		Hi-Z
CTLHEAD (–)		Hi-Z
HEADL (+)		Hi-Z
HEADL (–)		Hi-Z

Pin	Circuit format	After a reset
RFG0 RFG1		Hi-Z
EXTAL XTAL	 • Shows the circuit composition during oscillation. • Feedback resistor is removed and XTAL outputs High level during stop.	Oscillation
TEX TX	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At that time, TEX outputs Low level and TX outputs High level.	Oscillation
$\overline{\text{RST}}$		Low level (during a reset)

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13	V	PROM incorporated version
	AV_{DD}	AVss to +7.0*1	V	
	AV_{SS}	–0.3 to +0.3	V	
	$AMPV_{DD}$	$AMPV_{SS}$ to +7.0*2	V	
	$AMPV_{SS}$	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*3	V	
Output voltage	V_{OUT}	–0.3 to +7.0*3	V	
Medium drive output voltage	V_{OUTP}	–0.3 to +15.0	V	Port H (PH7 to PH4) pin
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Other than large current output ports (value per pin)
	I_{OLC}	20	mA	Large current output port*4 (value per pin)
Low level total output current	$\sum I_{OL}$	130	mA	Total of output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package type

*1 AV_{DD} should not exceed V_{DD} + 0.3V.

*2 $AMPV_{DD}$ should not exceed V_{DD} + 0.3V.

*3 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*4 The large current output port is port H (PH7 to PH4).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clock
		3.5	5.5		Guaranteed operation range for 1/16 frequency dividing clock or during sleep mode
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during stop
	Vpp	Vpp = V_{DD}		V	*8
Analog supply voltage	AV_{DD}	4.5	5.5	V	*1
	$AMPV_{DD}$	4.5	5.5	V	*2
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*3
	V_{IHS}	0.8V_{DD}	V_{DD}	V	CMOS schmitt input*4
	V_{IHTS}	2.2	V_{DD}	V	TTL schmitt input*5
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*6 TEX pin*7
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*3
	V_{ILS}	0	0.2V_{DD}	V	CMOS schmitt input*4
	V_{ILTS}	0	0.8	V	TTL schmitt input*5
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*6 TEX pin*7
Operating temperature	Topr	–20	+75	°C	

*1 AV_{DD} and V_{DD} should be set to the same voltage.

*2 $AMPV_{DD}$ and V_{DD} should be set to the same voltage.

*3 Normal input port (each pin of PC, PD2, PD3, PD6, PF0 to PF3, PI1 to PI7 and PH0 to PH3), MP pin

*4 Each pin of $\overline{RST}$, PD0/$\overline{INT1}$/$\overline{NMI}$, PD1/RMC, PD4/$\overline{CS0}$, PD5/$\overline{SCK0}$, PD7/SI0, PE0/$\overline{SCK1}$, PE2/SI1, PE3/SYNC, PE4/EXI0, PE5/EXI1, PI0/$\overline{INT0}$, PG3/$\overline{EC}$/$\overline{INT2}$ (For PE3/SYNC, when CMOS schmitt input is selected with mask option.)

*5 PE3/SYNC (when TTL schmitt input is selected with mask option.)

*6 Specifies only during external clock input.

*7 Specifies only during external event input.

*8 Vpp and V_{DD} should be set to the same voltage.

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V) (Ta = –10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE0 to PE1, PE6 to PE7, PF4 to PF7, PH (V_{OL} only) PI	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PH	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*1		–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PF, PG3, PI, MP, $\overline{AN0}$ to AN3, $\overline{RST}$*1	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain output leakage current (N-CH Tr off state)	I_{LOH}	PH4 to PH7	V_{DD} = 5.5V, V_{OH} = 12V			50	µA
		PH0 to PH3	V_{DD} = 5.5V, V_{OH} = 5.5V			10	µA
Supply current*2	I_{DD1}	V_{DD}, V_{SS}	16MHz crystal oscillation (C_1 = C_2 = 15pF) V_{DD} = 5.5V*3		37	50	mA
	I_{DDS1}		Sleep mode V_{DD} = 5.5V		2.1	8	mA
	I_{DD2}		32kHz crystal oscillation (C_1 = C_2 = 47pF) V_{DD} = 3.3V		58	1000	µA
	I_{DDS2}		Sleep mode V_{DD} = 3V ± 0.3V		9	35	µA
	I_{DDS3}		Stop mode (EXTAL and TEX pins oscillation stop) V_{DD} = 5V ± 0.5V			30	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C_{IN}	PC, PD, PE0, PE2 to PE5, PF, PG, PI, CTLHEAD (+), CTLHEAD (–), CTLFAMPI (+), CTLFAMPI (–), CTLSAMPI, RFG, XTAL, TEX	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 $\overline{RST}$ pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when no resistor is selected.

*2 When entire output pins are left open.

*3 When setting upper 2 bits (CPU clock selection) of clock control register (CLC: 00FEh) to "00" and operating in high speed mode (1/2 frequency dividing clock).

AC Characteristics

(1) Clock timing

(Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL}, t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise and fall times	t_{CR}, t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count clock input pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	t_{sys} + 200*1			ns
Event count clock input rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count clock input rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

*1 t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).
t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

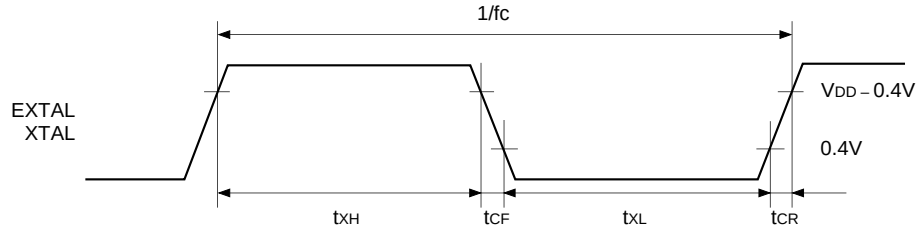


Fig. 1. Clock timing

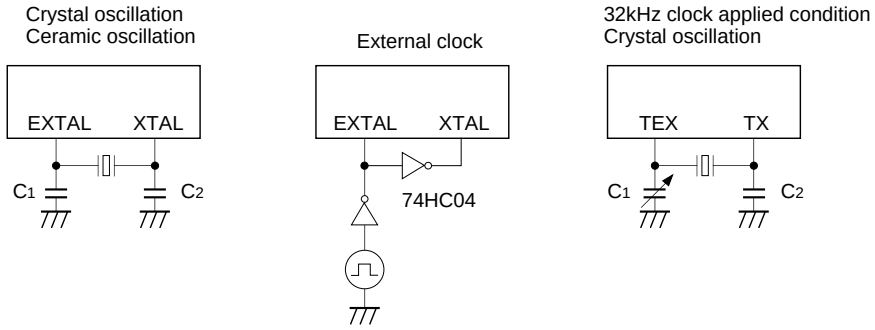


Fig. 2. Clock applied condition

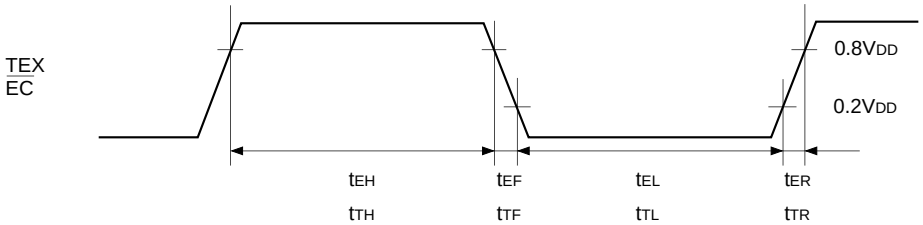


Fig. 3. Event count clock timing

(2) Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow$ SO0 floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 100		ns
SI0 input setup time (against $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	–tsys + 100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (against $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	2tsys + 100		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		2tsys + 100	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF + 1TTL.

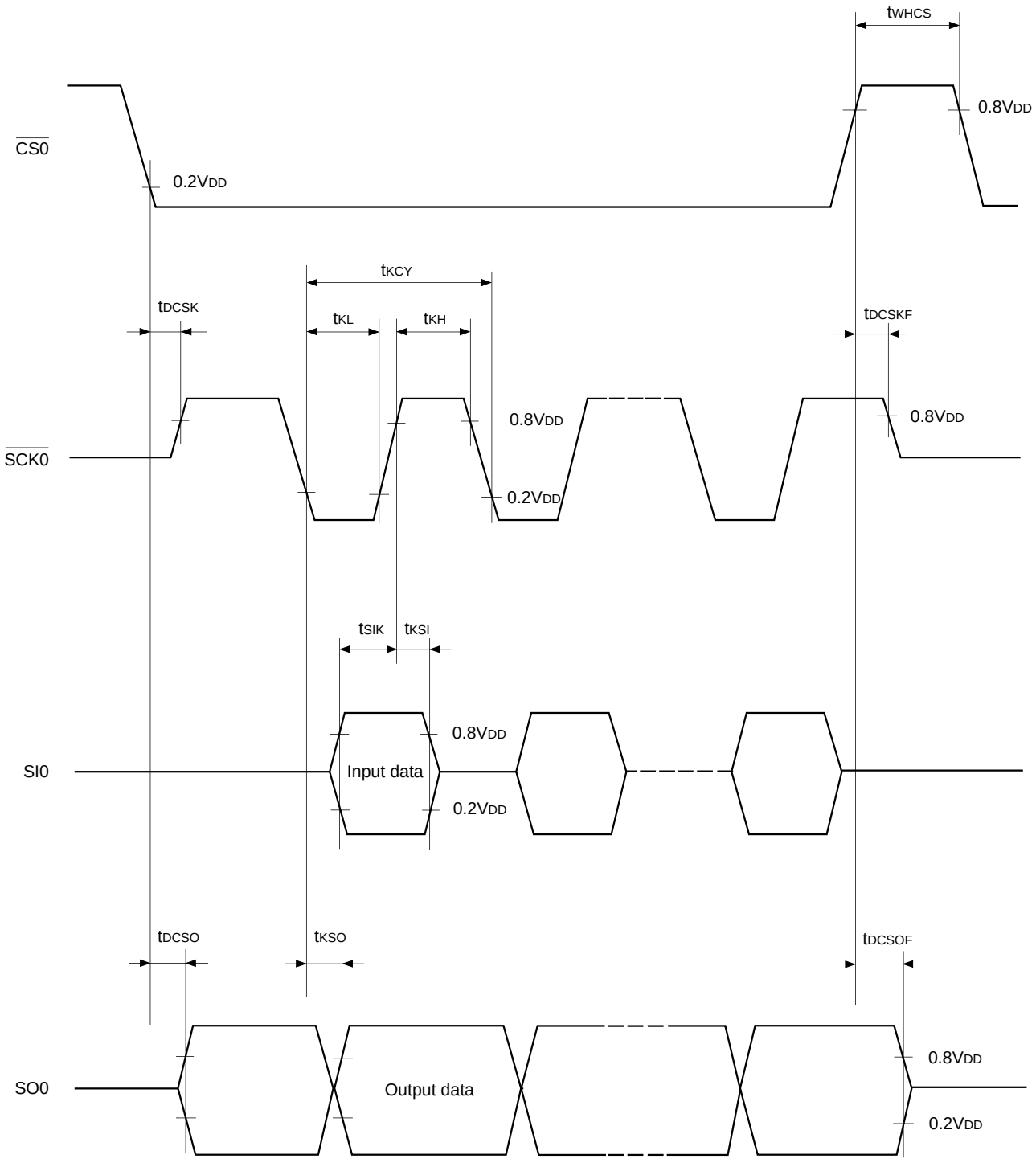


Fig. 4. Serial transfer timing (CH0)

Serial transfer (CH1) (SIO mode) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	tsys +100		ns
			Output mode	8000/fc – 50		ns
SI1 input setup time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	tsys + 200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		tsys + 200	ns
			$\overline{SCK1}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

Note 2) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF + 1TTL.

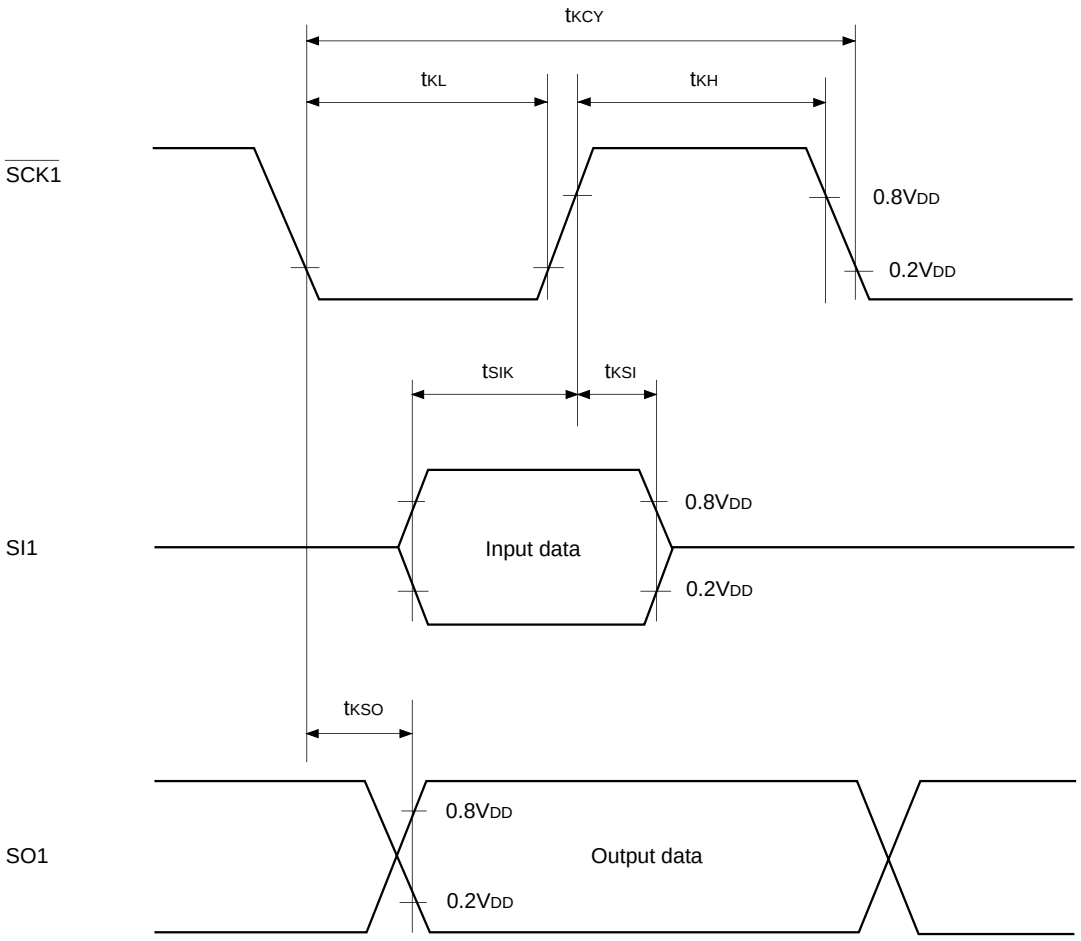


Fig. 5. Serial transfer CH1 timing (SIO mode)

Serial transfer (CH1) (Special mode) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	*1		104		µs
SI1 data setup time	t_{LSU}	SI1		2			µs
SI1 data hold time	t_{LHD}	SI1		2			µs

*1 t_{LCY} is specified only when serial mode register (CH1) (SIOM1: 05F2h) lower 2 bits (SO1 clock selection) are set at 104µs.

Note) The load of SO1 pin is 50pF + 1TTL.

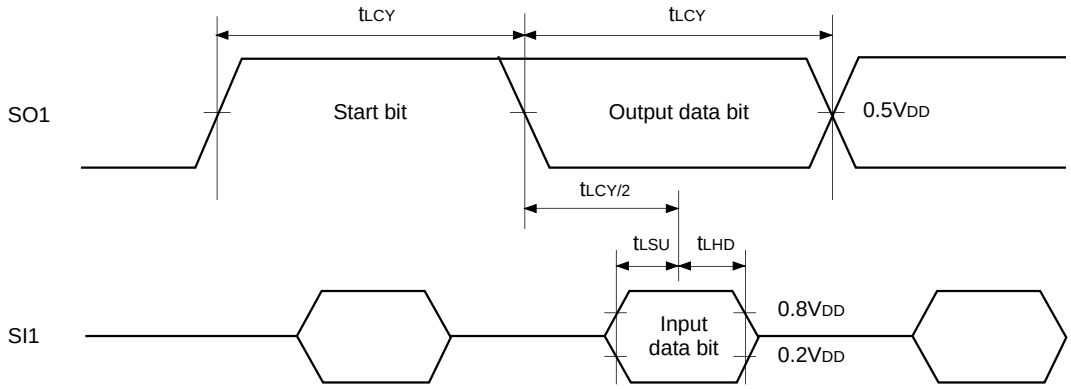


Fig. 6. Serial transfer CH1 timing (Special mode)

Serial transfer (CH2) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCL clock frequency	f_{SLC}	SCL			400	kHz
Bus-free time before starting transfer	t_{BUF}	SDA, SCL		2.6		µs
Hold time for starting transfer	$t_{HD;\,STA}$	SDA, SCL		1.0		µs
Clock low level width	t_{LOW}	SCL		1.0		µs
Clock high level width	t_{HIGH}	SCL		1.0		µs
Setup time for repetitive transfers	$t_{SU;\,STA}$	SDA, SCL		1.0		µs
Data hold time	$t_{HD;\,DAT}$	SDA, SCL		0*1		µs
Data setup time	$t_{SU;\,DAT}$	SDA, SCL		100		ns
SDA, SCL rise time	t_R	SDA, SCL			300	ns
SDA, SCL fall time	t_F	SDA, SCL			300	ns
Setup time for transfer completion	$t_{SU;\,STO}$	SDA, SCL		1.6		µs

*1 The SCL fall time (300ns Max.) is not included in the data hold time.

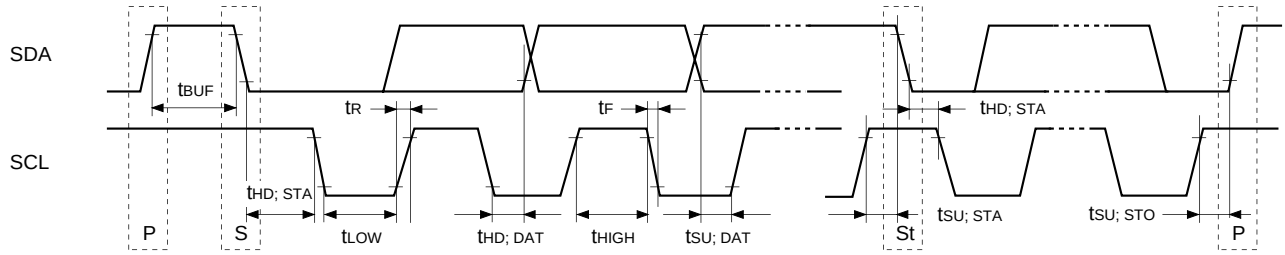


Fig. 7. Serial transfer CH2 timing

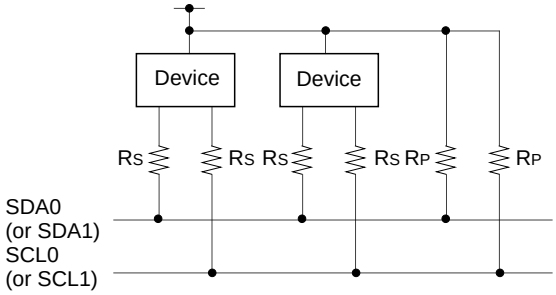


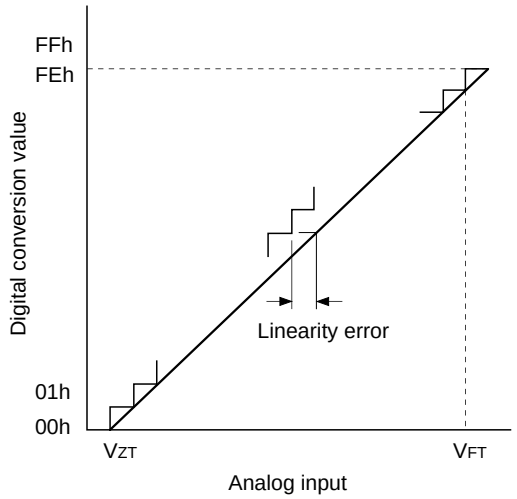
Fig. 8. Device recommended circuit

- A pull-up resistor (R_P) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce the spike noise caused by CRT flashover.

(4) A/D converter characteristics

(Ta = –10 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}*1			µs
Sampling time	t_{SAMP}			12/f_{ADC}*1			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD} – 0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
			Sleep mode Stop mode 32kHz operating mode			10	µA



*1 f_{ADC} indicates the follwing values due to the peripheral clock control register (PCC: 05F8h) bit 3 and clock control register (CLC: 00FEh) upper 2 bits.

ADCCK / PCK1, PCK0	0 (ϕ/2 selection)	1 (ϕ selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = fc/2	f_{ADC} = fc
01 (ϕ = f_{EX}/4)	f_{ADC} = fc/4	f_{ADC} = fc/2
11 (ϕ = f_{EX}/16)	f_{ADC} = fc/16	f_{ADC} = fc/8

Fig. 9. Definitions of A/D converter terms

(4) Interruption, reset input (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{NMI}$ PI0 to PI7		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

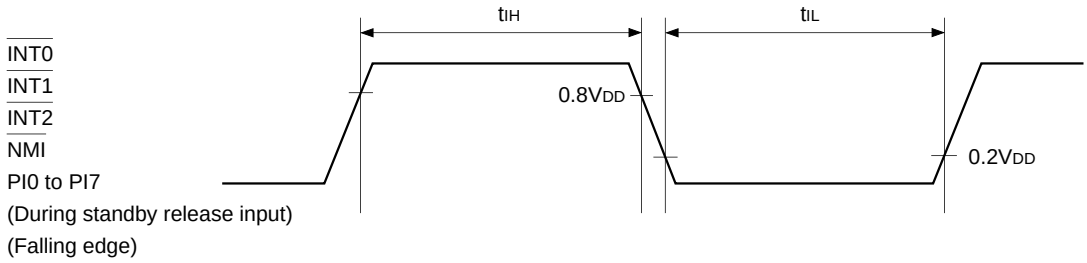


Fig. 10. Interruption input timing

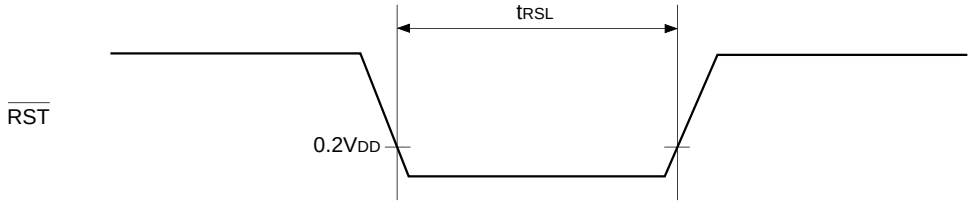


Fig. 11. Reset input timing

(5) Others (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
CFG input high and low level widths	t_{CFH} t_{CFL}	CFG		$24t_{FRC}$ + 200		ns
DFG input high and low level widths	t_{DFH} t_{DFL}	DFG		$16t_{FRC}$ + 200		ns
DPG minimum pulse width	t_{DPW}	DPG		$8t_{FRC}$ + 200		ns
DPG minimum removal time	trem	DPG		$16t_{FRC}$ + 200		ns
EXI input high and low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	tsys = 2000/fc	$8t_{FRC}$ + 200 + tsys		ns

Note 1) t_{FRC} = 1000/fc [ns]

Note 2) tsys indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

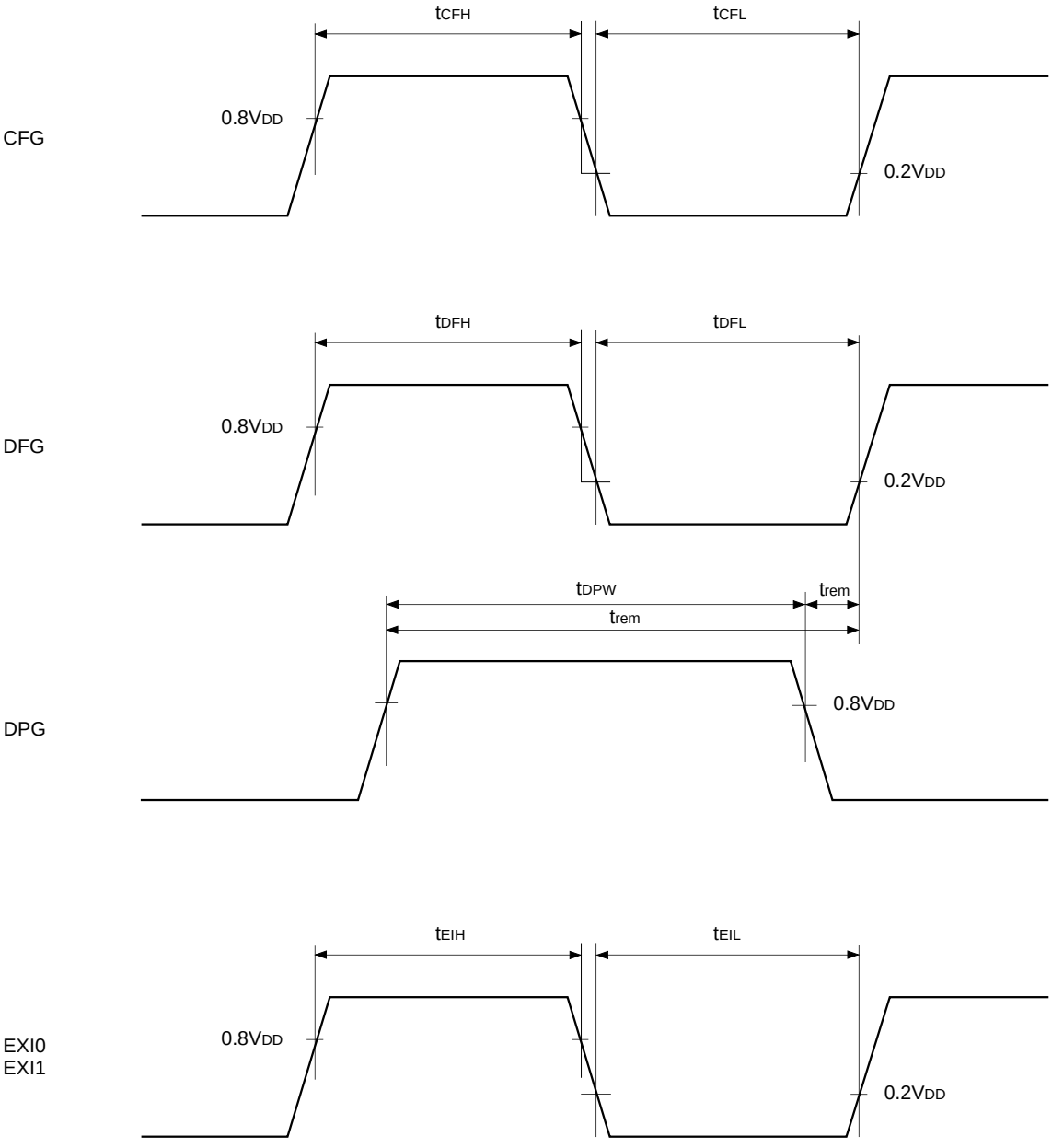


Fig. 12. Other timings

Analog Circuit Characteristics

(1) Amplifier circuit reference voltage characteristics ($AMPV_{DD}$ = V_{DD} = 5.0V, $AMPV_{SS}$ = Vss = 0V, Ta = –10 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Reference level output voltage	V_{OR}	CTLAGND		2.20	2.45	2.75	V

(2) CTL 1st amplifier characteristics ($AMPV_{DD}$ = V_{DD} = 5.0V, $AMPV_{SS}$ = Vss = 0V, Ta = –10 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain*1	A_{VCTL1}	CTLFAMPI (–) CTLFAMPI (+)	CTLFAMPI (–) = 0V, Gain = 16dB	13.5	15.5	17.5	dB
			CTLFAMPI (–) = 0V, Gain = 34dB	31.8	33.8	35.8	
			CTLFAMPI (–) = 0V, Gain = 49dB	46.5	48.5	50.5	
			CTLFAMPI (–) = 0V, Gain = 55dB	52.5	54.5	56.5	
Output offset voltage	V_{OSCTL1}	CTLFAMPI (–) CTLFAMPI (+)	CTLFAMPI (–), CTLFAMPI (+) = open, Gain = 16dB	–25	0	+25	mV

*1 The result after monitoring CTLFAMPO pin when the electrolytic capacitor (10µF) is connected to CTLFAMP (–) and CTLFAMP (+).

(3) CTL 2nd amplifier characteristics ($AMPV_{DD}$ = V_{DD} = 5.0V, $AMPV_{SS}$ = Vss = 0V, Ta = –10 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain*1	A_{VCTL2}	CTLSAMPI	Gain = 5dB	3.5	5.5	7.5	dB
			Gain = 8dB	6.2	8.2	10.2	
			Gain = 11dB	9.0	11.0	13.0	
			Gain = 14dB	12.0	14.0	16.0	
			Gain = 17dB	15.0	17.0	19.0	
			Gain = 20dB	18.0	20.0	22.0	
Output offset voltage	V_{OSCTL2}	CTLSAMPI	CTLSAMPI = open, Gain = 5dB	–30	0	+30	mV
LPF cut-off frequency	F_{CCTL}	CTLSAMPI	12kHz, f_{DC} – 3dB	8	12	24	kHz
			20kHz, f_{DC} – 3dB	12	20	42	

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Comparator level*2	V_{CCTL}	CTLSAMPI	Comparator level = +100mV$_{0\text{-}p}$	80	110	140	mV
			Comparator level = +150mV$_{0\text{-}p}$	110	150	190	
			Comparator level = +200mV$_{0\text{-}p}$	160	200	240	
			Comparator level = +250mV$_{0\text{-}p}$	210	250	290	
			Comparator level = +300mV$_{0\text{-}p}$	250	290	330	
			Comparator level = +400mV$_{0\text{-}p}$	340	380	420	
			Comparator level = +500mV$_{0\text{-}p}$	420	470	520	
			Comparator level = +600mV$_{0\text{-}p}$	530	570	610	
			Comparator level = +1000mV$_{0\text{-}p}$	850	920	990	
			Comparator level = –100mV$_{0\text{-}p}$	–90	–120	–150	
			Comparator level = –150mV$_{0\text{-}p}$	–110	–130	–190	
			Comparator level = –200mV$_{0\text{-}p}$	–150	–190	–230	
			Comparator level = –250mV$_{0\text{-}p}$	–200	–240	–280	
			Comparator level = –300mV$_{0\text{-}p}$	–240	–280	–320	
			Comparator level = –400mV$_{0\text{-}p}$	–340	–380	–420	
			Comparator level = –500mV$_{0\text{-}p}$	–430	–480	–530	
			Comparator level = –600mV$_{0\text{-}p}$	–540	–580	–620	
			Comparator level = –1000mV$_{0\text{-}p}$	–870	–970	–1070	

*1 The result after monitoring ANOUT pin when the electrolytic capacitor (10µF) is connected to CTLSAMPI.

*2 The reference value of the comparator level is CTLAGND.

(4) CTL amplifier characteristics (CTL1stAMP + CTL2ndAMP)

($AMPV_{DD}$ = V_{DD} = 5.0V, $AMPV_{SS}$ = Vss = 0V, Ta = –10 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain*3	A_{VCTL}	CTLHEAD (–) CTLHEAD (+)	CTLHEAD (–) = 0V, Gain = (16dB + 5dB)	17.0	20.5	23.5	dB
			CTLHEAD (–) = 0V, Gain = (55dB + 20dB)	70.5	74.5	77.0	
Input sensitivity	V_{SCTL}	CTLHEAD (–) CTLHEAD (+)	CTLHEAD (–) = 0V, Gain = (55dB + 20dB) Comparator = ±150mV$_{0\text{-}p}$	60	70	140	µVp-p

*3 The result when waveform is input from CTLHEAD (+) pin and ANOUT pin is monitored after performing coupling electrolytic capacitor (10µF) of CTLHEAD (–) and CTLHEAD (+), and coupling electrolytic capacitor (10µF) of HEADL (–) and HEADL (+), CTLFAMPI (–) and CTLFAMPI (+) , and CTLFAMPO and CTLSAMPI. Gain is maximum –1.5dB lowered when waveform is input from CTLHEAD (+) pin.

(5) RECCTL write circuit characteristics ($AMPV_{DD}$ = V_{DD} = 5.0V, $AMPV_{SS}$ = Vss = 0V, Ta = –10 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Write current*1	I_{OREC}	CTLHEAD (–) CTLHEAD (+)	Write current 2.0mAp-p	0.8	1.8	3.6	mA
			Write current 3.0mAp-p	1.4	2.8	5.0	
			Write current 4.0mAp-p	2.0	3.8	7.0	
			Write current 5.0mAp-p	2.4	4.8	8.5	
			Write current 6.0mAp-p	3.0	6.0	10.0	
			Write current 7.0mAp-p	3.5	6.8	11.5	
			Write current 8.0mAp-p	4.5	7.8	13.0	
			Write current 9.0mAp-p	5.0	8.8	15.0	
			Write current 10.0mAp-p	5.5	7.7	17.0	

*1 The current which flows when CTLHEAD (–) and CTLHEAD (+) shorts.

(6) Auto threshold control circuit (ATC) characteristics

($AMPV_{DD}$ = V_{DD} = 5.0V, $AMPV_{SS}$ = Vss = 0V, Ta = –10 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
ATC peak hold circuit initialize voltage value*2	$V_{ATCINIT}$		Voltage = –150mV_{0-P}	–110	–150	–190	mV
			Voltage = –400mV_{0-P}	–350	–400	–450	
ATC comparator level offset voltage*3	V_{ATCOFF}		Gain = 1/6 (16.7%)		–70	–160	mV
			Gain = 1/5 (20%)		–90	–210	
			Gain = 1/4 (25%)		–90	–210	
			Gain = 1/3 (33.3%)		–70	–160	
			Gain = 2/5 (40%)		–90	–210	
			Gain = 1/2 (50%)		–70	–160	
			Gain = 3/5 (60%)		–90	–210	

*2 Reference is CTLAGND.

*3 Reference is CTLAGND.
When comparator level is generated using ATC, actual comparator level is as follows by the offset voltage inside the ATC.

Vin × gain + |offset voltage|

Example: Gain = 1/2

Vin × 1/2 + 160

(7) Schmitt characteristics ($AMPV_{DD}$ = V_{DD} = 5.0V, $AMPV_{SS}$ = Vss = 0V, Ta = –10 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
RTG schmitt width	S_{RFG}	RFG0, RFG1	Schmitt width 1Vp-p	820	920	1020	mV
CFG/DFG/DPG	S_{CFG} S_{DFG} S_{DPG}	CFG, DFG, DPG	Schmitt width 410mVp-p	180	300	420	mV
			Schmitt width 1Vp-p	700	900	1100	

Appendix

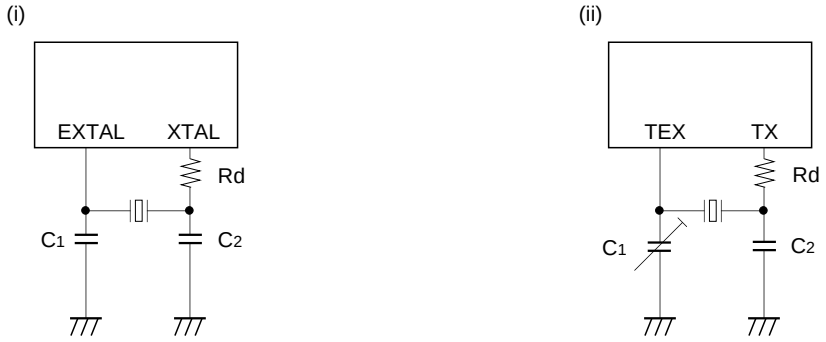


Fig. 13. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12	0	
		16.00	12	12	0	
	P3	32.768kHz	30	18	470k	(ii)

Mask option table

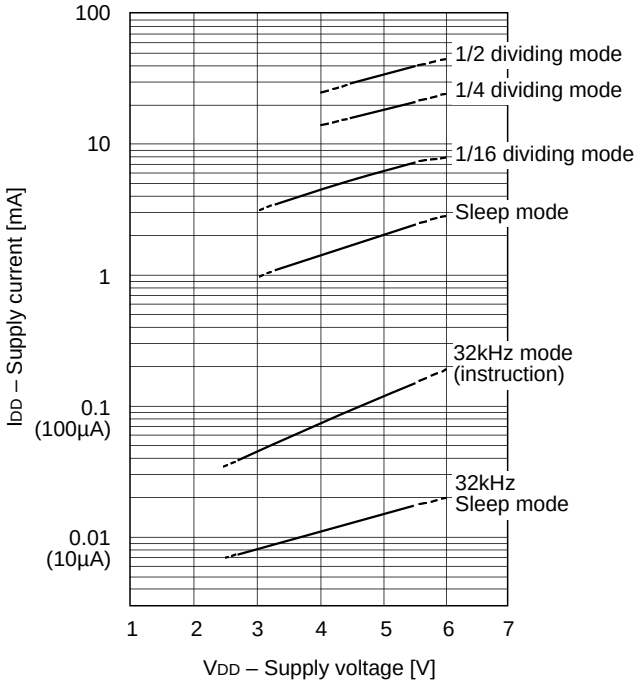
Item	Mask ROM	CXP884P60Q-1-□□□*2
Package	100-pin plastic QFP	100-pin plastic QFP
ROM capacity	40K/48K (CXP88340/88348) 52K/60K (CXP88452/88460)	PROM 60K bytes
Reset pin pull-up resistor	Existent/Non-existent	Existent
Input circuit format*1	CMOS schmitt/TTL schmitt	TTL schmitt

*1 The input circuit format can be selected for PE3/SYNC pin.

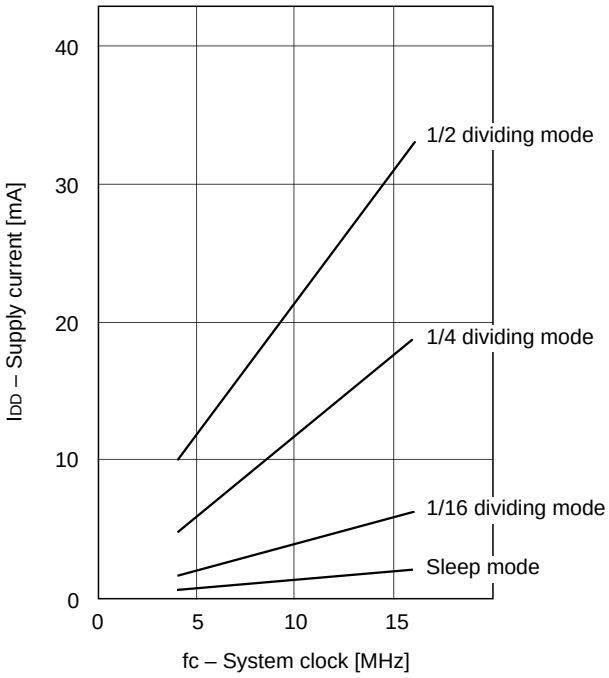
*2 OEM No.

Characteristics Curve

IDD vs. VDD
(fc = 16MHz, Ta = 25°C)

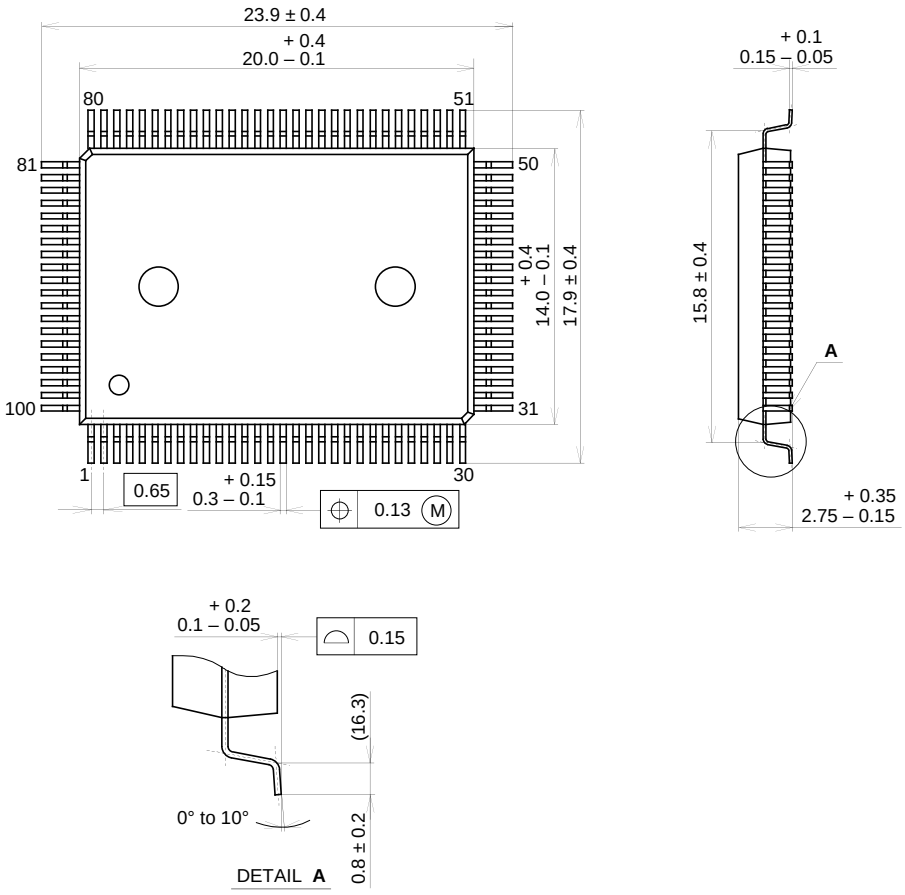


IDD vs. fc
(VDD = 5V, Ta = 25°C)



Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

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