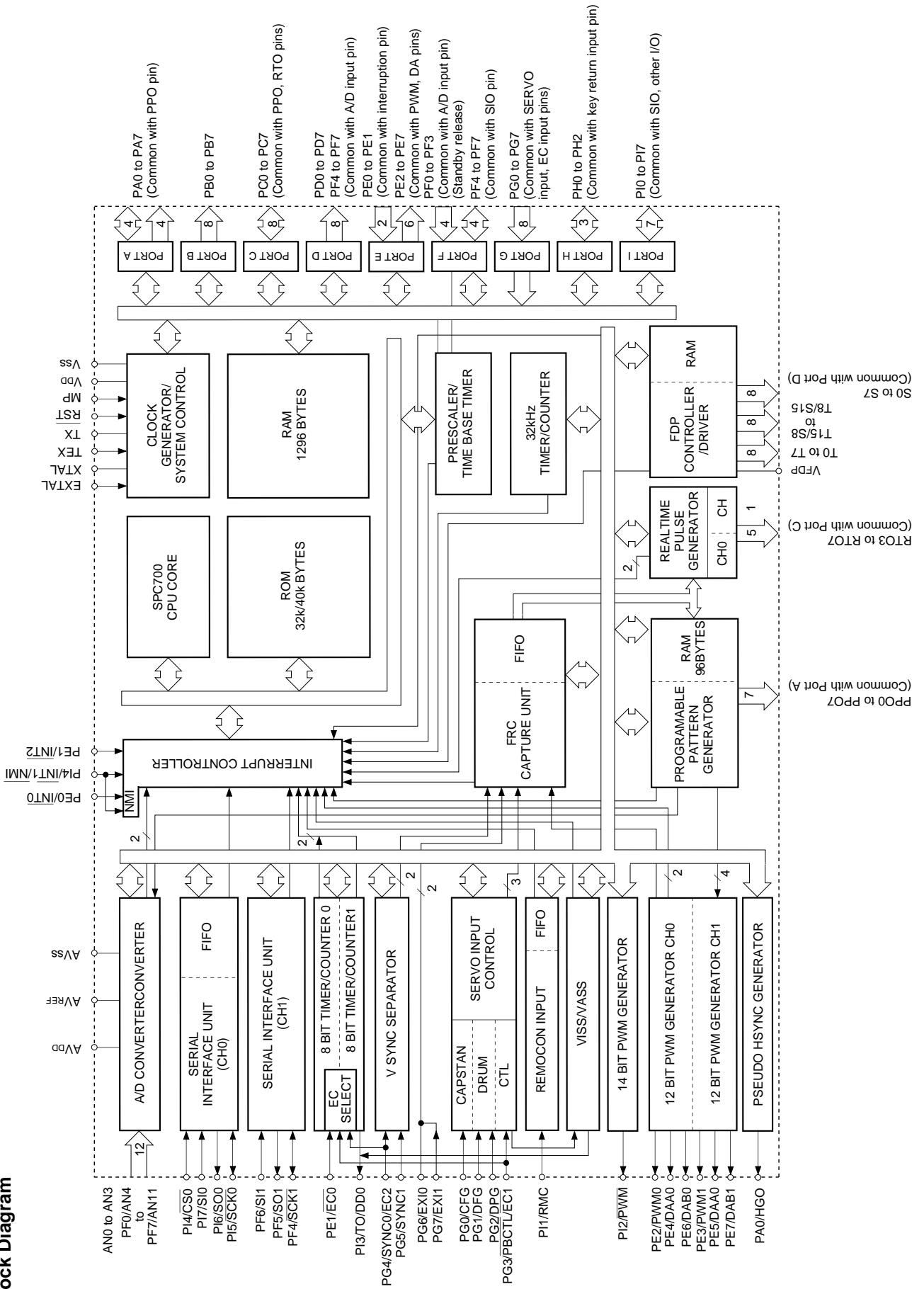
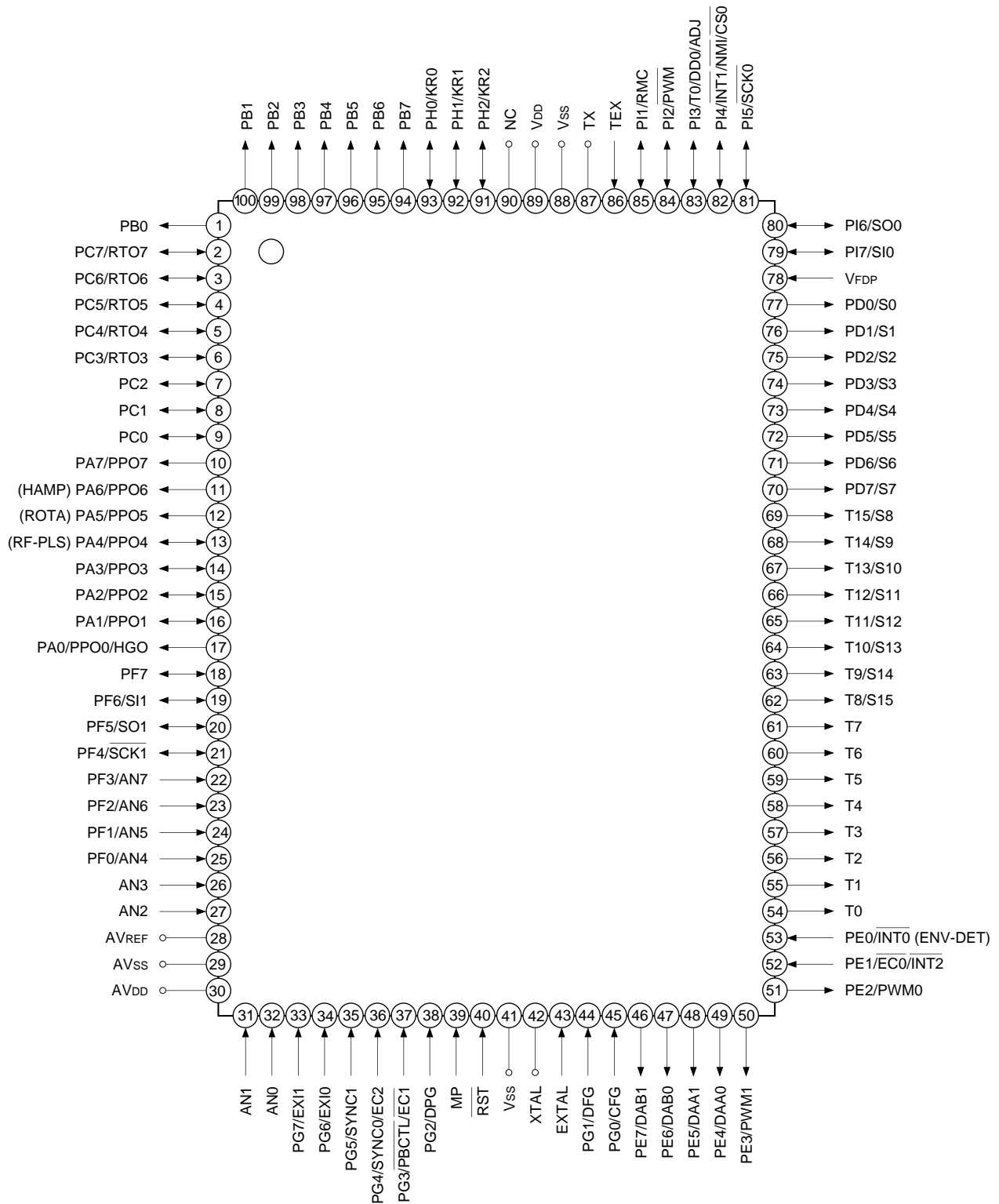




Block Diagram



Pin Configuration (Top View)



- Note)** 1. NC (Pin 90) is always connected to V<sub>DD</sub>.  
 2. V<sub>SS</sub> (Pins 41 and 88) are both connected to GND.

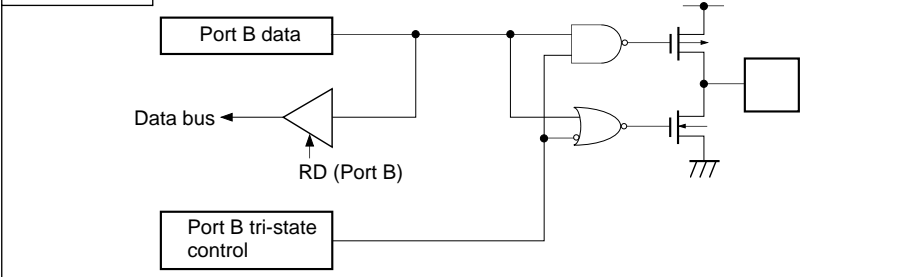
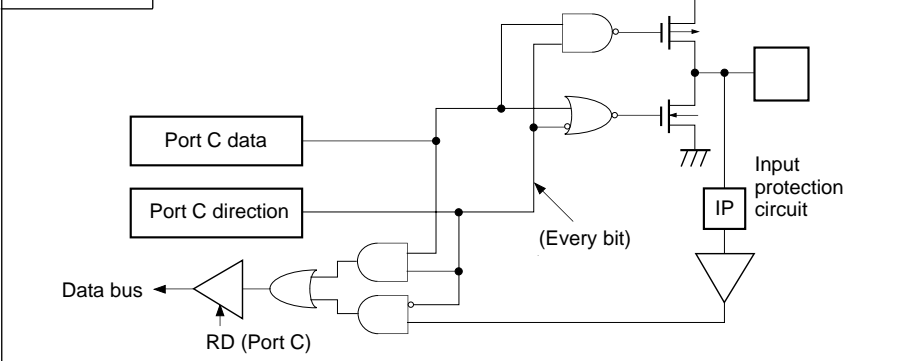
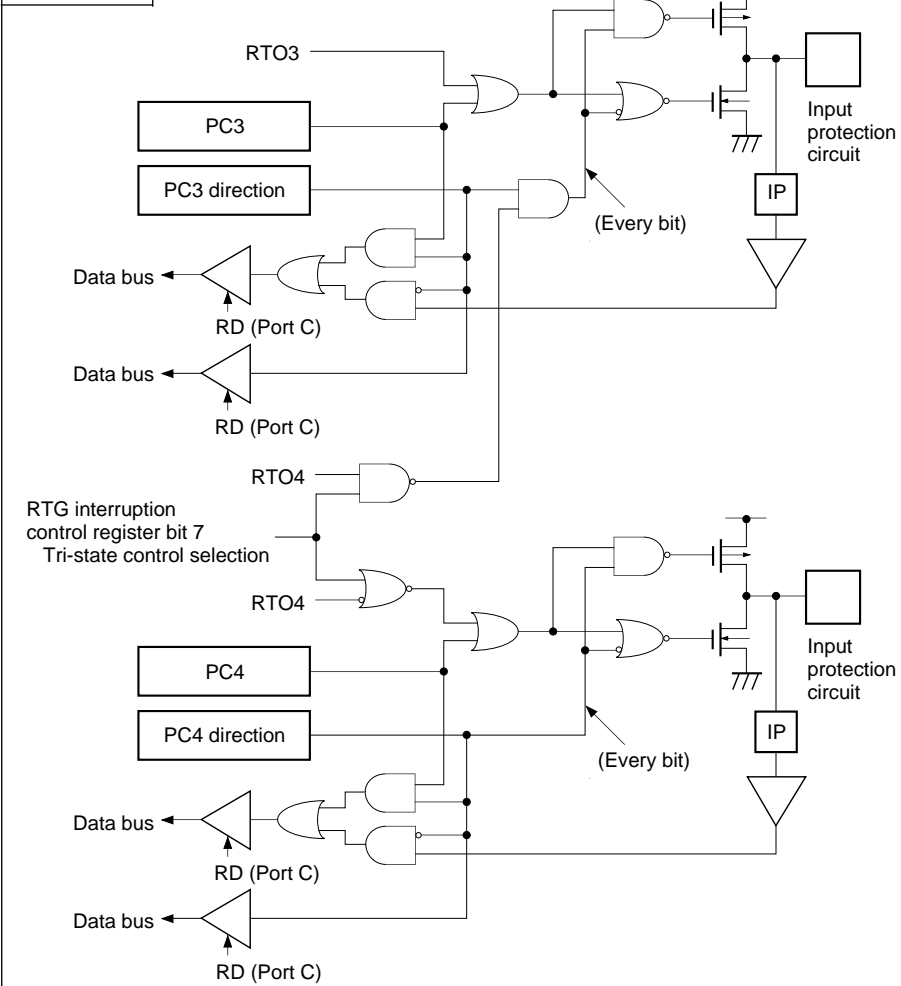
Pin Description

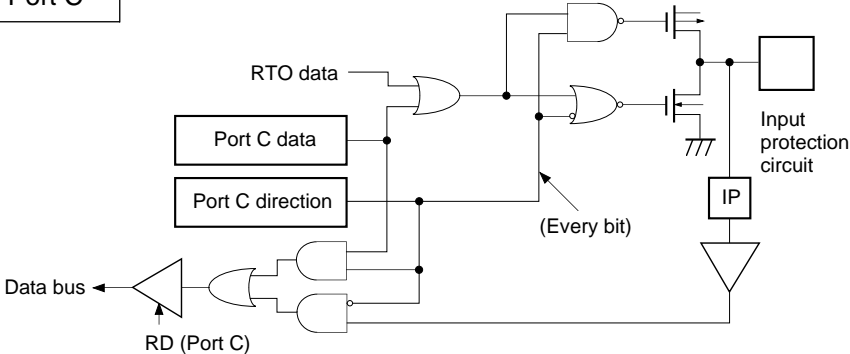
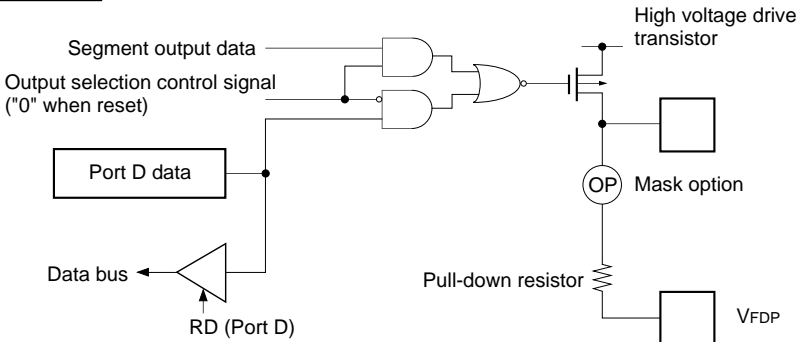
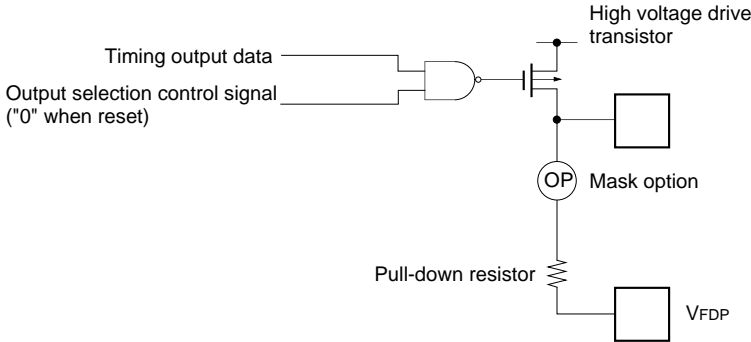
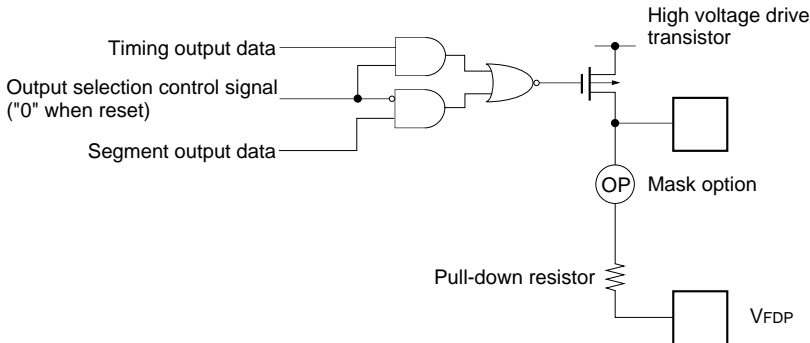
Symbol	I/O	Description		
PA0/PPO0/ HGO	Output/Real time output/output	(Port A) 8-bit I/O port. Enable to specify I/O by bit unit. Data is gated with RTO content by OR-gate and they are output. (8 pins)	Pseudo HSYNC output pin.	
PA1/PPO1	I/O/ Real time output		Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. (5 pins)	
PA2/PPO2				
PA3/PPO3				
PA4/PPO4	Output/ Real time output			Head switching output pins.
PA5/PPO5				
PA6/PPO6				
PA7/PPO7				
PB0 to PB7	Output	8-bit output port. Tri-state can be controlled. (8 pins)		
PC0/PPO8 to PC7/PPO15	Output/ Real time output	(Port C) 8-bit I/O port. Enable to specify I/O by bit unit. Data is gated with RTO content by OR-gate and they are output. (8 pins)	Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. (5 pins)	
T0 to T7	Output	FDP timing signal output pin.		
T8/S15 to T15/S8	Output/Output	Output pins for FDP timing signal and segment signal.		
PD0 to PD7	Output	(Port D) 8-bit output port. (8 pins)	FDP segment signal output pin.	
PE0/ $\overline{\text{INT0}}$	Input/Input	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Trigger pulse input pin for head switching output.	Input pin to request external interruption. Active when falling edge.
$\overline{\text{PE1/EC0/INT2}}$	Input/Input/Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output/Output		PWM output pins. (2 pins)	
PE3/PWM1	Output/Output			
PE4/DAA0	Output/Output			
PE5/DAA1	Output/Output			
PE6/DAB0	Output/Output			
PE7/DAB1	Output/Output		DA gate pulse output pins. (2 pins)	
AN0 to AN3	Input	Analog input pins to A/D converter. (8 pins)		
PF0/AN0 to PF3/AN3	Input/Input	(Port F) 8-bit I/O port. Enable to specify I/O by bit unit. (8 pins)		
PF4/SCK1	I/O/I/O			Serial clock (CH1) I/O pin.
PF5/SO1	I/O/Output			Serial data (CH1) output pin.
PF6/SI1	I/O/Input			Serial data (CH1) input pin.
PF7	I/O			

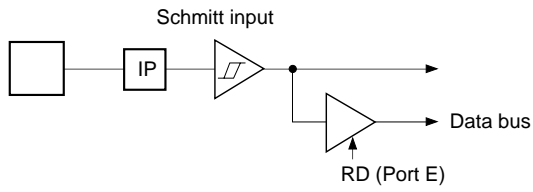
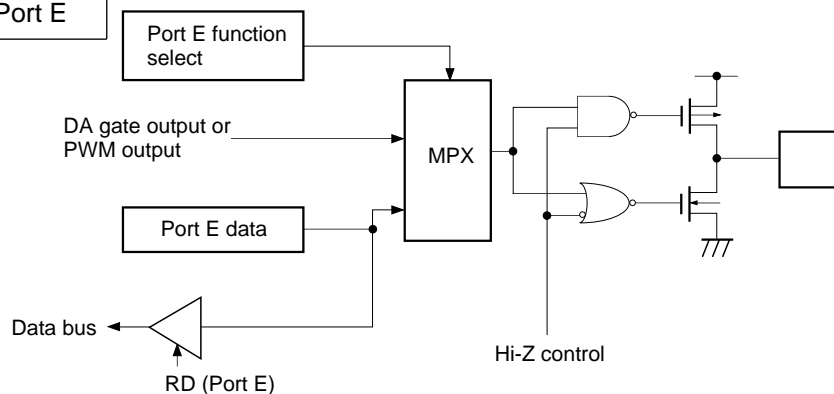
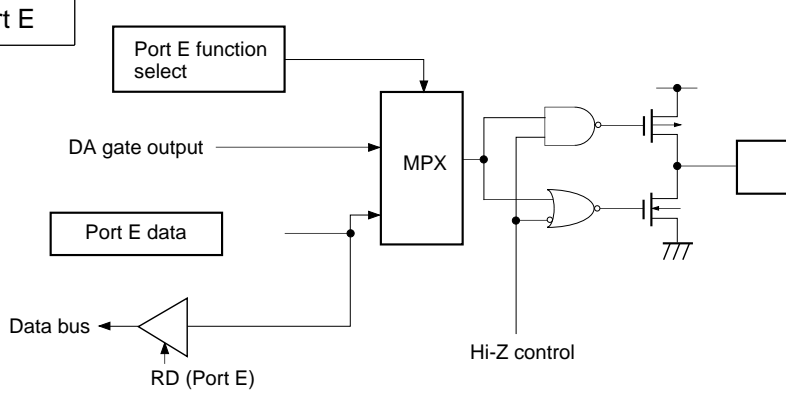
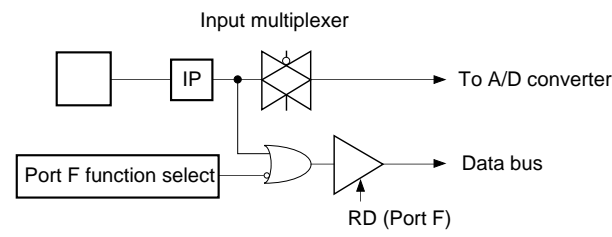
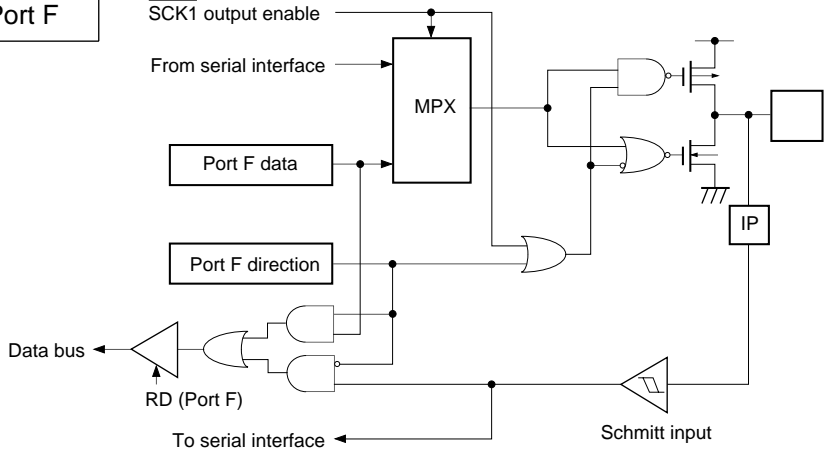
Symbol	I/O	Description		
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.	
PG1/DFG	Input/Input		Drum FG input pin.	
PG2/DPG	Input/Input		Drum PG input pin.	
PG3/ PBCTL/EC1	Input/Input/Input		Playback CTL input pin.	External event input pin for timer/counter.
PG4/ SYNC0/EC2	Input/Input/Input		Composite sync signal input pin.	External event input pin for timer/counter.
PG5/SYNC1	Input/Input			
PG6/EXI0	Input/Input			
PG7/EXI1	Input/Input		External input pin for FRC capture unit.	
PH0/KR0 to PH7/KR2	I/O/Input	(Port H) 3-bit I/O port. (3 pins)	Key return input signal for key scanning at FDP segment signal.	
PI1/RMC	I/O/Input	(Port I) 8-bit I/O port. Enable to specify I/O by bit unit. (8 pins)	Remote control receiving circuit input pin.	
PI2/PWM	I/O/Input		14-bit PWM output pin.	
PI3/TO/ DDO/ADJ	I/O/Input		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output pin.	
PI4/INT1/ NMI/CS0	I/O/Input/ Input/Input		Input pin to request external interruption, non-maskable interruption and for serial chip select (CH0). Active when falling edge.	
PI5/SCK0	I/O/Input		Serial clock (CH1) I/O pin.	
PI6/SO0	I/O/Output		Serial data (CH1) output pin.	
PI7/SI0	I/O/Input		Serial data (CH1) input pin.	
EXTAL	Input		Connecting pin of crystal oscillator for system clock.	
XTAL	Output	When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock.		
TX	Output	When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)		
RST	Input	System reset pin of active "L" level.		
MP	Input	Microprocessor mode input pin. Always connect to GND.		
V <sub>FDP</sub>		FPD voltage supply pin when specifying internal resistor by mask option.		
AV <sub>DD</sub>		Positive power supply pin of A/D converter.		
AV <sub>REF</sub>	Input	Reference voltage input pin of A/D converter.		
AV <sub>SS</sub>		GND pin of A/D converter.		
V <sub>DD</sub>		Positive power supply pin.		
V <sub>SS</sub>		GND pin. Connect both V <sub>SS</sub> pins to GND.		

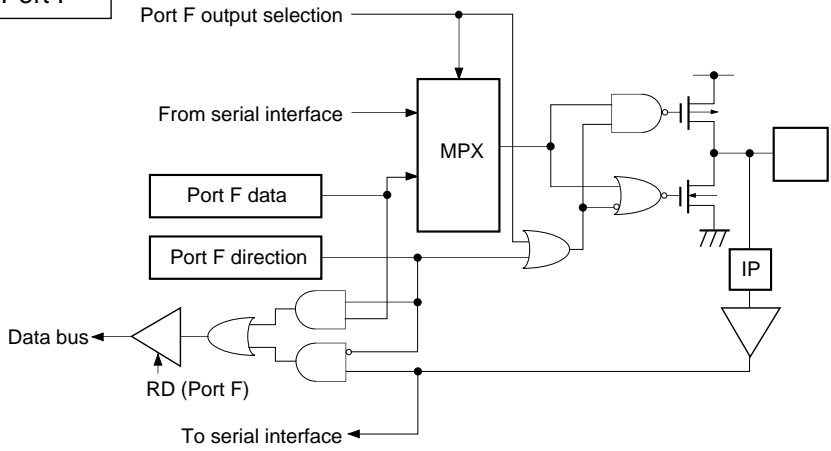
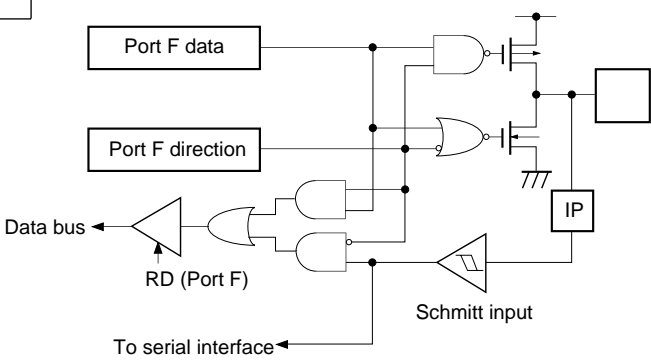
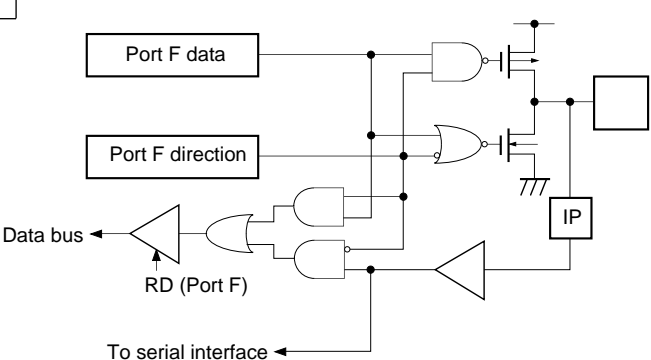
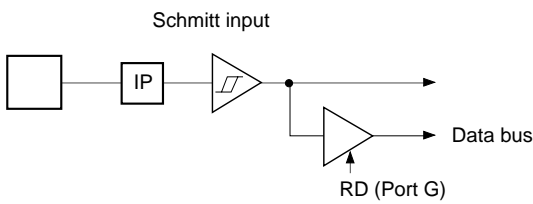
Input/Output Circuit Formats for Pins

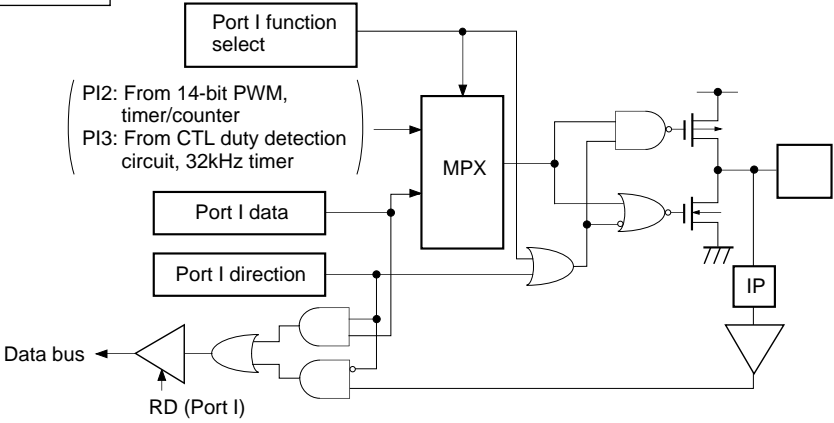
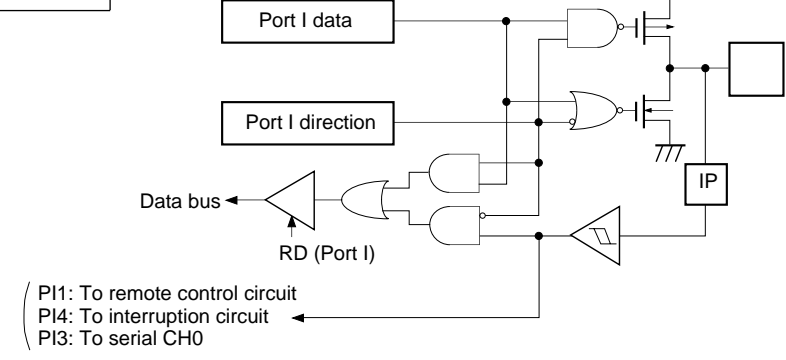
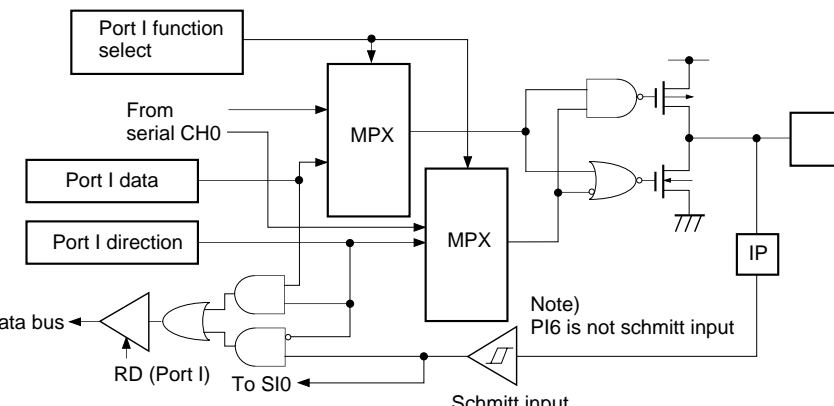
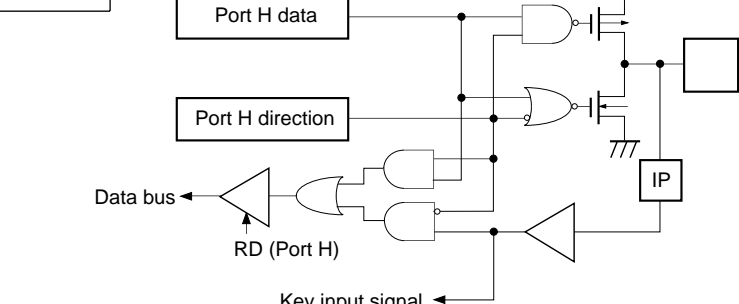
Pin	Circuit format	When reset
<p>PA0/PPO0/ HGO</p> <p>1 pin</p>	<p>Port A</p> <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>PA1/PPO1</p> <p>1 pin</p>	<p>Port A</p> <p>PPG control status register bit 0 Tri-state control selection</p> <p>Input protection circuit</p> <p>(Every bit)</p>	<p>Hi-Z</p>
<p>PA2/PPO2 to PA4/PPO4</p> <p>3 pins</p>	<p>Port A</p> <p>Input protection circuit</p> <p>(Every bit)</p>	<p>Hi-Z</p>
<p>PA5/PPO5 to PA7/PPO7</p> <p>3 pins</p>	<p>Port A</p> <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>

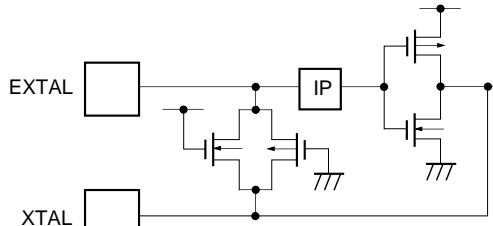
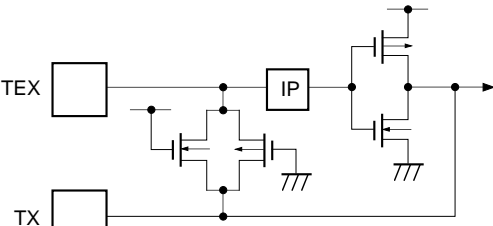
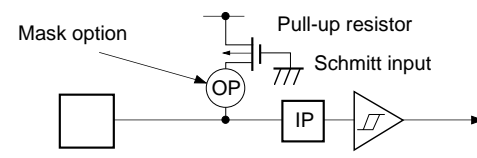
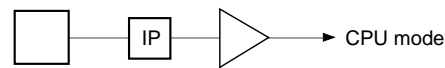
Pin	Circuit format	When reset
PB0 to PB7  8 pins	<p>Port B</p> 	Hi-Z
PC0 to PC2  3 pins	<p>Port C</p> 	Hi-Z
PC3/RTO3  1 pin  PC4/RTO4  1 pin	<p>Port C</p> 	Hi-Z

Pin	Circuit format	When reset
<p>PC5/RT05 to PC7/RT07</p> <p>3 pins</p>	<p>Port C</p> 	<p>Hi-Z</p>
<p>PD0/S0 to PD7/S7</p> <p>8 pins</p>	<p>Port D</p> 	<p>Hi-Z</p>
<p>T0 to T7</p> <p>8 pins</p>		<p>Hi-Z</p>
<p>T8/S15 to T15/S8</p> <p>8 pins</p>		<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE0/<math>\overline{\text{INT0}}</math> PE1/<math>\overline{\text{EC0/INT2}}</math></p> <p>2 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1</p> <p>4 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE6/DAB0 PE7/DAB1</p> <p>2 pins</p>	<p>Port E</p> 	<p>High level</p>
<p>PF0/AN4 to PF3/AN7</p> <p>4 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PF4/<math>\overline{\text{SCK1}}</math></p> <p>1 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PF5/SO1</p> <p>1 pin</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PF6/SI1</p> <p>1 pin</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PF7</p> <p>1 pin</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL/ EC1 PG4/SYNC0/ EC2 PG5/SYNC1 PG6/EXI0 PG7/EXI1</p> <p>8 pins</p>	<p>Port G</p>  <p>Note) For PG4/SYNC and PG5/SYNC1, CMOS schmitt input or TTL schmitt input can be selected with the mask option.</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PI2/<math>\overline{\text{PWM}}</math> PI3/<math>\overline{\text{TO}}</math>/ DDO/<math>\overline{\text{ADJ}}</math></p> <p>2 pins</p>	<p>Port I</p>  <p>Port I function select</p> <p>( PI2: From 14-bit PWM, timer/counter PI3: From CTL duty detection circuit, 32kHz timer )</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>IP</p>	<p>Hi-Z</p>
<p>PI1/RMC PI4/<math>\overline{\text{INT1}}</math>/ <math>\overline{\text{NMI}}</math>/<math>\overline{\text{CS0}}</math> PI7/SI0</p> <p>1 pin</p>	<p>Port I</p>  <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>IP</p> <p>( PI1: To remote control circuit PI4: To interruption circuit PI3: To serial CH0 )</p>	<p>Hi-Z</p>
<p>PI5/<math>\overline{\text{SCK0}}</math> PI6/<math>\overline{\text{SO0}}</math></p> <p>2 pins</p>	<p>Port I</p>  <p>Port I function select</p> <p>From serial CH0</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>MPX</p> <p>IP</p> <p>Note) PI6 is not schmitt input</p> <p>Schmitt input</p> <p>To SI0</p>	<p>Hi-Z</p>
<p>PH0/KR0 to PH2/KR2</p> <p>3 pins</p>	<p>Port H</p>  <p>Port H data</p> <p>Port H direction</p> <p>Data bus</p> <p>RD (Port H)</p> <p>MPX</p> <p>IP</p> <p>Key input signal</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop.</li> </ul>	<p>Hi-Z</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level.</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>	 <p>Mask option</p> <p>Pull-up resistor</p> <p>Schmitt input</p>	<p>Low level</p>
<p>MP</p> <p>1 pin</p>	 <p>CPU mode</p>	<p>Hi-Z</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	AV <sub>DD</sub>	AV <sub>SS</sub> to +7.0* <sup>1</sup>	V	
	AV <sub>SS</sub>	-0.3 to +0.3	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>2</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>3</sup>	V	
Display output voltage	V <sub>OD</sub>	V <sub>DD</sub> - 4.0 to V <sub>DD</sub> + 0.3	V	As P-channel transistor is open drain, V <sub>DD</sub> is reference.
High level output current	I <sub>OH</sub>	-5	mA	All pins excluding display outputs (value per pin)* <sup>3</sup>
	I <sub>ODH1</sub>	-15	mA	Display outputs S0 to S7 (value per pin)
	I <sub>ODH2</sub>	-35	mA	Display outputs T0 to T7, and T8/S15 to T15/S8 (value per pin)
High level total output current	∑I <sub>OH</sub>	-50	mA	Total for all pins excluding display outputs
	∑I <sub>ODH</sub>	-100	mA	Total for all display outputs
Low level output current	I <sub>OL</sub>	15	mA	
Low level total output current	∑I <sub>OL</sub>	130	mA	Total for all outputs
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	600	mW	

\*1 AV<sub>DD</sub> and V<sub>DD</sub> should be set to a same voltage.

\*2 V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*3 It specifies output current of general-purpose I/O port.

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.5	5.5		Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during STOP
Analog power supply	AV <sub>DD</sub>	4.5	5.5	V	*1
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*2
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	CMOS schmitt input*3
	V <sub>IHTS</sub>	2.2	V <sub>DD</sub>	V	TTL schmitt input*4
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin*5 TEX pin*6
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*2
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	CMOS schmitt input*3
	V <sub>ILTS</sub>	0	0.8	V	TTL schmitt input*4
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*5 TEX pin*6
Operating temperature	Topr	-20	+75	°C	

\*1 AV<sub>DD</sub> and V<sub>DD</sub> should be set to a same voltage.

\*2 Normal input port (each pin of PA1 to PA4, PC, PF0 to PF3, PF5, PF7, PH, PI2, PI3 and PI6), MP pin

\*3 Each pin of  $\overline{RST}$ , PE0/ $\overline{INT0}$ , PE1/ $\overline{EC0}/\overline{INT2}$ , PF4/ $\overline{SCK1}$ , PF6/SI1, PI1/RMC, PI4/ $\overline{CS0}/\overline{NMI}/\overline{INT1}$ , PI5/ $\overline{SCK0}$ , PI7/SI1 and PG (For PG4 and PG5, when CMOS schmitt input is selected with mask option)

\*4 Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)

\*5 It specifies only when the external clock is input.

\*6 It specifies only when the external event is input.

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA to PC, PE PF4 to PF7, PH, PI1 to PI7, RST*1	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output voltage	VOL	(VOL only)	VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
Display output current	IOH	S0 to S7		-8			mA
		S8/T15 to S15/T8, T0 to T7	VDD = 4.5V, VOH = VDD - 2.5V	-20			mA
Open drain output leakage current (P-CH Tr OFF in state)	ILOL	S0 to S7, S8/T15 to S15/T8, T0 to T7	VDD = 5.5V, VOL = VDD - 35V VFDP = VDD - 35V			-20	μA
Pull-down resistor*3	RL	S0 to S7, S8/T15 to S15/T8, T0 to T7	VDD = 5V, VFDP - VDD = 30V	60	100	270	kΩ
Input current	IIHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
			VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IILE	TEX	VDD = 5.5V, VIH = 5.5V	0.1		10	μA
			VDD = 5.5V, VIL = 0.4V	-0.1		-10	μA
IILR	RST*2	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA	
I/O leakage current	IIZ	PA to PC, PE to PI, AN1 to AN3, MP, RST*2	VDD = 5.5V, VI = 0, 5.5V			±10	μA
Supply current*4	IDD1	VDD, VSS	1/2 dividing clock		25	45	mA
			VDD = 5.5V, 16MHz crystal oscillation (C1 = C2 = 15pF)				
	IDD2		VDD = 3V, 32kHz crystal oscillation 16MHz oscillation stop (C1 = C2 = 47pF)	40	100	mA	
	IDDS1		Sleep mode		1.2	8	μA
			VDD = 5.5V, 16MHz crystal oscillation (C1 = C2 = 15pF)				
IDDS2	VDD = 3V, 32kHz crystal oscillation 16MHz oscillation stop (C1 = C2 = 47pF)	7	30	μA			
IDDS3	Stop mode VDD = 5.5V 16MHz and 32kHz oscillation stop			10	μA		
Input capacity	CIN	Other than S0 to S15, T0 to T7, PA0, PA5 to PA7 PE2 to PE7 PB, VDD, VSS AVDD, AVSS	Clock 1MHz 0V other than the measured pins		10	20	pF

- \*1  $\overline{\text{RST}}$  pin is specified when evaluation mode is in use.
- \*2  $\overline{\text{RST}}$  pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.
- \*3 When built-in pull-down resistor is selected with mask option.
- \*4 When entire output pins are open.

**AC Characteristics**

**(1) Clock timing**

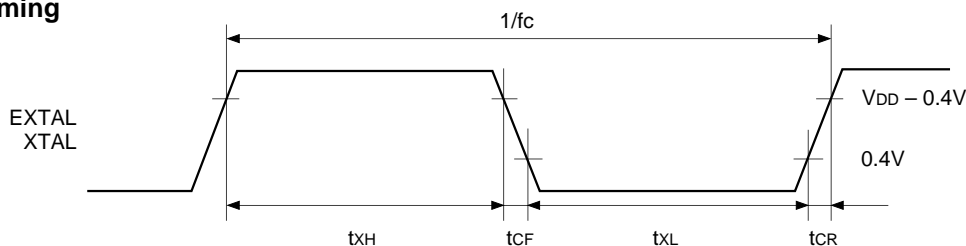
( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	$f_c$	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	$t_{xL}$ , $t_{xH}$	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise and fall times	$t_{cR}$ , $t_{cF}$	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count clock input pulse width	$t_{eH}$ , $t_{eL}$	$\overline{\text{EC0}}$ , $\overline{\text{EC1}}$ , $\overline{\text{EC2}}$	Fig. 3	$t_{\text{sys}} + 200^*$			ns
Event count clock input rise and fall times	$t_{eR}$ , $t_{eF}$	$\overline{\text{EC0}}$ , $\overline{\text{EC1}}$ , $\overline{\text{EC2}}$	Fig. 3			20	ms
System clock frequency	$f_c$	TEX TX	$V_{DD} = 2.7$ to $5.5\text{V}$ Fig. 2 (32kHz clock applying condition)		32.768		kHz
Event count clock input pulse width	$t_{tL}$ , $t_{tH}$	TEX	Fig. 3	10			$\mu\text{s}$
Event count clock input rise and fall times	$t_{tR}$ , $t_{tF}$	TEX	Fig. 3			20	ms

\*  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$$t_{\text{sys}} [\text{ns}] = 2000/f_c \text{ (Upper 2 bits = "00")}, 4000/f_c \text{ (Upper 2 bits = "01")}, 16000/f_c \text{ (Upper 2 bits = "11")}$$

**Fig. 1. Clock timing**



**Fig. 2. Clock applying condition**

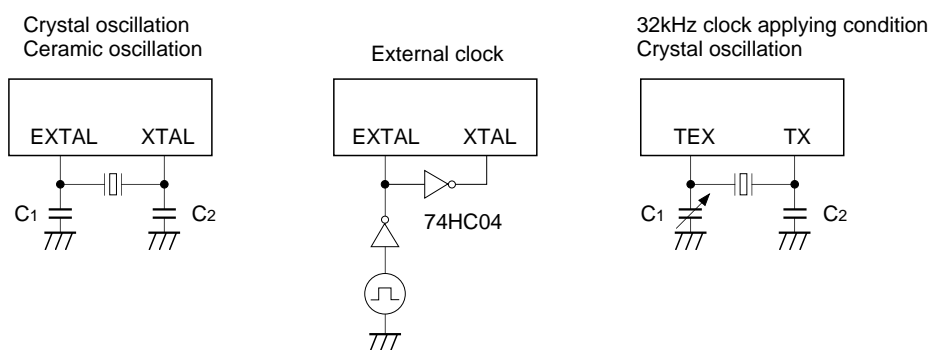
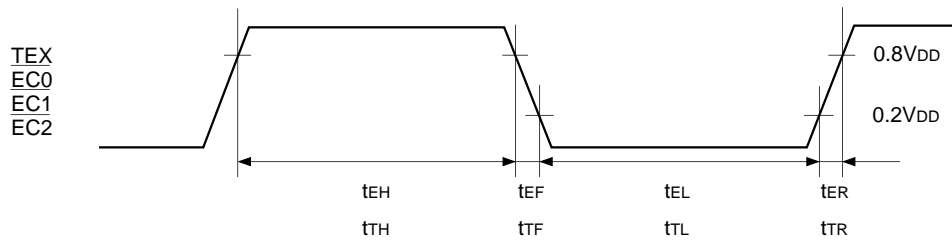


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

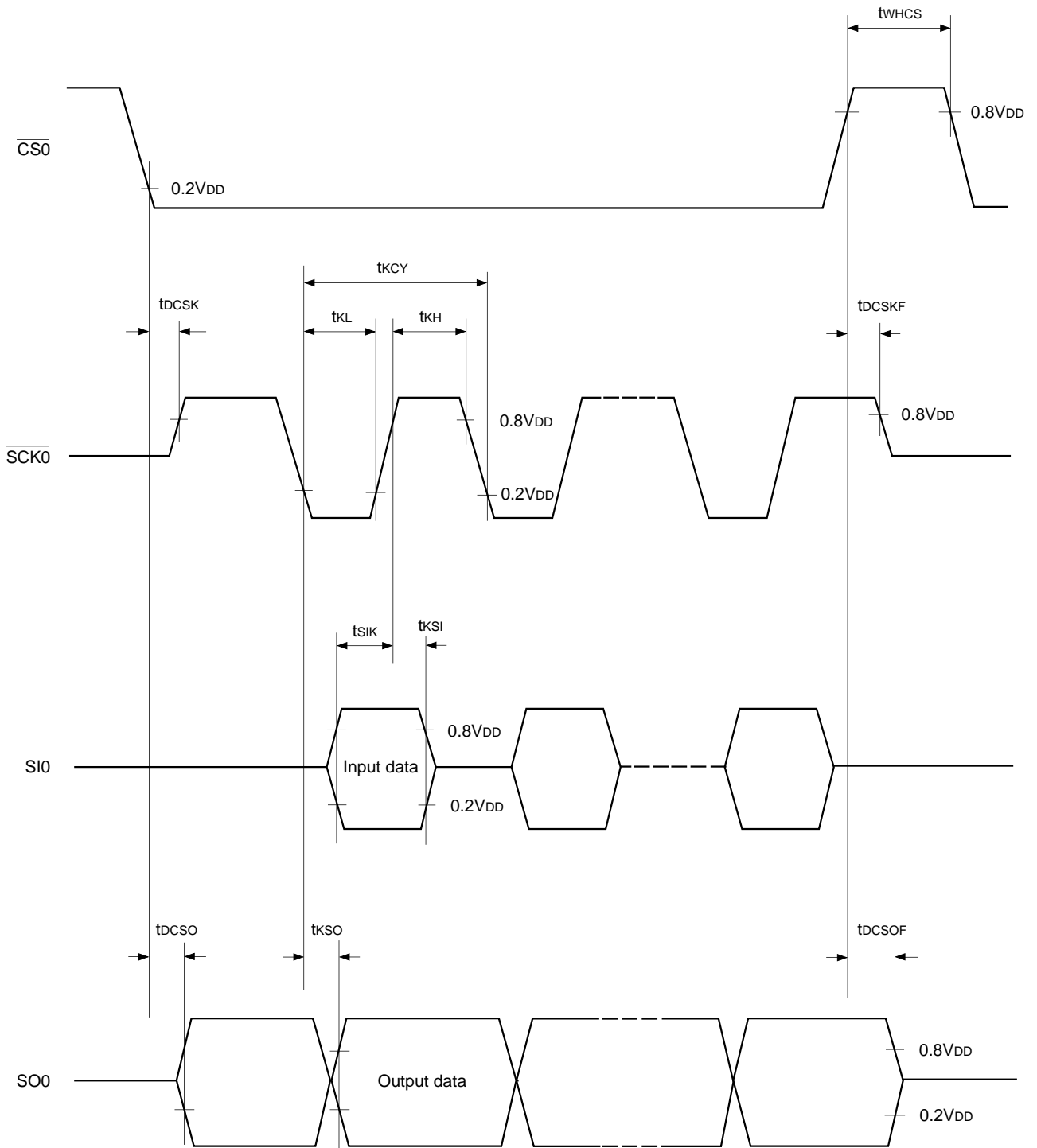
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	$t_{\text{DCSK}}$	$\overline{\text{SCK0}}$	Chip select transfer mode ( $\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ floating delay time	$t_{\text{DCSKF}}$	$\overline{\text{SCK0}}$	Chip select transfer mode ( $\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	$t_{\text{DCSO}}$	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ floating delay time	$t_{\text{DCSOF}}$	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}}$ high level width	$t_{\text{WHCS}}$	$\overline{\text{CS0}}$	Chip select transfer mode	$t_{\text{sys}} + 200$		ns
$\overline{\text{SCK0}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK0}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/\text{fc}$		ns
$\overline{\text{SCK0}}$ high and low level widths	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK0}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/\text{fc} - 50$		ns
SI0 input set-up time (against $\overline{\text{SCK0}} \uparrow$ )	$t_{\text{SIK}}$	SI0	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (against $\overline{\text{SCK0}} \uparrow$ )	$t_{\text{KSI}}$	SI0	$\overline{\text{SCK0}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	$t_{\text{KSO}}$	SO0	$\overline{\text{SCK0}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

**Note 1)**  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (address; 00FE<sub>H</sub>) upper 2 bits (CPU clock selection).

$t_{\text{sys}}$  [ns] =  $2000/\text{fc}$  (Upper 2 bits = "00"),  $4000/\text{fc}$  (Upper 2 bits = "01"),  $16000/\text{fc}$  (Upper 2 bits = "11")

**Note 2)** The load of  $\overline{\text{SCK0}}$  output mode and SO0 output delay time is  $50\text{pF} + 1\text{TTL}$ .

Fig. 4. Serial transfer CH0 timing



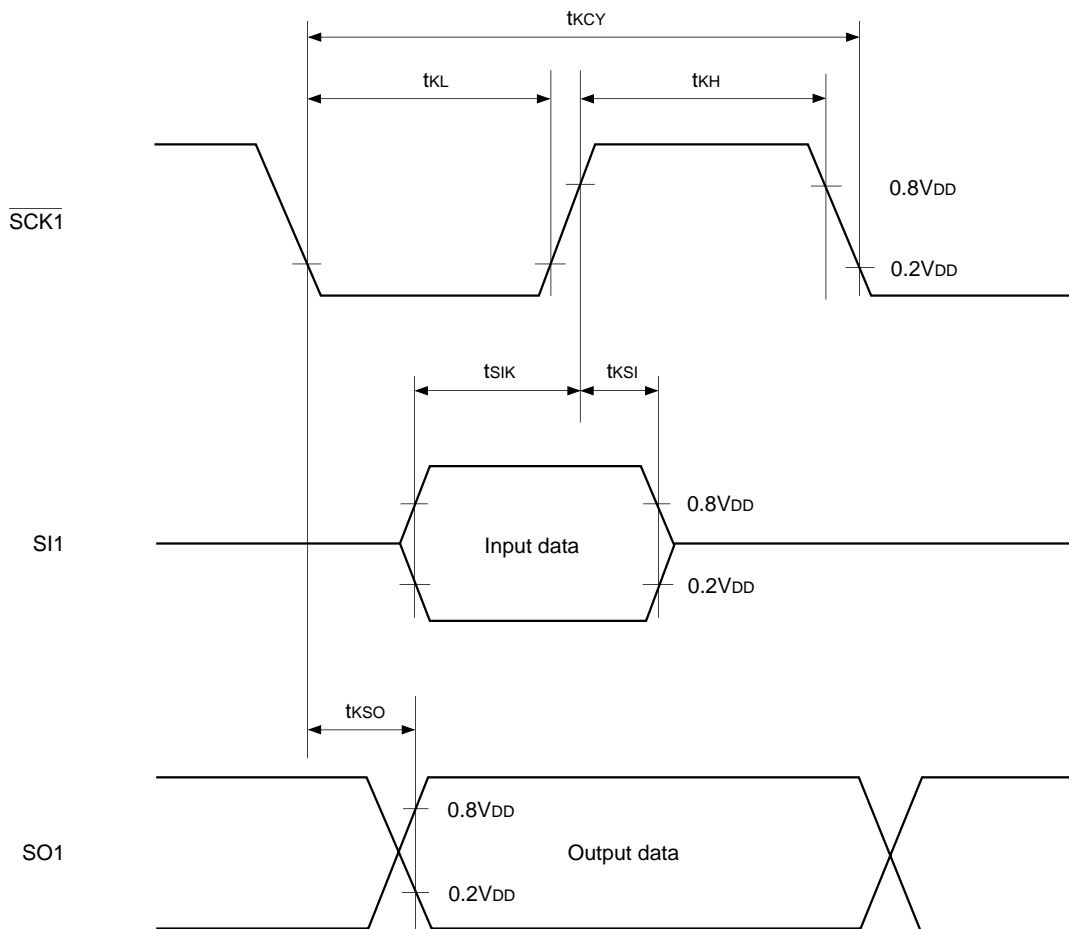
**Serial transfer (CH1)**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level widths	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input set-up time (against $\overline{\text{SCK1}} \uparrow$ )	$t_{\text{SIK}}$	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}} \uparrow$ )	$t_{\text{KSI}}$	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	$t_{\text{KSO}}$	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

**Note)** The load of  $\overline{\text{SCK1}}$  output mode and SO1 output delay time is  $50\text{pF} + 1\text{TTL}$ .

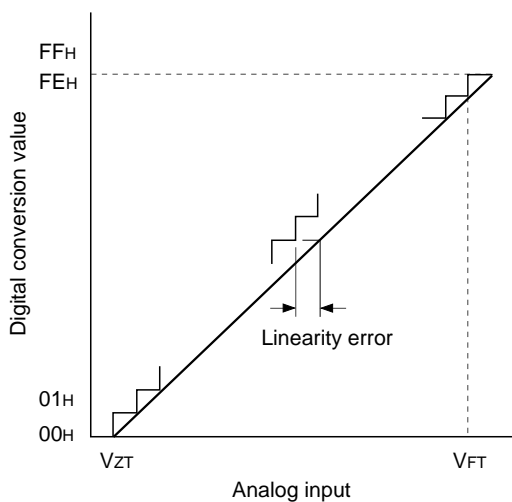
**Fig. 5. Serial transfer CH1 timing**



**(3) A/D converter characteristics** (Ta = -20 to +75°C, VDD = AVDD = 4.5 to 5.5V, AVREF = 4.0 to AVDD, VSS = AVSS = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation Ta = 25°C			±1	LSB
Absolute error			VDD = AVDD = AVREF = 5.0V VDD = AVSS = 0V			±2	LSB
Conversion time	t <sub>CONV</sub>			160/f <sub>ADC</sub>			µs
Sampling time	t <sub>SAMP</sub>			12/f <sub>ADC</sub>			µs
Reference input voltage	V <sub>REF</sub>	AV <sub>REF</sub>	VDD = AVDD = 4.5 to 5.5V	AVDD - 0.5		AVDD	V
Analog input voltage	V <sub>IAN</sub>	AN0 to AN7		0		AV <sub>REF</sub>	V
AV <sub>REF</sub> current	I <sub>REF</sub>	AV <sub>REF</sub>	Operation mode AV <sub>REF</sub> = 4.0 to 5.5V		0.6	1.0	mA
			SLEEP mode STOP mode 32kHz operation mode				10

**Fig. 6. Definitions of A/D converter terms**

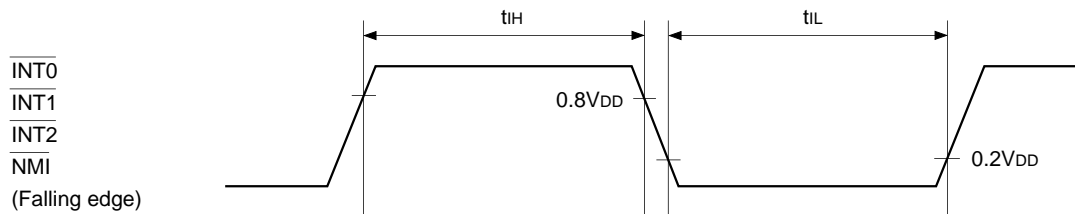


\* The value of f<sub>ADC</sub> is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).  
 When PS2 is selected, f<sub>ADC</sub> = fc/2  
 When PS1 is selected, f<sub>ADC</sub> = fc

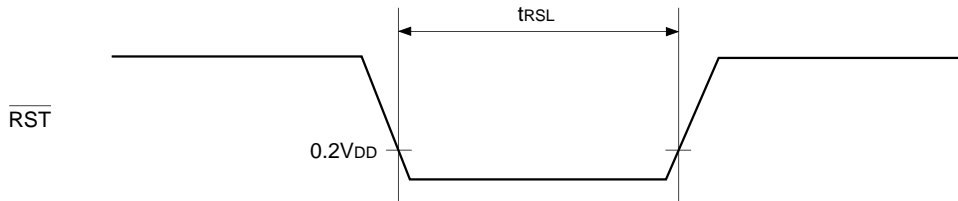
**(4) Interruption, reset input** (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t <sub>IH</sub> t <sub>IL</sub>	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{NMI}}$		1		μs
Reset input low level width	t <sub>RSL</sub>	$\overline{\text{RST}}$		32/fc		μs

**Fig. 7. Interruption input timing**



**Fig. 8. Reset input timing**



**(5) Others** (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V)

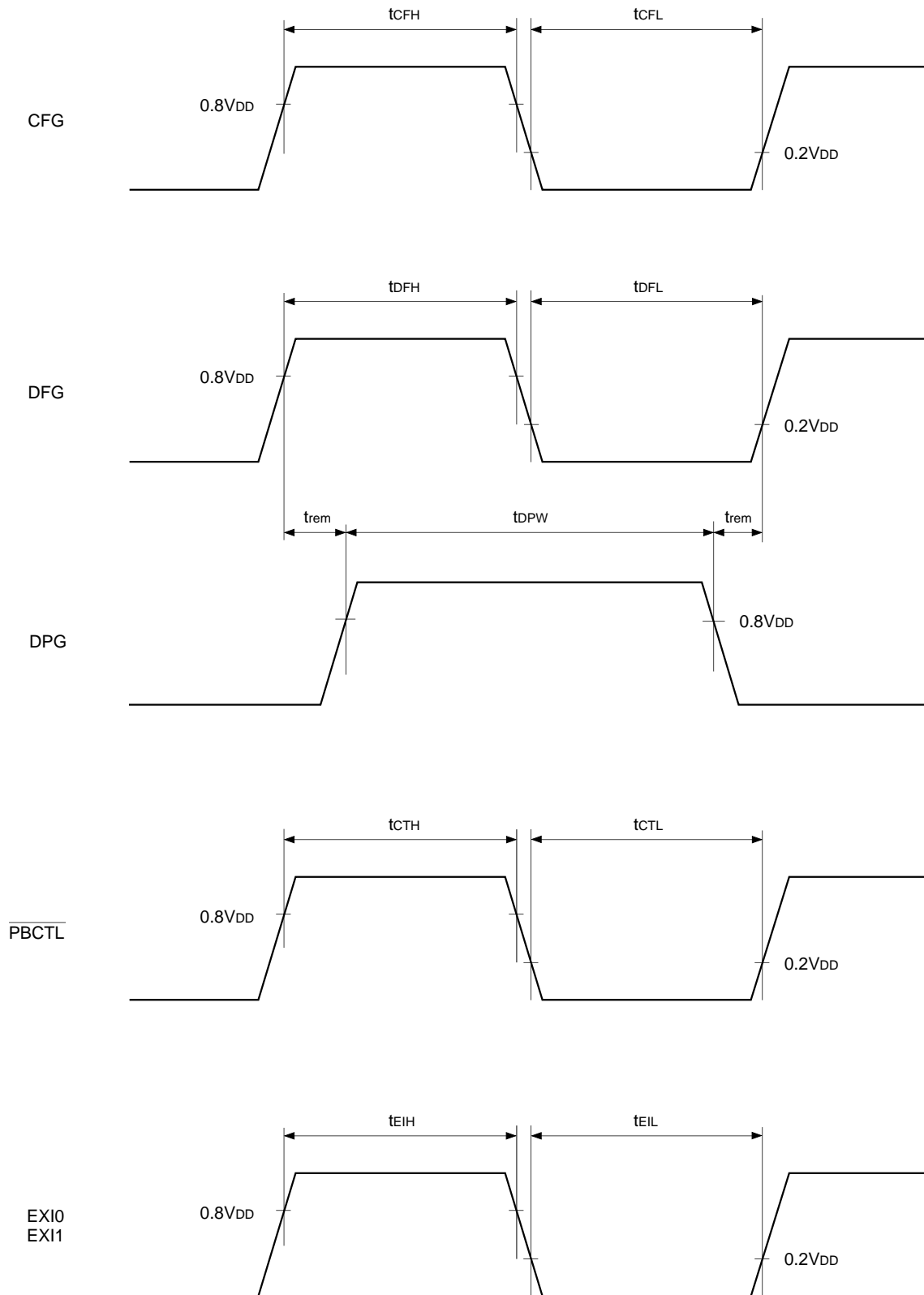
Item	Symbol	Pin	Condition	Min.	Max.	Unit
CFG input high and low level widths	t <sub>CFH</sub> t <sub>CFL</sub>	CFG		t <sub>FRC</sub> × 24 + 200		ns
DFG input high and low level widths	t <sub>DFH</sub> t <sub>DFL</sub>	DFG		t <sub>FRC</sub> × 16 + 200		ns
DPG minimum pulse width	t <sub>DPW</sub>	DPG		t <sub>FRC</sub> × 8 + 200		ns
DPG minimum removal time	t <sub>rem</sub>	DPG		t <sub>FRC</sub> × 16 + 200		ns
$\overline{\text{PBCTL}}$ input high and low level widths	t <sub>CTH</sub> t <sub>CTL</sub>	$\overline{\text{PBCTL}}$	t <sub>sys</sub> = 2000/fc	t <sub>FRC</sub> × 8 + t <sub>sys</sub> + 200		ns
EXI input high and low level widths	t <sub>EIH</sub> t <sub>EIL</sub>	EXI0 EXI1	t <sub>sys</sub> = 2000/fc	t <sub>FRC</sub> × 8 + t <sub>sys</sub> + 200		ns

**Note 1)** t<sub>sys</sub> indicates three values according to the contents of the clock control register (address; 00FE<sub>H</sub>) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

**Note 2)** t<sub>FRC</sub> = 1000/fc (ns)

Fig. 9. Other timings



Supplement

Fig. 10. Recommended oscillation circuit



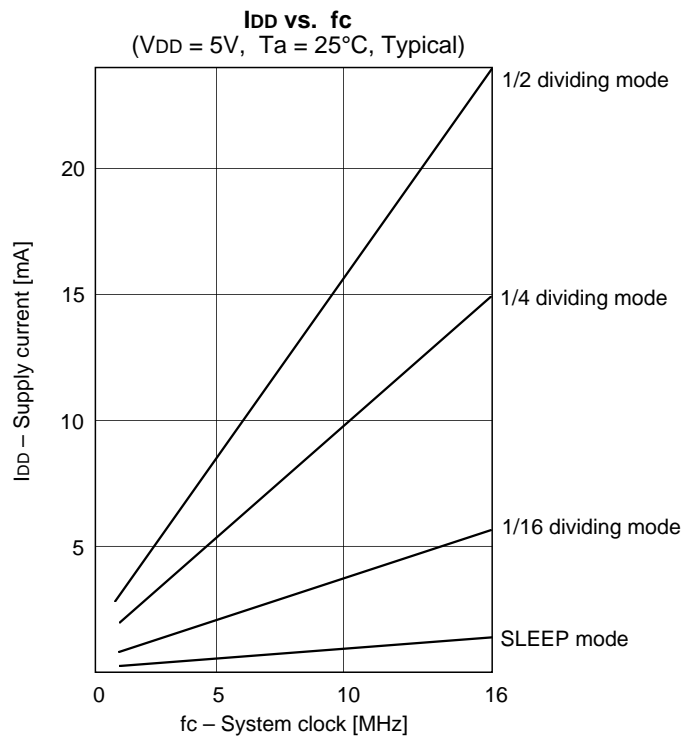
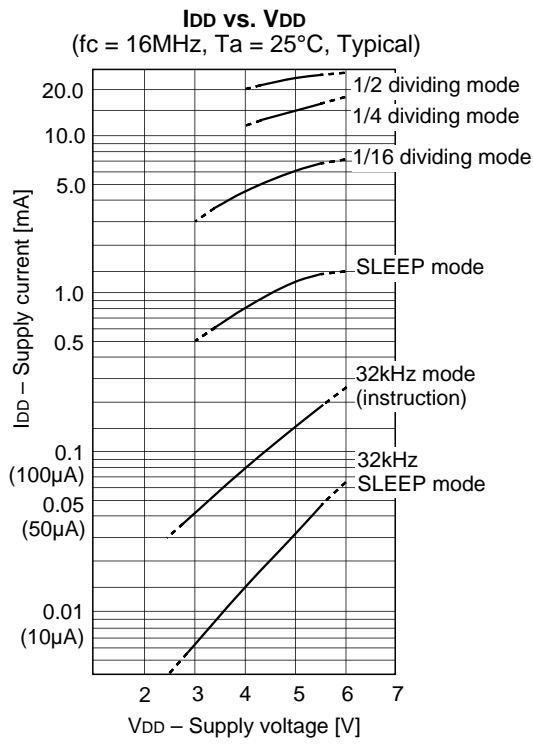
Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	22 (15)	22 (15)	0	(i)
		10.00				
		12.00	15	15		
		16.00	12	12		
	P3	32.768kHz	30	18	470K	(ii)

Mask option table

Item	Content	
	Reset pin pull-up resistor	Non-existent
Power-on reset circuit	Non-existent	
High voltage drive output port pull-down resistor	Non-existent	Existent
Input circuit format*	CMOS schmitt	TTL schmitt

\* In PG4/SYNC0/ $\overline{EC}2$  pin and PG5/SYNC1 pin, the input circuit format can be selected every pin.

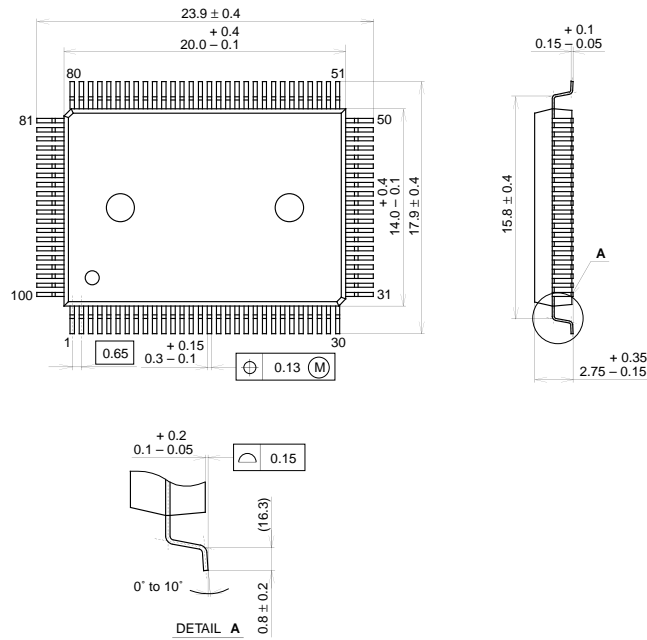
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

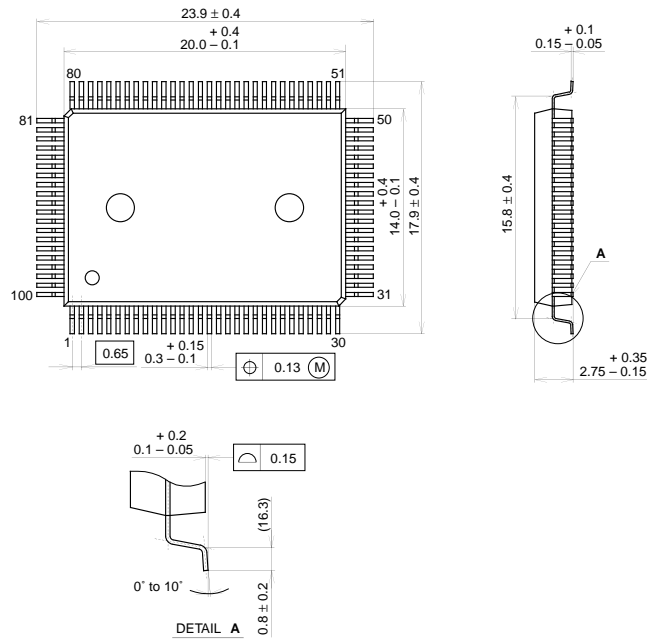


SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm



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