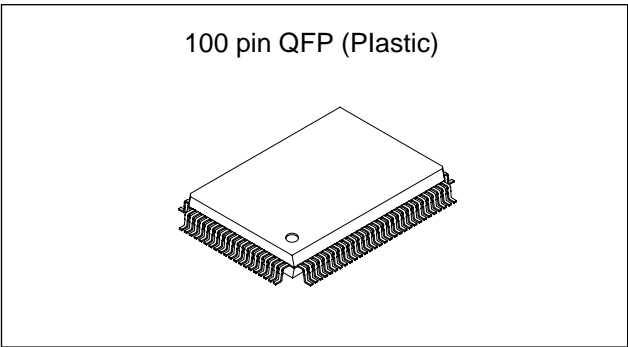


CMOS 8-bit Single Chip Microcomputer

Description

The CXP87940/87948 is a CMOS 8-bit single chip microcomputer which consists of A/D converter, serial interface, timer/counter, time base timer, high precision timing pattern generation circuit, PWM output, VISS/VASS circuit, 32kHz timer/counter, remote control reception circuit, VSYNC separator and the measurement circuit which measures signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port.

Also the CXP87940/87948 provides sleep/stop functions which enable to lower power consumption.



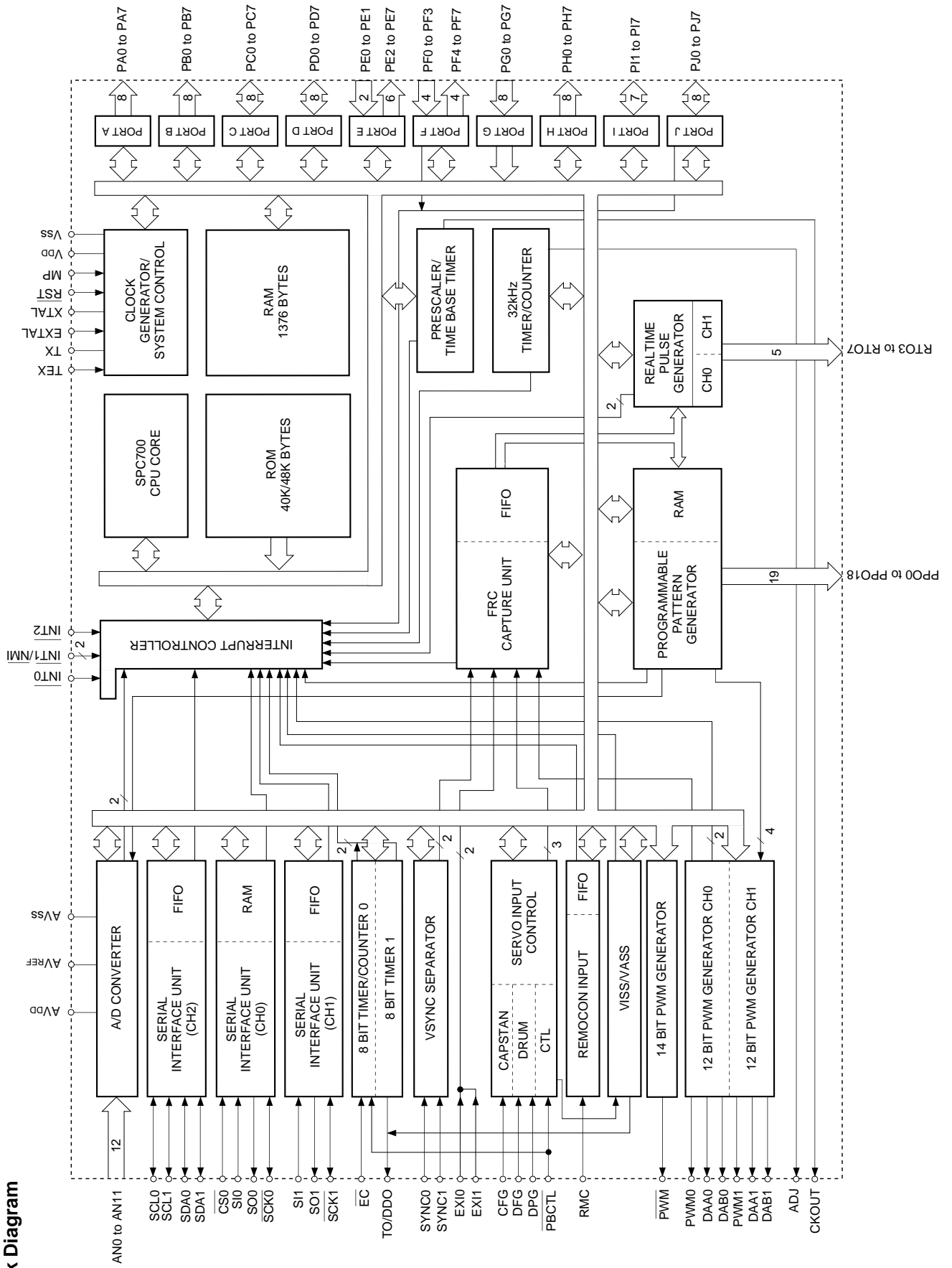
Structure

Silicon gate CMOS IC

Features

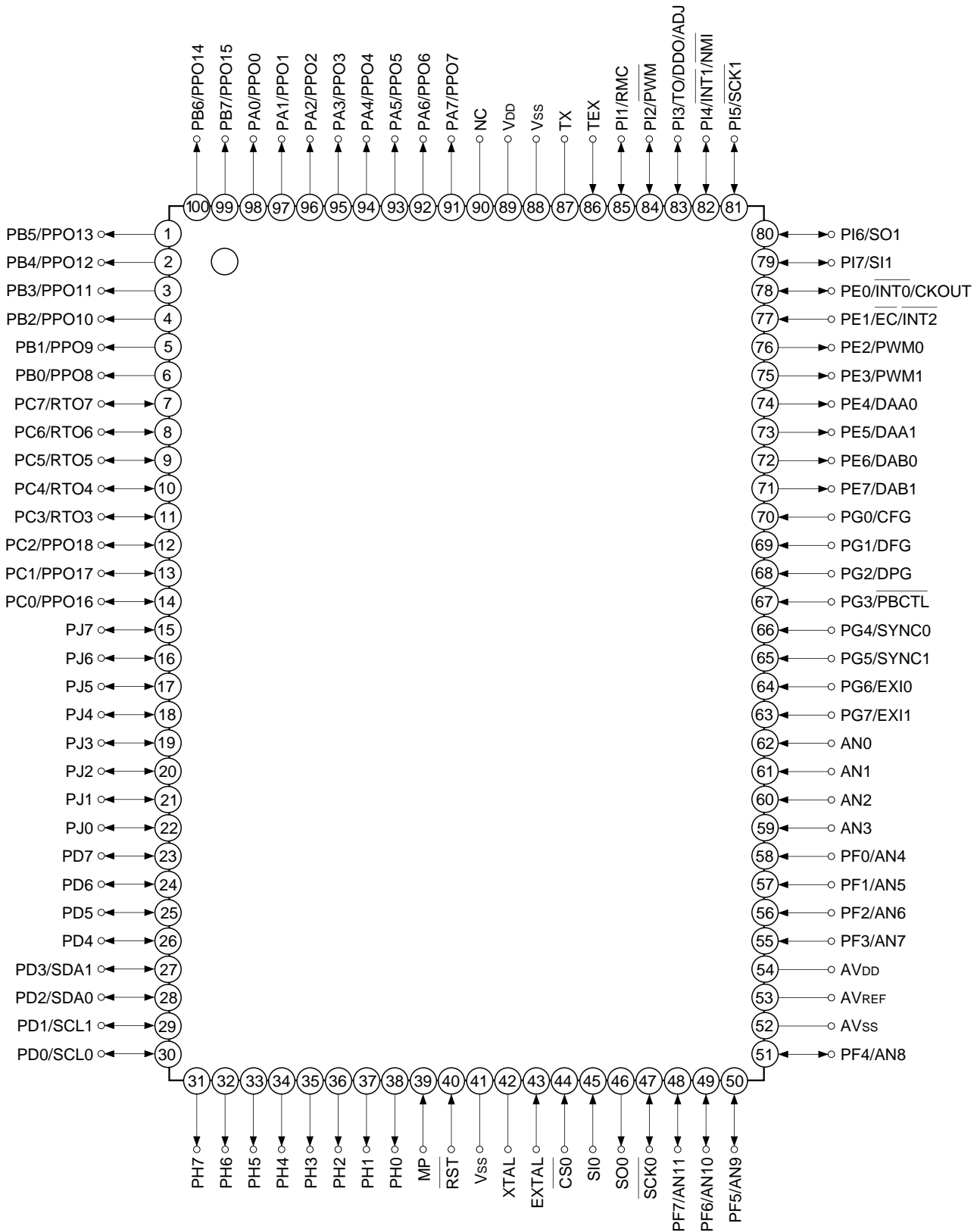
- A wide instruction set (213 instructions) which covers various types of data
 - 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
 - 250ns at 16MHz operation (4.5V to 5.5V)
 - 122µs at 32kHz operation (2.7V to 5.5V)
- Incorporated ROM capacity 40K bytes (CXP87940), 48K bytes (CXP87948)
- Incorporated RAM capacity 1376 bytes
- Peripheral functions
 - A/D converter 8 bits, 12 channels, successive approximation method (Conversion time of 20.0µs at 16MHz)
 - Serial Interface Incorporated buffer RAM (Auto transfer for 1 to 32 bytes), 1 channel
Incorporated 8-bit and 8-stage FIFO (Auto transfer for 1 to 8 bytes), 1 channel
Incorporated two-wire 8-bit and 8-stage FIFO (Auto transfer for 1 to 8 bytes), 1 channel
 - Timer 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 32kHz timer/counter
 - High-precision timing pattern generator PPG: maximum of 19 pins, 32 stages programmable
RTG: 5 pins, 2 channels
 - PWM/DA gate output PWM: 12 bits, 2 channels (Repetitive frequency of 62kHz at 16MHz)
DA gate pulse output: 13 bits, 4 channels
Capstan FG, drum FG/PG, CTL input
 - Servo input control Incorporated 26-bit and 8-stage FIFO
 - VSYNC separator 14 bits
 - FRC capture unit Pulse duty auto detection circuit
 - PWM output 8-bit pulse measurement counter with on-chip 6-stage FIFO
 - VISS/VASS circuit 22 factors, 15 vectors, multi-interruption possible
 - Remote control reception circuit Sleep/stop
- Interruption 100-pin plastic QFP
- Standby mode CXP87800 100-pin ceramic PQFP
- Package
- Piggyback/evaluator

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Block Diagram

Pin Assignment (Top View)



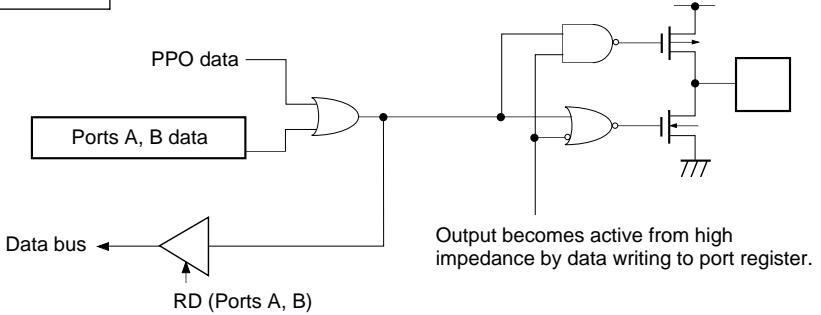
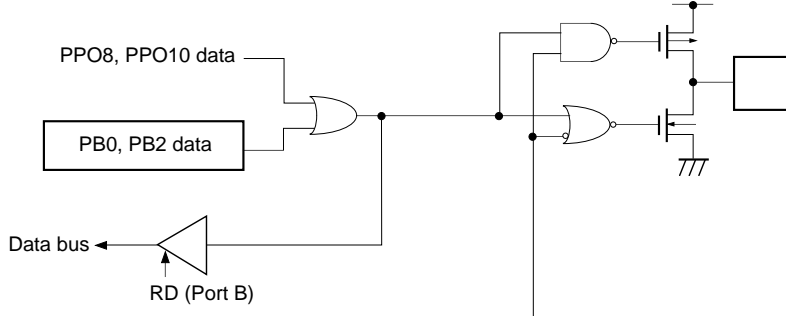
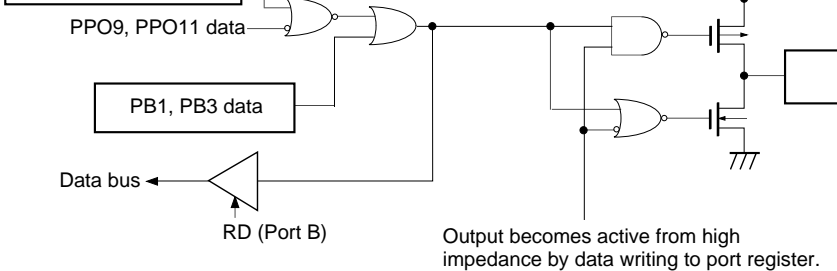
- Note** 1. NC (Pin 90) is always connected to VDD.
 2. VSS (Pins 41 and 88) are both connected to GND.
 3. MP (Pin 39) is always connected to GND.

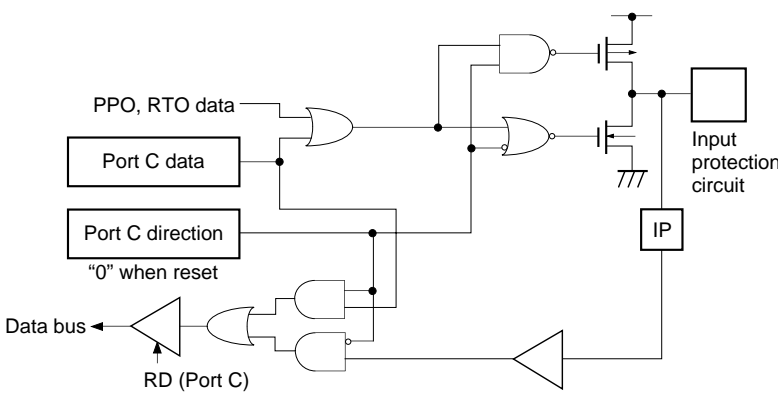
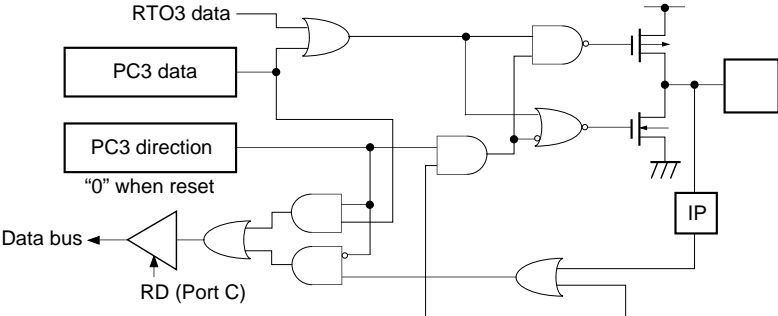
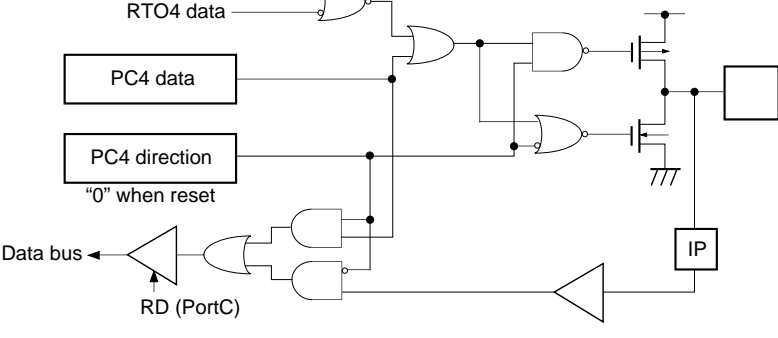
Pin Description

Symbol	I/O	Description		
PA0/PPO0 to PA7/PPO7	Output/ Real-time output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high-precision real-time pulse output port. PB0 and PB2 can be 3-state controlled with PPG. (19 pins)	
PB0/PPO8 to PB7/PPO15	Output/ Real-time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)		
PC0/PPO16 to PC2/PPO18	I/O/ Real-time output	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)		
PC3/RTO3 to PC7/RTO7	I/O/ Real-time output		Real-time pulse generator (RTG) output. Functions as high-precision real-time pulse output port. PC3 can be 3-state controlled with RTG. (5 pins)	
PD0/SCL0 PD1/SCL1	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits for upper 4 bits. Can drive 12mA sink current. Lower 4-bit output is N-ch open drain. (8 pins)	Serial clock (CH2) I/O. (2 pins)	
PD2/SDA0 PD3/SDA1			Serial data (CH2) I/O. (2 pins)	
PD4 to PD7				
PE0/ $\overline{\text{INT0}}$ / CKOUT	Input/Input/Output	(Port E) 8-bit port. Lower 2 bits are for inputs; upper 6 bits are for outputs. (8 pins)	Input to request external interruption. Active at the falling edge.	System clock frequency dividing output.
PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$	Input/Input/Input		External event input for timer/counter.	Input to request external interruption. Active at the falling edge.
PE2/PWM0	Output/Output		PWM outputs. (2 pins)	
PE3/PWM1	Output/Output			
PE4/DAA0	Output/Output			
PE5/DAA1	Output/Output			
PE6/DAB0	Output/Output		DA gate pulse outputs. (4 pins)	
PE7/DAB1	Output/Output			
AN0 to AN3	Input	Analog inputs to A/D converter. (12 pins)		
PF0/AN4 to PF3/AN7	Input/Input	(Port F) 8-bit port. Lower 4 bits are for inputs; upper 4 bits are for outputs. Lower 4 bits also serve as standby release input pin. (8 pins)		
PF4/AN8 to PF7/AN11	Output/Input			
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O.		
SO0	Output	Serial data (CH0) output.		
SI0	Input	Serial data (CH0) input.		
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input.		

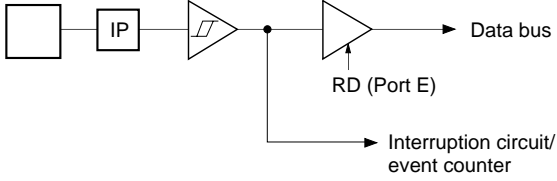
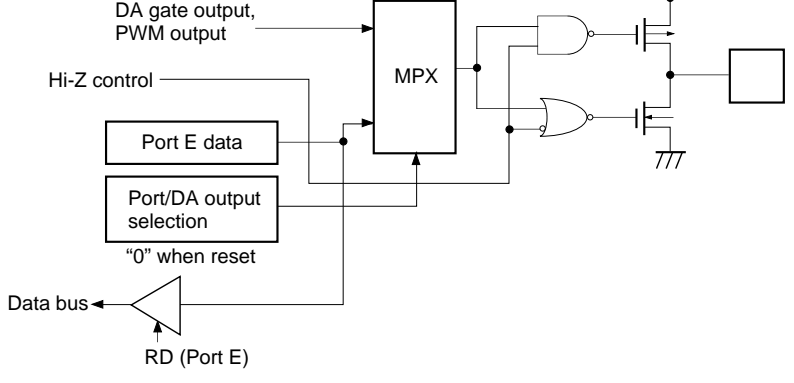
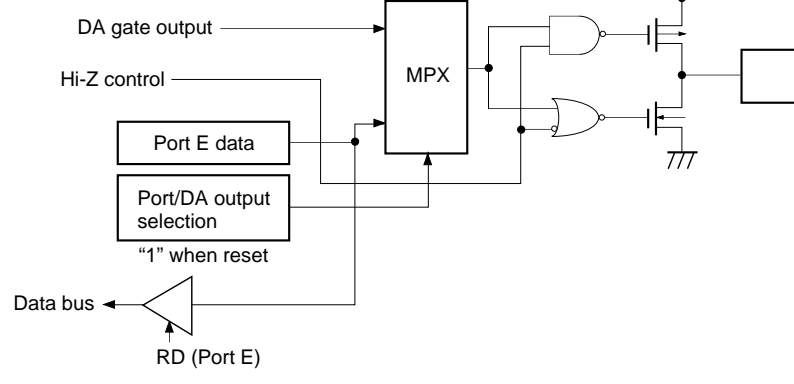
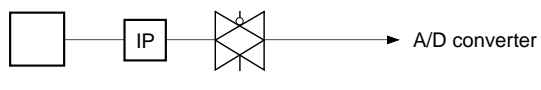
Symbol	I/O	Description	
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input.
PG1/DFG	Input/Input		Drum FG input.
PG2/DPG	Input/Input		Drum PG input.
PG3/ $\overline{\text{PBCTL}}$	Input/Input		Playback CTL pulse input. External event input for timer/counter.
PG4/SYNC0	Input/Input		Composite sync signal input. (2 pins)
PG5/SYNC1	Input/Input		
PG6/EXI0	Input/Input		External input to FRC capture unit. (2 pins)
PG7/EXI1	Input/Input		
PH0 to PH7	Output	(Port H) 8-bit output port. N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O port can be set in a unit of single bits. (7 pins)	Remote control reception circuit input.
PI2/ $\overline{\text{PWM}}$	I/O/Output		14-bit PWM output.
PI3/TO/ DDO/ADJ	I/O/Output/ Output/Output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output.
PI4/ $\overline{\text{INT1}}$ / NMI	I/O/Input/Input		Input to request external interruption and non-maskable interruption. Active at the falling edge.
PI5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O.
PI6/SO1	I/O/Output		Serial data (CH1) output.
PI7/SI1	I/O/Input		Serial data (CH1) input.
PJ0 to PJ7	I/O		(Port J) 8-bit I/O port. I/O and standby release input function can be set in a unit of single bits.
EXTAL	Input	Connects a crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL and input the opposite phase clock to XTAL .	
XTAL	Output		
TEX	Input	Connects a crystal oscillator for 32kHz timer/counter clock. The 32kHz crystal oscillator is inserted between TEX and TX. When used as event input, connect the clock source to TEX and leave TX open.	
TX	Output		
$\overline{\text{RST}}$	Input	System reset; active at Low level.	
MP	Input	Test mode input. Always connect to GND.	
AV _{DD}		Positive power supply of A/D converter.	
AV _{REF}	Input	Reference voltage input of A/D converter.	
AV _{SS}		GND of A/D converter.	
V _{DD}		Positive power supply. Connect V _{DD} pin to V _{DD} .	
NC		No connected. Connect to V _{DD} in normal operation.	
V _{SS}		GND. Connect both V _{SS} pins to GND.	

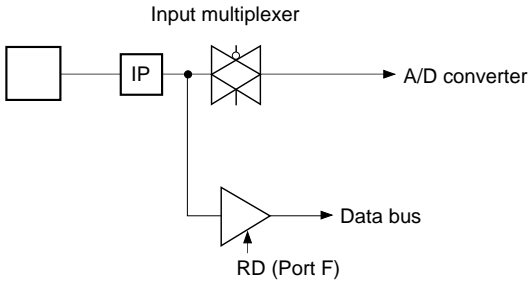
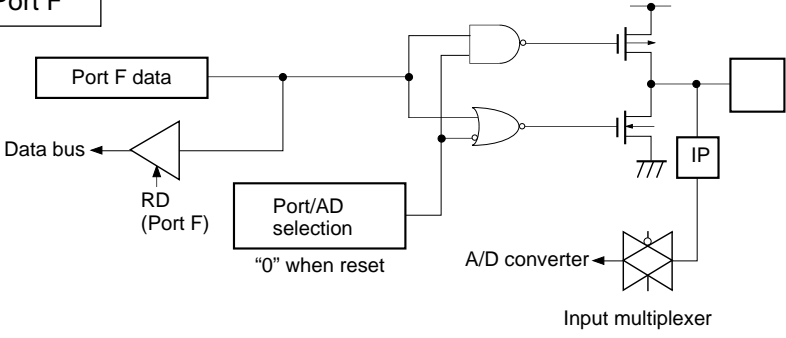
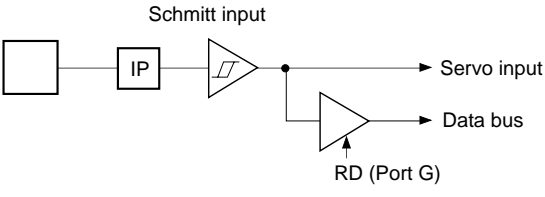
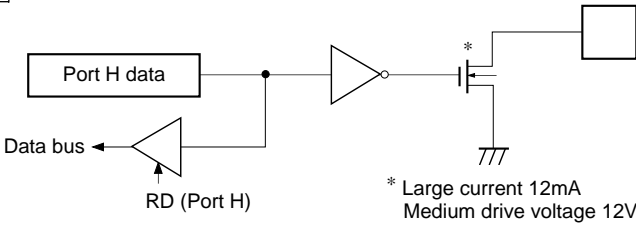
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>Port A Port B</p> <p>PA0 /PPO0 to PA7/PPO7</p> <p>PB4/PPO12 to PB7/PPO15</p> <p>12 pins</p>	 <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>PB0/PPO8 PB2/PPO10</p> <p>2 pins</p>	 <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>PPG control status register bit 0 3-state control selection</p> <p>PB1/PPO9 PB3/PPO11</p> <p>2 pins</p>	 <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PC0/PPO16 to PC2/PPO18</p> <p>PC5/RTO5 to PC7/RTO7</p> <p>6 pins</p>	<p>Port C</p> 	<p>Hi-Z</p>
<p>PC3/RTO3</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>PC4/RTO4</p> <p>1 pin</p>	 <p>RTO data is OR-gate data of CH0 and CH1.</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PD0/SCL0 PD1/SCL1 PD2/SDA0 PD3/SDA1</p> <p>4 pins</p>	<p>Port D</p> <p>SCL, SDA</p> <p>Serial interface CH2 output enable</p> <p>Port D data</p> <p>Data bus</p> <p>RD (Port D)</p> <p>SCL, SDA (Serial interface CH2 circuit)</p> <p>Schmitt input</p> <p>BUS SW</p> <p>To another serial CH2 pin</p> <p>* Large current 12mA</p>	<p>Hi-Z</p>
<p>PD4 to PD7</p> <p>4 pins</p>	<p>Port D</p> <p>Port D data</p> <p>Port D direction</p> <p>"0" when reset</p> <p>Data bus</p> <p>RD (Port D)</p> <p>* Large current 12mA</p>	<p>Hi-Z</p>
<p>PE0/$\overline{\text{INT0}}$/ CKOUT</p> <p>1 pin</p>	<p>Port E</p> <p>ESL0</p> <p>Port E selection</p> <p>ESL1</p> <p>PS1 01 PS2 10 PS3 11</p> <p>MPX</p> <p>Data bus</p> <p>RD (Port E)</p> <p>Interruption circuit</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE1/$\overline{\text{EC}}/\overline{\text{INT2}}$</p> <p>1 pin</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1</p> <p>4 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE6/DAB0 PE7/DAB1</p> <p>2 pins</p>	<p>Port E</p> 	<p>High level</p>
<p>AN0 to AN3</p> <p>4 pins</p>	<p>Input multiplexer</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PF0/AN4 to PF3/AN7</p> <p>4 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PF4/AN8 to PF7/AN11</p> <p>4 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1</p> <p>8 pins</p>	<p>Port G</p>  <p>Note) For PG4/SYNC0, PG5/SYNC1, CMOS Schmitt input and TTL Schmitt input can be selected with the mask option.</p>	<p>Hi-Z</p>
<p>PH0 to PH7</p> <p>8 pins</p>	<p>Port H</p>  <p>* Large current 12mA Medium drive voltage 12V</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PI2/$\overline{\text{PWM}}$ PI3/$\overline{\text{TO}}$/ DDO/$\overline{\text{ADJ}}$</p> <p>2 pins</p>	<p>Port I</p> <p>Port I function selection "0" when reset</p> <p>PI2...14-bit PWM PI3...Timer/counter, CTL duty detection circuit, 32kHz timer</p> <p>Port I data</p> <p>Port I direction "0" when reset</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>IP</p>	<p>Hi-Z</p>
<p>PI1/$\overline{\text{RMC}}$ PI4/$\overline{\text{INT1/NMI}}$ PI7/$\overline{\text{SI1}}$</p> <p>3 pins</p>	<p>Port I</p> <p>Port I data</p> <p>Port I direction "0" when reset</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Schmitt input</p> <p>IP</p> <p>(PI1...Remote control circuit PI4...Interruption circuit PI7...Serial interface CH1</p>	<p>Hi-Z</p>
<p>PI5/$\overline{\text{SCK1}}$ PI6/$\overline{\text{SO1}}$</p> <p>2 pins</p>	<p>Port I</p> <p>Port I function selection "0" when reset Serial interface CH1</p> <p>Port I data</p> <p>Port I direction "0" when reset</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>MPX</p> <p>IP</p> <p>Serial interface CH1</p> <p>PI6 is not Schmitt input.</p>	<p>Hi-Z</p>
<p>PJ0 to PJ7</p> <p>8 pins</p>	<p>Port J</p> <p>Port J data</p> <p>Port J direction "0" when reset</p> <p>Data bus</p> <p>RD (PortJ)</p> <p>Edge detection</p> <p>Standby release</p> <p>Data bus</p> <p>RD (Port J direction)</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
$\overline{CS0}$ SIO 2 pins		Hi-Z
$SO0$ 1 pin		Hi-Z
$\overline{SCK0}$ 1 pin		Hi-Z
$EXTAL$ $XTAL$ 2 pins	<ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode and XTAL becomes High level. 	Oscillation
TEX TX 2 pins	<ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs Low level and TX pin outputs High level. 	Oscillation
\overline{RST} 1 pin		Low level

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	-0.3 to +0.3	V	
	AV _{REF}	AV _{SS} to +7.0* ¹	V	
Input voltage	V _{IN}	-0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ²	V	
Medium drive output voltage	V _{OUTP}	-0.3 to +15.0	V	Port H pin
High level output current	I _{OH}	-5	mA	
High level total output current	∑I _{OH}	-50	mA	Total of output pins
Low level output current	I _{OL}	15	mA	Ports excluding large current output (value per pin)
	I _{OLC}	20	mA	Large current output port (value per pin* ³)
Low level total output current	∑I _{OL}	130	mA	Total of output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*¹ AV_{DD} and AV_{REF} should not exceed V_{DD} + 0.3V.

*² V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*³ The large current output ports are the pins of the port D (PD) and Port H (PH).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing modes
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing mode or during sleep mode
		2.7	5.5	V	Guaranteed operation range by TEX clock
		2.0	5.5	V	Guaranteed data hold range during stop mode
Analog voltage	AV _{DD}	4.5	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	Includes the serial CH2 input*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS Schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pin
			5.5	V	CMOS Schmitt input*7
	V _{IHTS}	2.2	5.5	V	TTL Schmitt input*4
V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*5 and TEX pin*6	
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	Includes the serial CH2 input*2
	V _{ILS}	0	0.2V _{DD}	V	CMOS Schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pin
	V _{ILTS}	0	0.8	V	TTL Schmitt input*4
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*5 and TEX pin*6
Operating temperature	Topr	-20	+75	°C	

*1 AV_{DD} and V_{DD} should be set to the same voltage.

*2 Normal input port (PC, PD4 to PD7, PF0 to PF3, PG, PI and PJ), MP pin

*3 SCK0, RST, $\overline{\text{EC/INT2}}$, RMC, $\overline{\text{INT1/NMI}}$, SCK1 and SI1

*4 PG4 and PG5 (When TTL Schmitt input is selected with mask option)

*5 Specifies only when the external clock is input.

*6 Specifies only when the external event count clock is input.

*7 CS0, SI0, and PG (For PG4 and PG5, when CMOS Schmitt input is selected with mask option.)

Electrical Characteristics

DC Characteristics ($V_{DD} = 4.5$ to $5.5V$)

($T_a = -20$ to $+75^\circ C$, $V_{SS} = 0V$ reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PC, PD4 to PD7, PE2 to PE7, PF4 to PF7, PH (V_{OL} only)	$V_{DD} = 4.5V, I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V, I_{OH} = -1.2mA$	3.5			V
Low level output voltage	V_{OL}	PI1 to PI7, PJ, SO0, SCK0	$V_{DD} = 4.5V, I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V, I_{OL} = 3.6mA$			0.6	V
		PD, PH	$V_{DD} = 4.5V, I_{OL} = 12.0mA$			1.5	V
		PD0 to PD3 (SCL0, CSL1, SDA0, SDA1)	$V_{DD} = 4.5V, I_{OL} = 3.0mA$			0.4	V
			$V_{DD} = 4.5V, I_{OL} = 6.0mA$			0.6	V
		Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.5	
I_{ILE}	$V_{DD} = 5.5V, V_{IL} = 0.4V$		-0.5			-40	μA
I_{IHT}	TEX		$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.1		10	μA
I_{ILT}			$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.1		-10	μA
I_{ILR}			\overline{RST}^{*1}	$V_{DD} = 5.5V, V_{IL} = 0.4V$	-1.5		-400
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP, AN0 to AN3, CS0, SI0, SO0, SCK0, \overline{RST}^{*1}	$V_{DD} = 5.5V, V_I = 0, 5.5V$			± 10	μA
Open drain output leakage current (in N-CH Tr off state)	I_{LOH}	PH	$V_{DD} = 5.5V, V_{OH} = 12V$			50	μA
		PD0 to PD3	$V_{DD} = 5.5V, V_{OH} = 5.5V$			10	μA
Serial interface CH2 bus switch connection impedance (in output Tr off state)	RBS	SCL0: SCL1, SDA0: SDA1	$V_{DD} = 4.5V, V_{SCL0} = V_{SCL1} = 2.25V, V_{SDA0} = V_{SDA1} = 2.25V$			120	Ω

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*2	I _{DD1}	V _{DD}	1/2 frequency dividing clock operation		36	50	mA
			V _{DD} = 5.5V, 16MHz crystal oscillation (C ₁ = C ₂ = 16pF)				
	I _{DD2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		60	100	μA
	I _{DDS1}		Sleep mode		2.8	8	mA
			V _{DD} = 5.5V, 16MHz crystal oscillation (C ₁ = C ₂ = 16pF)				
	I _{DDS2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		10	30	μA
I _{DDS3}	Stop mode V _{DD} = 5.5V, termination of 16MHz and 32kHz crystal oscillation				10	μA	
Input capacity	C _{IN}	PC, PD, PE0, PE1, PF, PG, PI1 to PI7, PJ, $\overline{\text{CS0}}$, SI0, $\overline{\text{SCK0}}$, AN0 to AN3, EXTAL, XTAL, TEX, TX, MP, $\overline{\text{RST}}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{\text{RST}}$ pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2 When all output pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t _{XL} , t _{XH}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)	28			ns
System clock input rise and fall times	t _{CR} , t _{CF}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)			200	ns
Event count input clock pulse width	t _{EH} , t _{EL}	\overline{EC}	Fig. 3	4t _{sys} *1			ns
Event count input clock rise and fall times	t _{ER} , t _{EF}	\overline{EC}	Fig. 3			20	ns
System clock frequency	fc	TEX TX	Fig. 2 V _{DD} = 2.7 to 5.5V (32kHz clock applied condition)		32.768		kHz
Event count input clock pulse width	t _{TL} , t _{TH}	TEX	Fig. 3	10			μs
Event count input clock rise and fall times	t _{TR} , t _{TF}	TEX	Fig. 3			20	ms

*1 t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

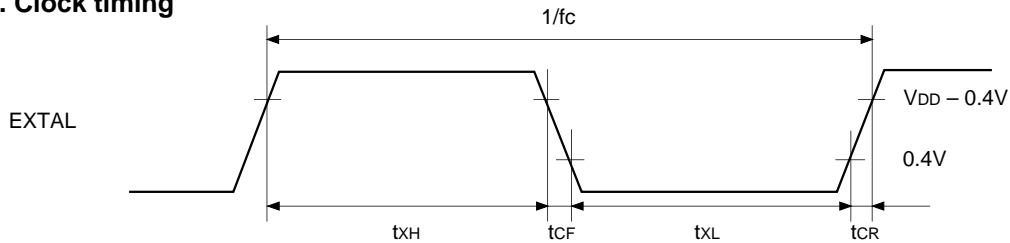


Fig. 2. Clock applied condition

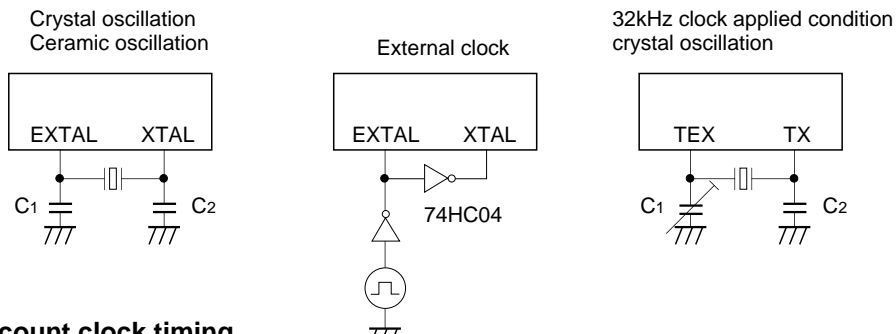
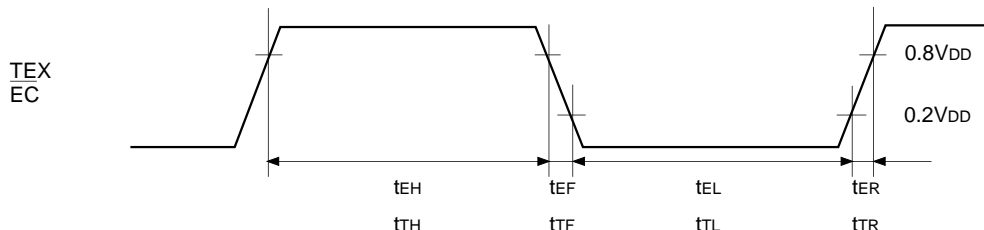


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

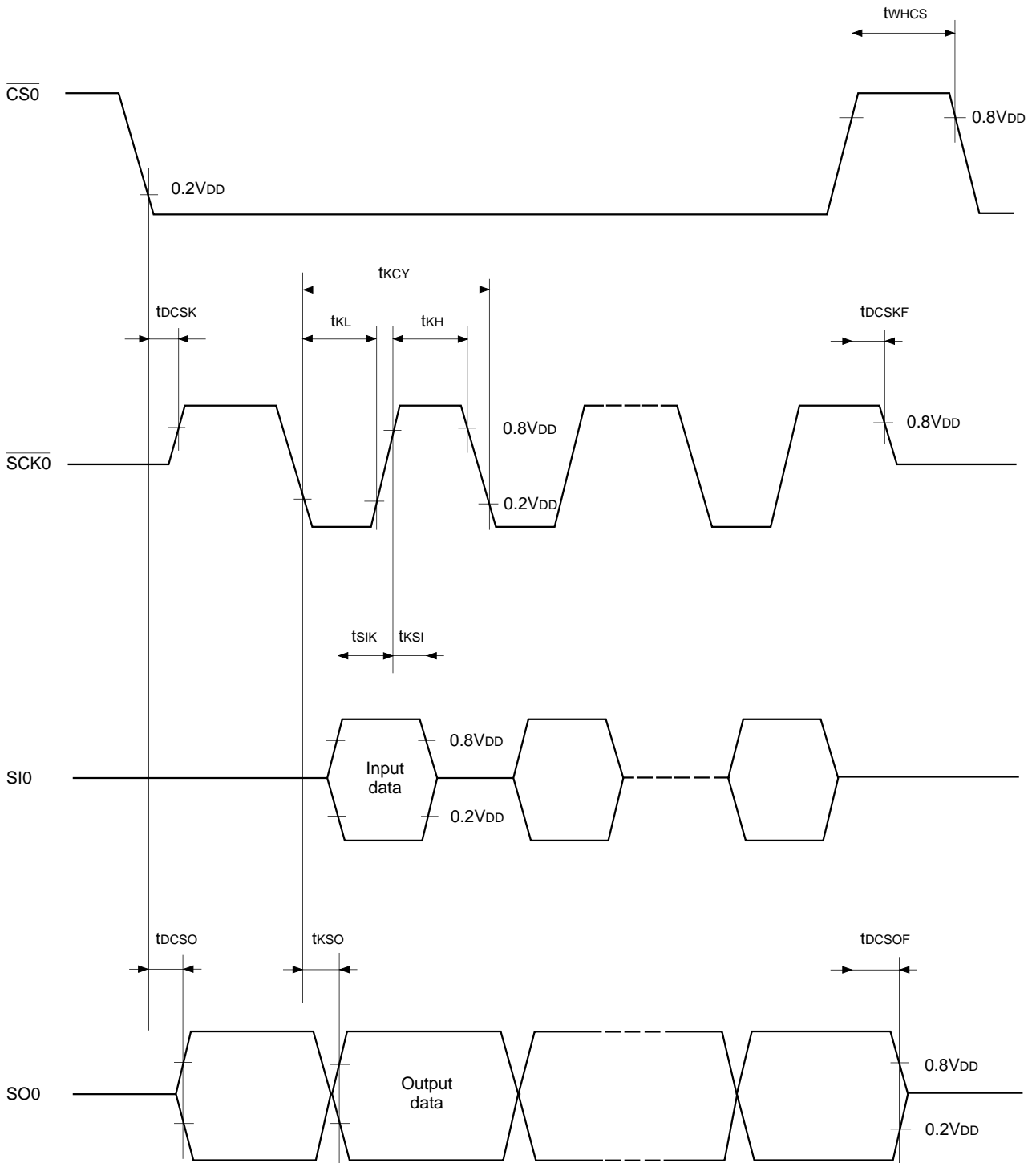
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t _{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode (SCK = output mode)		t _{sys} + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ floating delay time	t _{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode (SCK = output mode)		t _{sys} + 200	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ floating delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS0}}$ High level width	t _{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{\text{SCK0}}$ cycle time	t _{KCY}	$\overline{\text{SCK0}}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK0}}$ High and Low level widths	t _{KH} t _{KL}	$\overline{\text{SCK0}}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 100		ns
SI0 input setup time (for $\overline{\text{SCK0}} \uparrow$)	t _{SIK}	SI0	$\overline{\text{SCK}}$ input mode	-t _{sys} + 100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI0 input hold time (for $\overline{\text{SCK0}} \uparrow$)	t _{KSI}	SI0	$\overline{\text{SCK}}$ input mode	2t _{sys} + 100		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{KSO}	SO0	$\overline{\text{SCK}}$ input mode		2t _{sys} + 200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK0}}$ output mode and SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing



Serial transfer (CH1) (SIO mode)

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

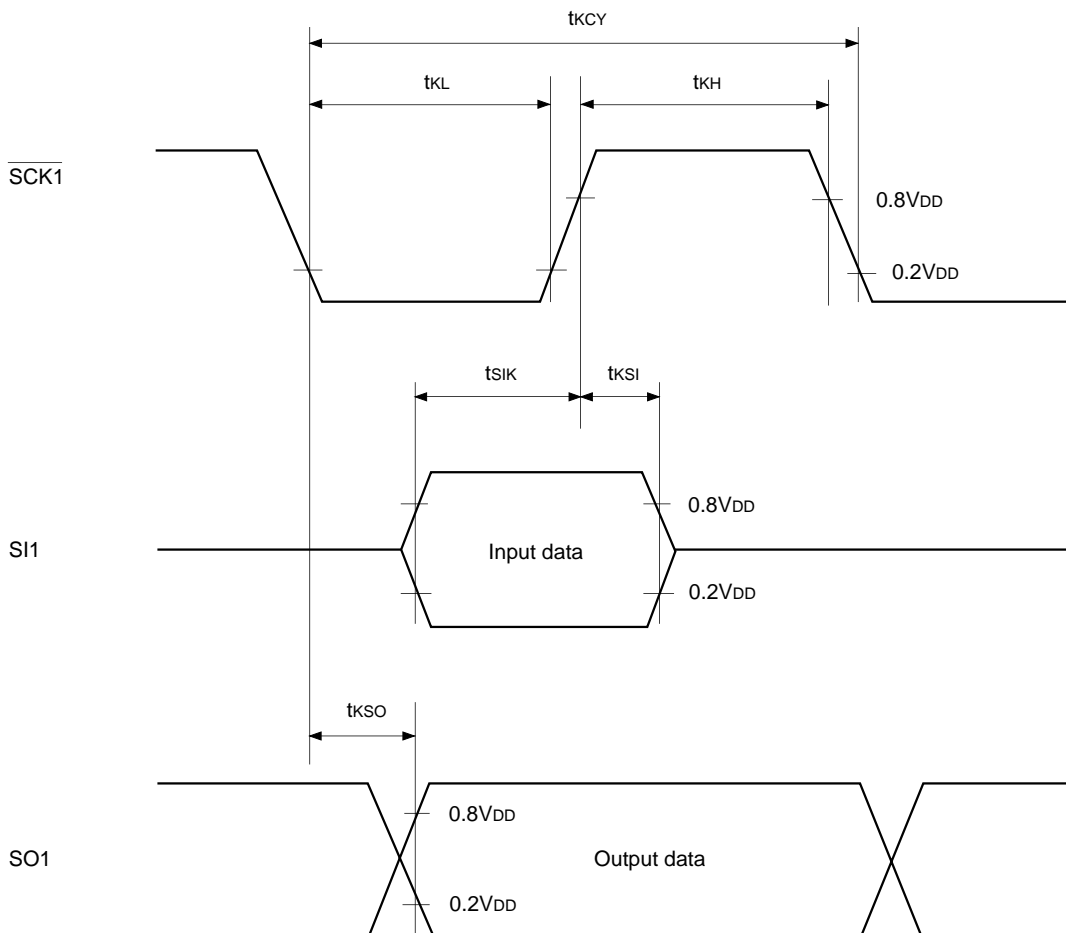
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ High and Low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input setup time (for $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEH) upper 2 bits (CPU clock selection).

$$t_{\text{sys}} [\text{ns}] = 2000/f_c \text{ (Upper 2 bits = "00")}, 4000/f_c \text{ (Upper 2 bits = "01")}, 16000/f_c \text{ (Upper 2 bits = "11")}$$

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

Fig. 5. Serial transfer CH1 timing (SIO mode)



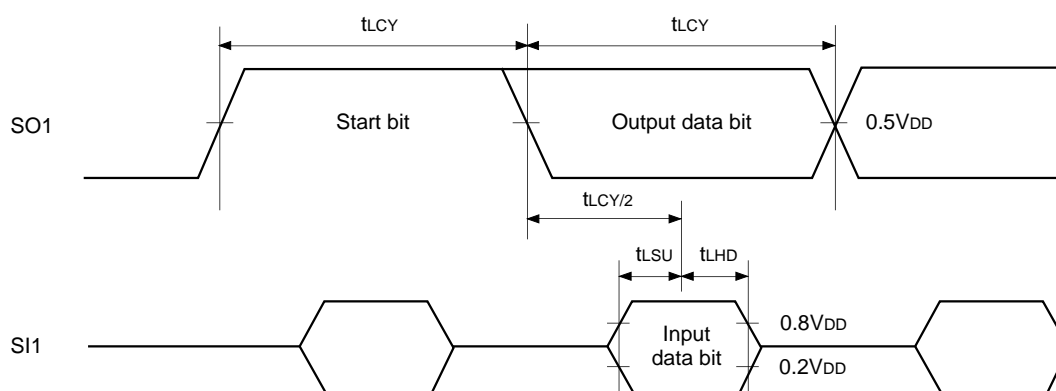
Serial transfer (CH1) (Special mode) ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	*1		104		μs
SI1 data setup time	t_{LSU}	SI1		2			μs
SI1 data hold time	t_{LHD}	SI1		2			μs

*1 t_{LCY} is specified only when serial mode register (CH1) (SIOM1: 05FZH) lower 2 bits (SO1 clock selection) are set at $104\mu\text{s}$.

Note) The load of SO1 pin is $50\text{pF} + 1\text{TTL}$.

Fig. 6. Serial transfer CH1 timing (Special mode)



Serial transfer (CH2)

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL0, SCL1 clock frequency	f_{SCL}	SCL0, SCL1			400	kHz
Bus-free time before starting transfer	t_{BUF}	SDA0, SCL1 SDA0, SCL1		2.6		μs
Hold time for starting transfer	$t_{HD}; STA$	SDA0, SCL1 SDA1, SCL1		1.0		μs
Clock Low level width	t_{LOW}	SCL0, SCL1		1.0		μs
Clock High level width	t_{HIGH}	SCL0, SCL1		1.0		μs
Setup time for repeated transfers	$t_{SU}; STA$	SDA0, SCL0 SDA0, SCL1		1.0		μs
Data hold time	$t_{HD}; DAT$	SDA0, SCL0 SDA1, SCL1		0*1		μs
Data setup time	$t_{SU}; DAT$	SDA0, SCL0 SDA1, SCL1		100		ns
SDA0, SCL0, SDA1, SCL1 rise time	t_R	SDA0, SCL0 SDA1, SCL1			300	ns
SDA0, SCL0, SDA1, SCL1 fall time	t_F	SDA0, SCL0 SDA1, SCL1			300	ns
Setup time for transfer completion	$t_{SU}; STO$	SDA0, SCL0 SDA1, SCL1		1.6		μs

*1 The SCL0, SCL1 fall time (300ns Max.) is not included in the data hold time.

Fig. 7. Serial transfer CH2 timing

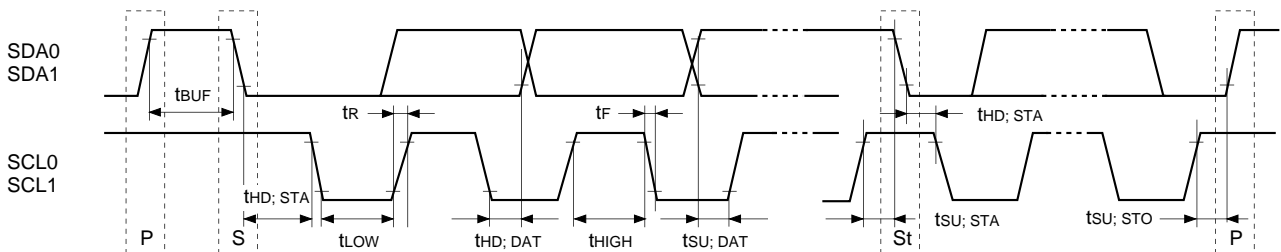
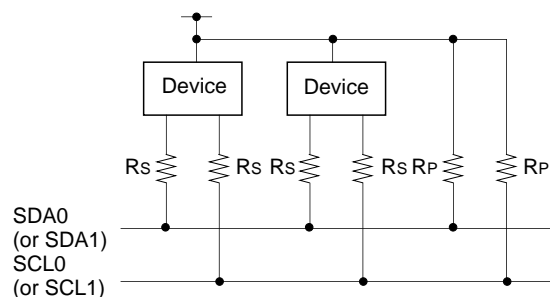


Fig. 8. Device recommended circuit



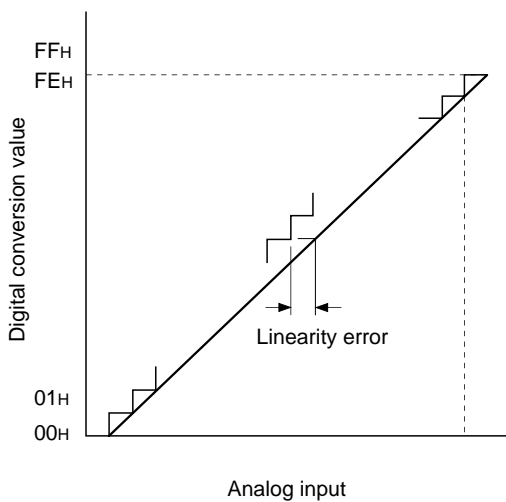
- A pull-up resistor (R_P) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance ($R_S = 300\Omega$ or less) can be used to reduce the spike noise caused by CRT flashover.

(3) A/D converter characteristics

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 1	LSB
Absolute error						± 2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}^{*1}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*1}$			μs
Reference input voltage	V_{REF}	AV_{REF}		$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0		AV_{REF}	V
AVREF current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode 32kHz operation mode			10	μA

Fig. 9. Definitions of A/D converter terms



*1 f_{ADC} indicates the below values due to the peripheral clock control register (PCC: 05F8H) bit 3 and clock control register (CLC: 00FEH) upper 2 bits.

CLC upper 2 bits	PCC bit 3	
	0 ($\phi/2$ selection)	1 (ϕ selection)
00 ($\phi = f_{EX}/2$)	$f_{ADC} = f_c/2$	$f_{ADC} = f_c$
01 ($\phi = f_{EX}/4$)	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ($\phi = f_{EX}/16$)	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

(4) Interruption, reset input (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High and Low level widths	t _{IH} t _{IL}	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ NMI PJ0 to PJ7		1		μs
Reset input Low level width	t _{RSL}	$\overline{\text{RST}}$		32/fc		μs

Fig. 10. Interruption input timing

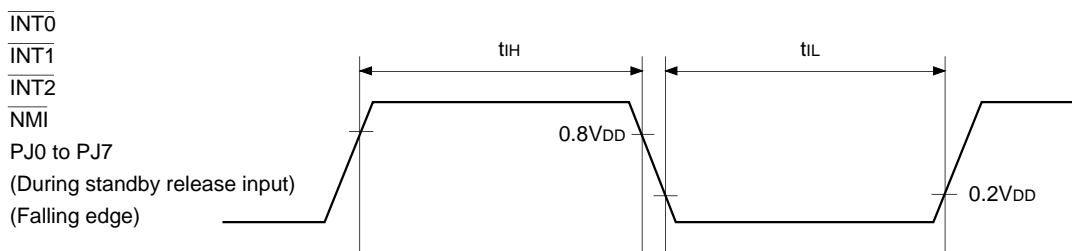
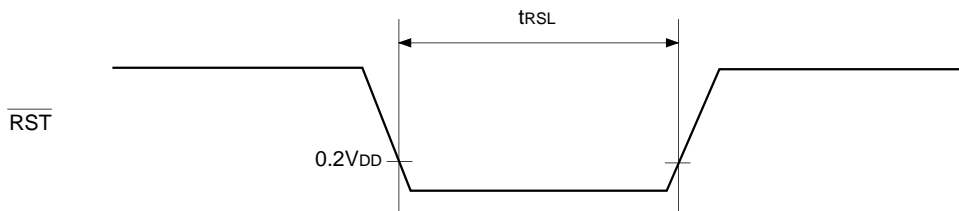


Fig. 11. $\overline{\text{RST}}$ input timing



(5) Others

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

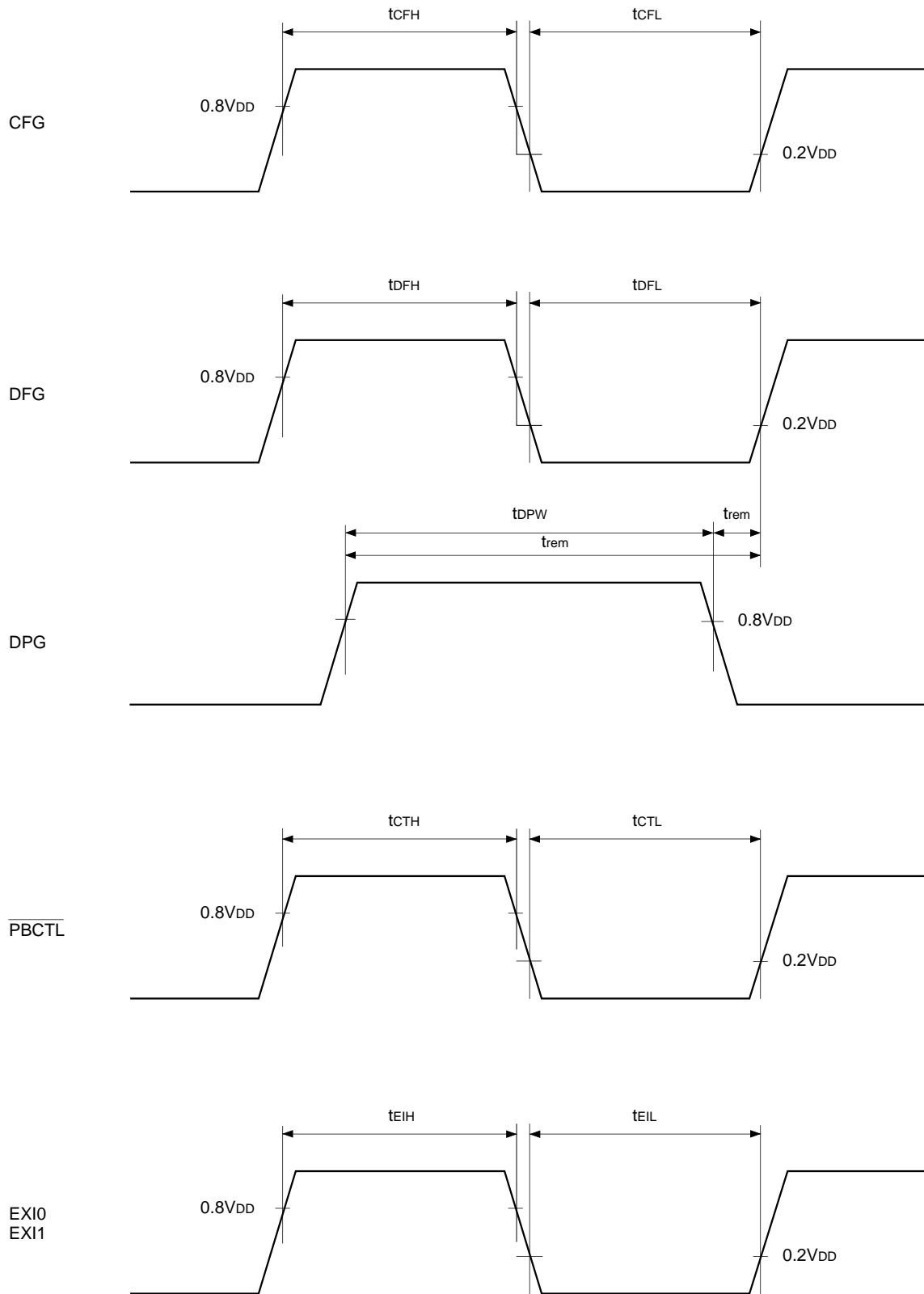
Item	Symbol	Pins	Conditions	Min.	Max.	Unit
CFG input High and Low level widths	t _{CFH} t _{CFL}	CFG		24t _{FRC} + 200		ns
DFG input High and Low level widths	t _{DFH} t _{DFL}	DFG		16t _{FRC} + 200		ns
DPG minimum pulse width	t _{DPW}	DPG		8t _{FRC} + 200		ns
DPG minimum removal time	t _{rem}	DPG		16t _{FRC} + 200		ns
$\overline{\text{PBCTL}}$ input High and Low level widths	t _{CTH} t _{CTL}	$\overline{\text{PBCTL}}$	t _{sys} = 2000/fc	8t _{FRC} + 200 + t _{sys}		ns
EXI input High and Low level widths	t _{EIH} t _{EIL}	EXI0 EXI1	t _{sys} = 2000/fc	8t _{FRC} + 200 + t _{sys}		ns

Note 1) t_{FRC} = 1000/fc [ns]

Note 2) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEH) upper 2 bits (CPU clock selection).

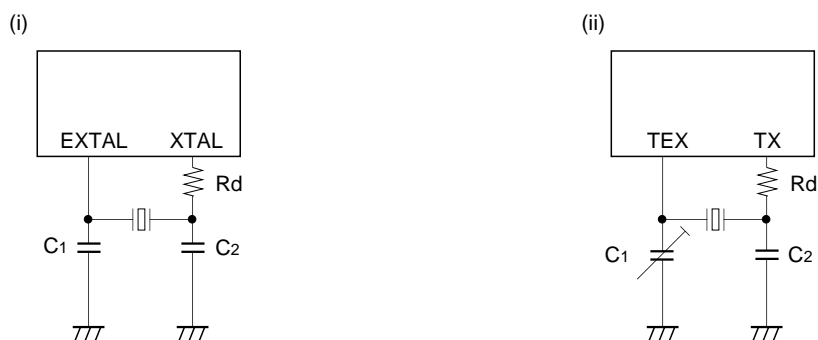
t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 12. Other timings



Appendix

Fig. 13. Recommended oscillation circuit for SPC 700 series



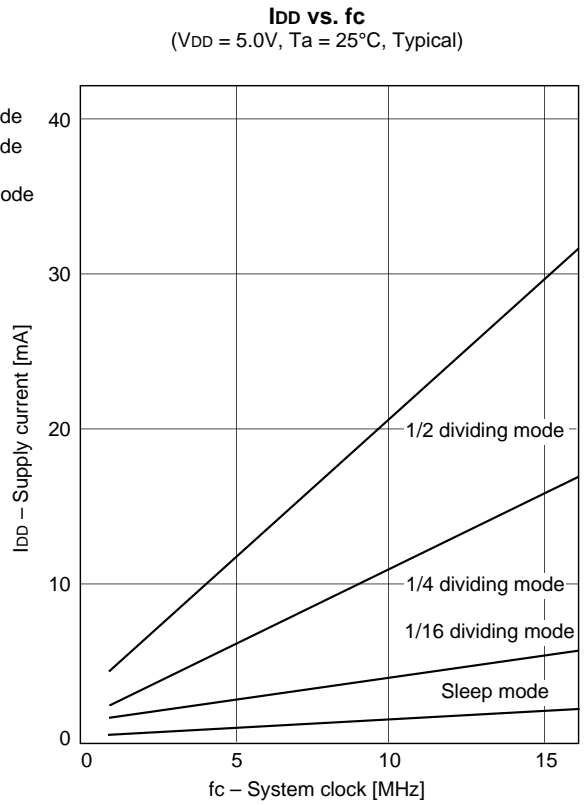
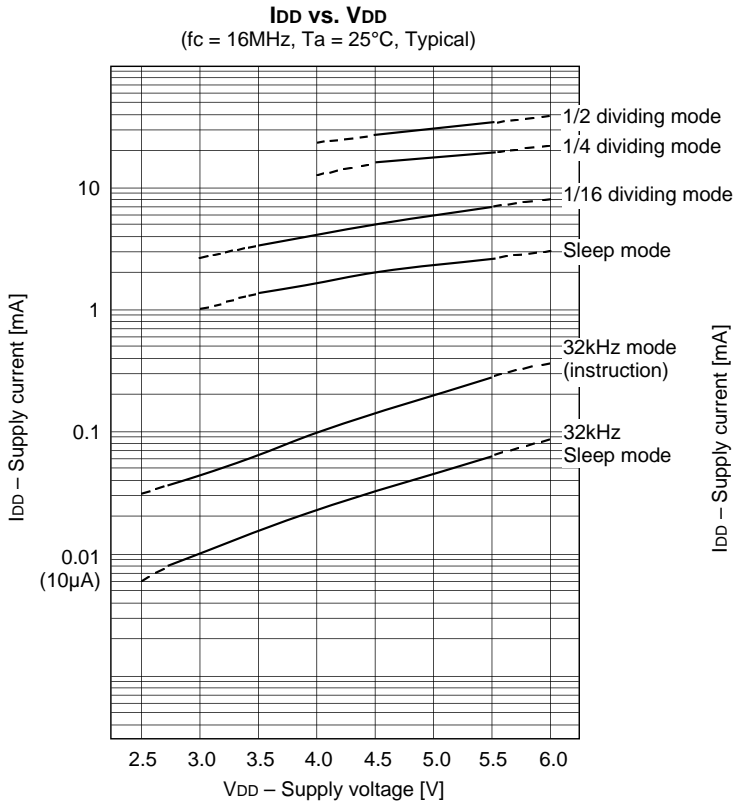
Manufacturer	Model	fc (MHz)	C ₁ (pF)	C ₂ (pF)	R _d (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16	16	0	(i)
		10.00	16	16		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
Input circuit format*1	C-MOS Schmitt	TTL Schmitt

*1 The input circuit format can be selected for PG4/SYNC0 and PG5/SYNC1, respectively.

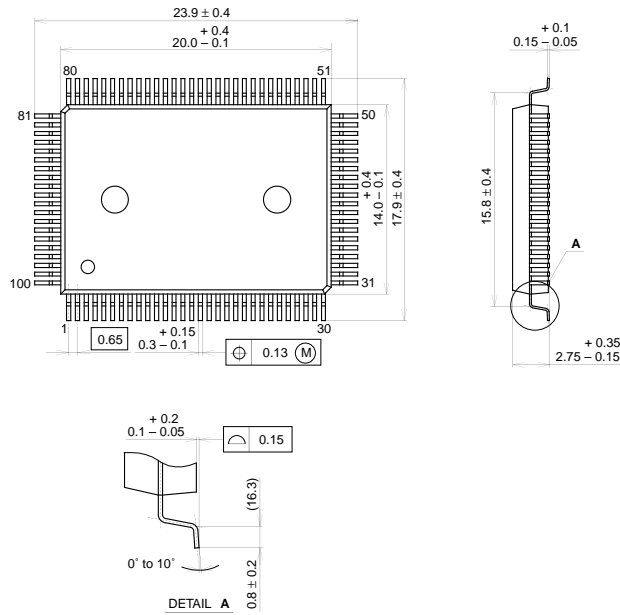
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

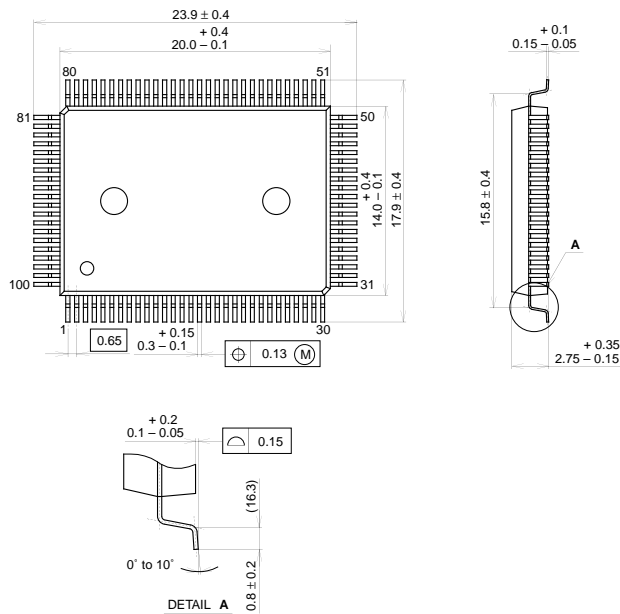


PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm



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