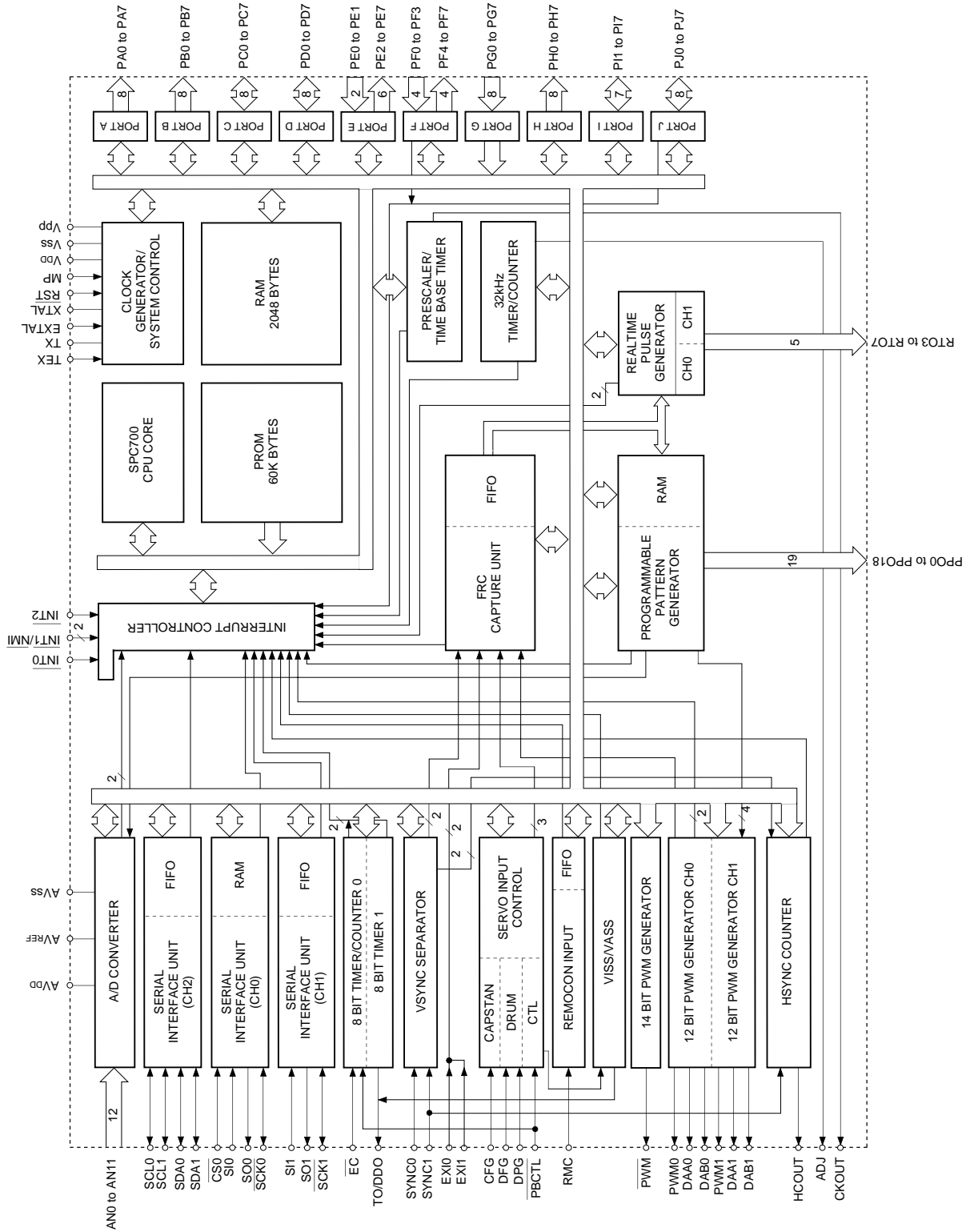
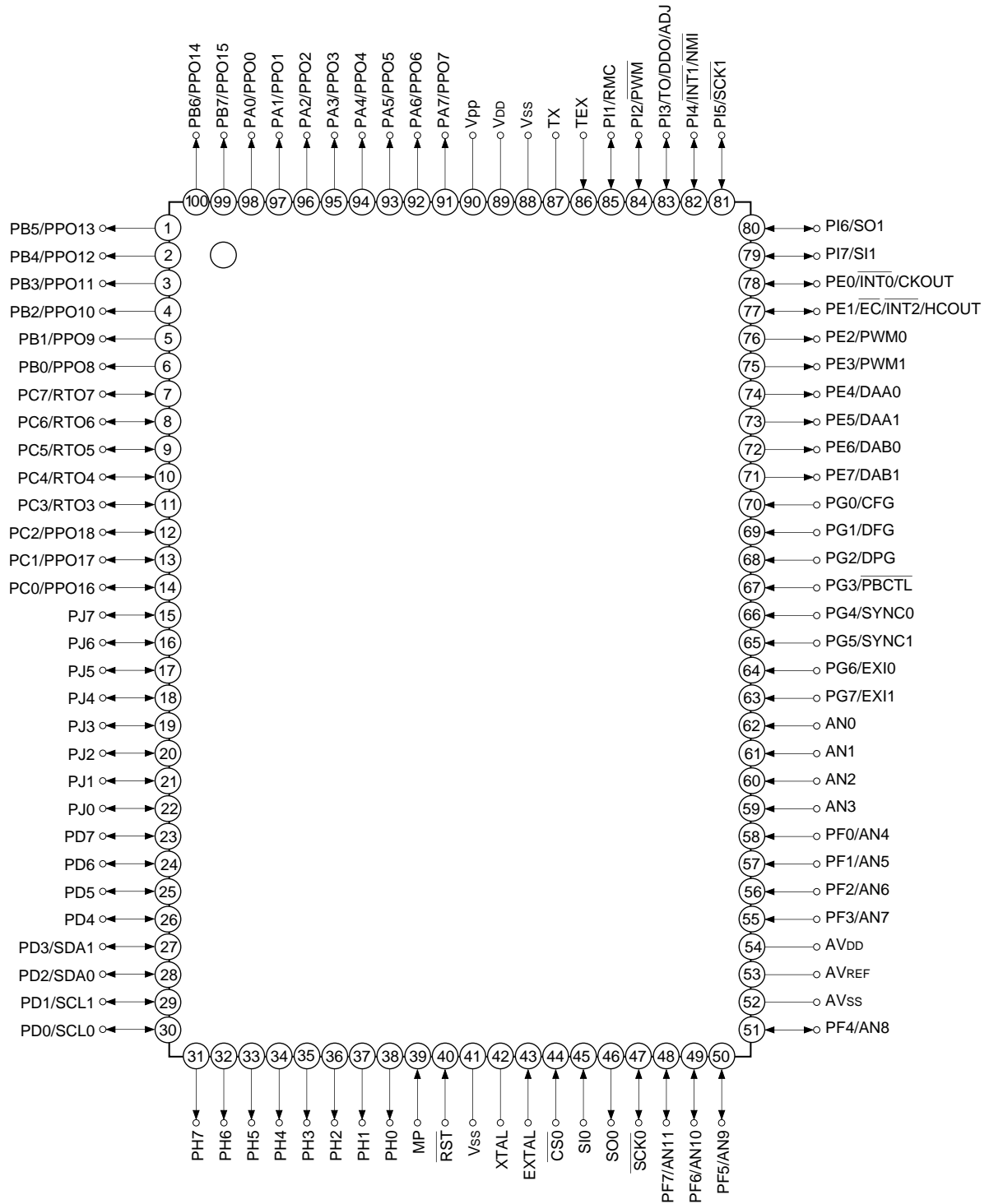




Block Diagram



Pin Assignment (Top View)



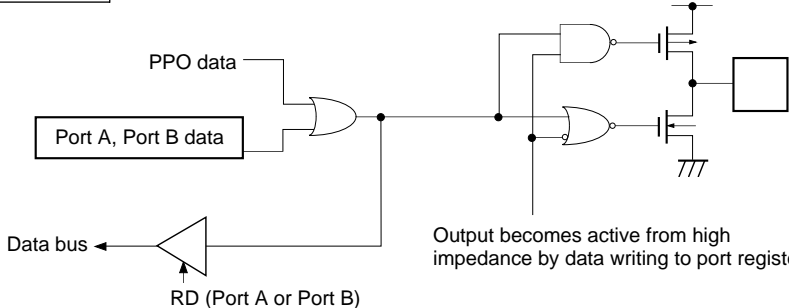
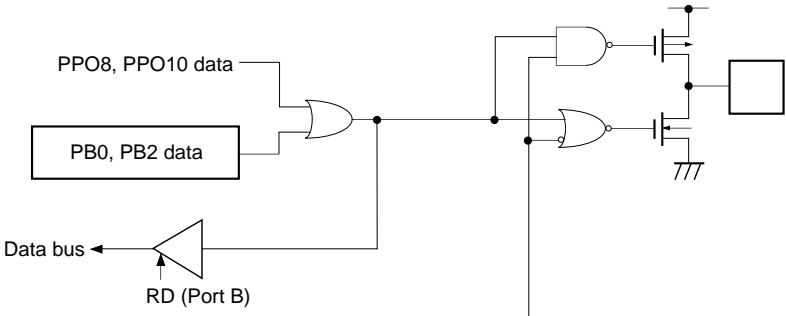
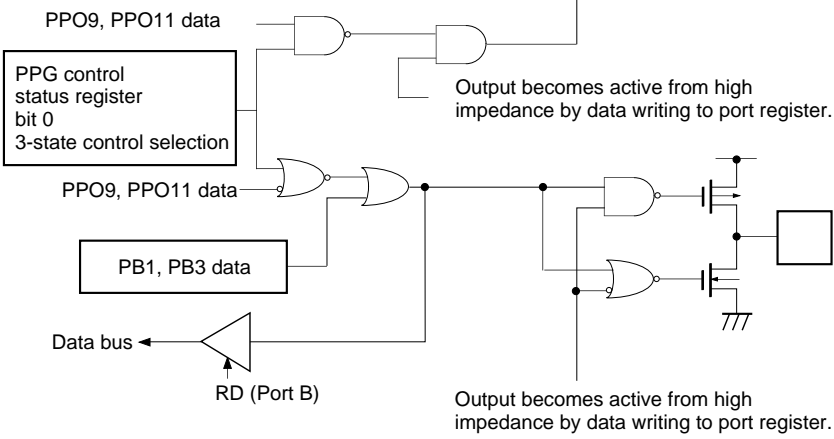
- Note)** 1. Vpp (Pin 90) is always connected to VDD.  
 2. Vss (Pins 41 and 88) are both connected to GND.  
 3. MP (Pin 39) is always connected to GND.

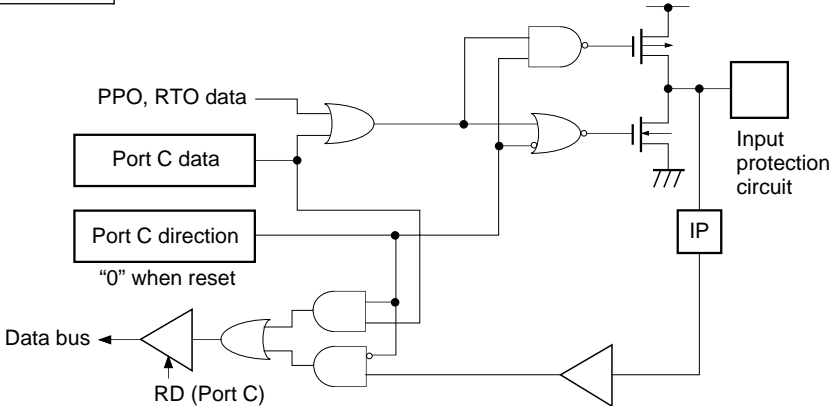
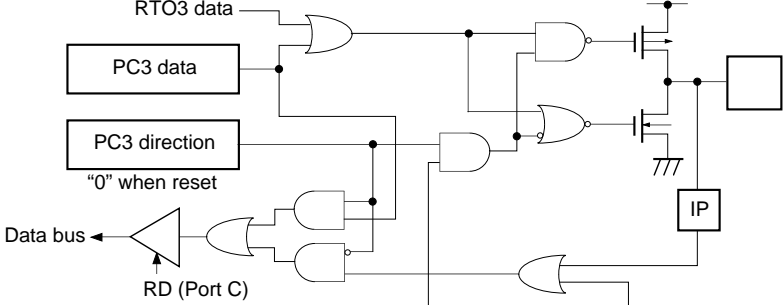
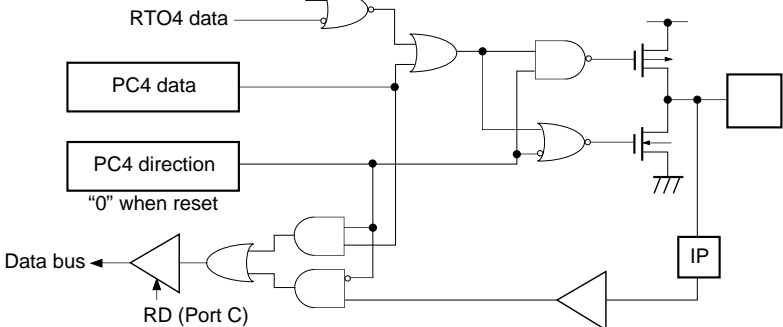
Pin Description

Symbol	I/O	Description			
PA0/PPO0 to PA7/PPO7	Output/ Real-time output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port. PB0 and PB2 can be 3-state controlled with PPG. (19 pins)		
PB0/PPO8 to PB7/PPO15	Output/ Real-time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)			
PC0/PPO16 to PC2/PPO18	I/O/ Real-time output	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)			
PC3/RTO3 to PC7/RTO7	I/O/ Real-time output		Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. PC3 can be 3-state controlled with RTG. (5 pins)		
PD0/SCL0 PD1/SCL1	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits for upper 4 bits. Can drive 12mA sink current. Lower 4-bit output is N-ch open drain. (8 pins)	Serial clock (CH2) I/O. (2 pins)		
PD2/SDA0 PD3/SDA1			Serial data (CH2) I/O. (2 pins)		
PD4 to PD7					
PE0/ $\overline{\text{INT0}}$ / CKOUT	Input/Input/Output	(Port E) 8-bit port. Lower 2 bits are for inputs; upper 6 bits are for outputs. (8 pins)	Input to request external interruption. Active at the falling edge.	System clock frequency dividing output.	
PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$ / HCOUT	Input/Input/Input/ Output		External event input for timer/counter.	Input to request external interruption. Active at the falling edge.	Coincidence signal output of HSYNC counter.
PE2/PWM0	Output/Output		PWM outputs. (2 pins)		
PE3/PWM1	Output/Output				
PE4/DAA0	Output/Output		DA gate pulse outputs. (4 pins)		
PE5/DAA1	Output/Output				
PE6/DAB0	Output/Output				
PE7/DAB1	Output/Output				
AN0 to AN3	Input	Analog input to A/D converter. (12 pins)			
PF0/AN4 to PF3/AN7	Input/Input	(Port F) 8-bit port. Lower 4 bits are for inputs; upper 4 bits are for outputs.			
PF4/AN8 to PF7/AN11	Output/Input	Lower 4 bits also serve as standby release input pin. (8 pins)			
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O.			
SO0	Output	Serial data (CH0) output.			
SI0	Input	Serial data (CH0) input.			
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input.			

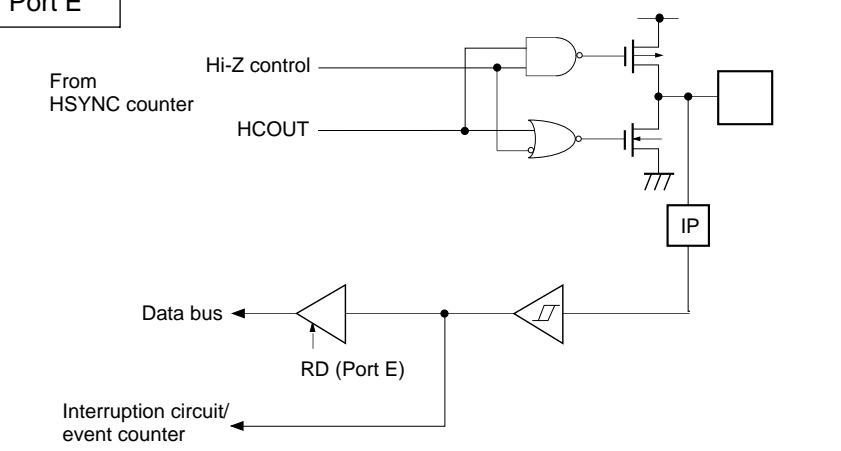
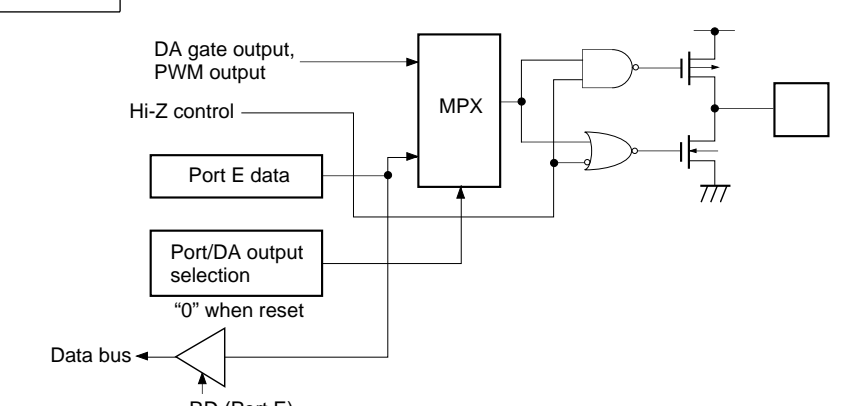
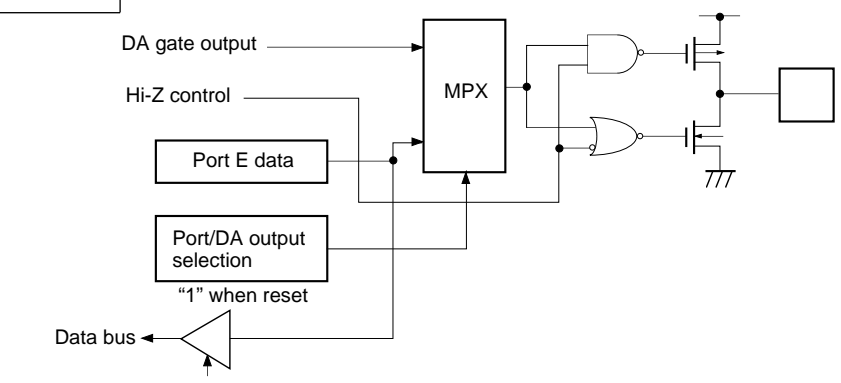
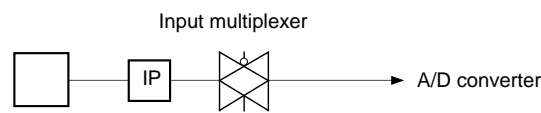
Symbol	I/O	Description	
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input.
PG1/DFG	Input/Input		Drum FG input.
PG2/DPG	Input/Input		Drum PG input.
PG3/ $\overline{\text{PBCTL}}$	Input/Input		Playback CTL pulse input. External event input for timer/counter.
PG4/SYNC0	Input/Input		Composite sync signal input. (2 pins)
PG5/SYNC1	Input/Input		
PG6/EXI0	Input/Input		External input to FRC capture unit. (2 pins)
PG7/EXI1	Input/Input		
PH0 to PH7	Output	(Port H) 8-bit output port ; N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O port can be set in a unit of single bits. (7 pins)	Remote control reception circuit input.
PI2/ $\overline{\text{PWM}}$	I/O/Output		14-bit PWM output.
PI3/TO/ DDO/ADJ	I/O/Output/ Output/Output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output.
PI4/ $\overline{\text{INT1}}$ / NMI	I/O/Input/Input		Input to request external interruption and non-maskable interruption. Active at the falling edge.
PI5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O.
PI6/SO1	I/O/Output		Serial data (CH1) output.
PI7/SI1	I/O/Input		Serial data (CH1) input.
PJ0 to PJ7	I/O		(Port J) 8-bit I/O port. I/O and standby release input function can be set in a unit of single bits.
EXTAL	Input	Connects a crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL and input the opposite phase clock to XTAL.	
XTAL	Output		
TEX	Input	Connects a crystal oscillator for 32kHz timer/counter clock. The 32kHz crystal oscillator is inserted between TEX and TX. When used as event counter, connect the clock source to TEX and leave TX open.	
TX	Output		
$\overline{\text{RST}}$	Input	System reset; active at Low level.	
MP	Input	Test mode input. Always connect to GND.	
AV <sub>DD</sub>		Positive power supply of A/D converter.	
AV <sub>REF</sub>	Input	Reference voltage input of A/D converter.	
AV <sub>SS</sub>		GND of A/D converter.	
V <sub>DD</sub>		Positive power supply. Connect V <sub>DD</sub> pin to V <sub>DD</sub> .	
V <sub>pp</sub>		Positive power supply for incorporated PROM writing. In normal operation, connect to V <sub>DD</sub> .	
V <sub>SS</sub>		GND. Connect both V <sub>SS</sub> pins to GND.	

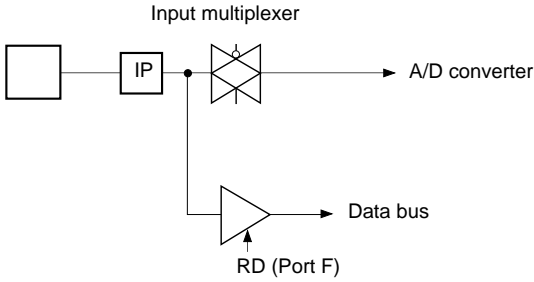
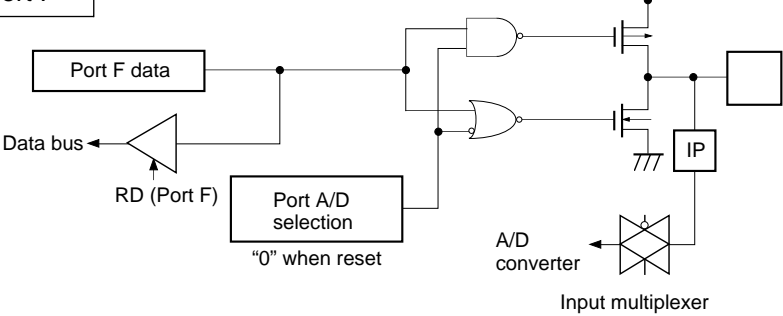
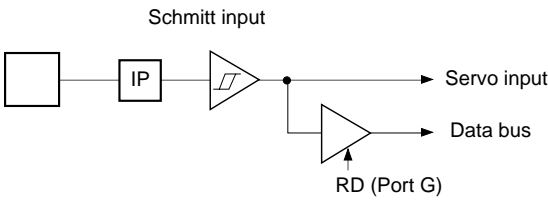
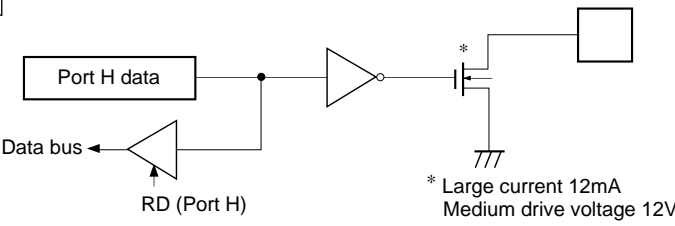
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>Port A Port B</p> <p>PA0 /PPO0 to PA7/PPO7</p> <p>PB4/PPO12 to PB7/PPO15</p> <p>12 pins</p>	 <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>PB0 /PPO8 PB2/PPO10</p> <p>2 pins</p>	 <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>PB1/PPO9 PB3/PPO11</p> <p>2 pins</p>	 <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PC0/PPO16 to PC2/PPO18</p> <p>PC5/RTO5 to PC7/RTO7</p> <p>6 pins</p>	<p>Port C</p> 	<p>Hi-Z</p>
<p>PC3/RTO3</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>PC4/RTO4</p> <p>1 pin</p>	 <p>RTO data is OR-gate data of CH0 and CH1.</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PD0/SCL0 PD1/SCL1 PD2/SDA0 PD3/SDA1</p> <p>4 pins</p>	<p>Port D</p> <p>SCL, SDA Serial interface CH2 output enable Port D data Data bus RD (Port D) SCL, SDA (Serial CH2 circuit) Schmitt input BUS SW To another serial CH2 pin * Large current 12mA</p>	<p>Hi-Z</p>
<p>PD4 to PD7</p> <p>4 pins</p>	<p>Port D</p> <p>Port D data Port D direction "0" when reset Data bus RD (Port D) * Large current 12mA</p>	<p>Hi-Z</p>
<p>PE0/<math>\overline{\text{INT0}}</math>/ CKOUT</p> <p>1 pin</p>	<p>Port E</p> <p>ESL0 Port E selection ESL1 PS1 01 PS2 10 PS3 11 MPX Data bus RD (Port E) Interruption circuit</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE1/<math>\overline{\text{EC}}/\overline{\text{INT2}}</math> /HCOUT</p> <p>1 pin</p>	<p>Port E</p>  <p>From HSYNC counter</p> <p>Hi-Z control</p> <p>HCOUT</p> <p>IP</p> <p>Data bus</p> <p>RD (Port E)</p> <p>Interruption circuit/ event counter</p>	<p>Hi-Z</p>
<p>PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1</p> <p>4 pins</p>	<p>Port E</p>  <p>DA gate output, PWM output</p> <p>Hi-Z control</p> <p>Port E data</p> <p>Port/DA output selection "0" when reset</p> <p>Data bus</p> <p>RD (Port E)</p> <p>MPX</p> <p>IP</p>	<p>Hi-Z</p>
<p>PE6/DAB0 PE7/DAB1</p> <p>2 pins</p>	<p>Port E</p>  <p>DA gate output</p> <p>Hi-Z control</p> <p>Port E data</p> <p>Port/DA output selection "1" when reset</p> <p>Data bus</p> <p>RD (Port E)</p> <p>MPX</p> <p>IP</p>	<p>High level</p>
<p>AN0 to AN3</p> <p>4 pins</p>	<p>Input multiplexer</p>  <p>IP</p> <p>A/D converter</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PF0/AN4 to PF3/AN7</p> <p>4 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PF4/AN8 to PF7/AN11</p> <p>4 pins</p>	<p>Port F</p>  <p>Port A/D selection "0" when reset</p>	<p>Hi-Z</p>
<p>PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1</p> <p>8 pins</p>	<p>Port G</p>  <p>Note) For PG4 and PG5 input format, there is TTL Schmitt input with product.</p>	<p>Hi-Z</p>
<p>PH0 to PH7</p> <p>8 pins</p>	<p>Port H</p>  <p>* Large current 12mA Medium drive voltage 12V</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PI2/<math>\overline{\text{PWM}}</math> PI3/<math>\overline{\text{TO}}</math>/ DDO/<math>\overline{\text{ADJ}}</math></p> <p>2 pins</p>	<p>Port I</p> <p>Port I function selection "0" when reset</p> <p>PI2...14-bit PWM PI3...Timer/counter, CTL duty detection circuit, 32kHz timer</p> <p>Port I data</p> <p>Port I direction "0" when reset</p> <p>Data bus</p> <p>RD (Port I)</p> <p>IP</p>	<p>Hi-Z</p>
<p>PI1/<math>\overline{\text{RMC}}</math> PI4/<math>\overline{\text{INT1/NMI}}</math> PI7/<math>\overline{\text{SI1}}</math></p> <p>3 pins</p>	<p>Port I</p> <p>Port I data</p> <p>Port I direction "0" when reset</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Schmitt input</p> <p>IP</p> <p>PI1...Remote control circuit PI4...Interruption circuit PI7...Serial interface CH1</p>	<p>Hi-Z</p>
<p>PI5/<math>\overline{\text{SCK1}}</math> PI6/<math>\overline{\text{SO1}}</math></p> <p>2 pins</p>	<p>Port I</p> <p>Port I function selection</p> <p>Serial interface CH1</p> <p>Port I data</p> <p>Port I direction "0" when reset</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>MPX</p> <p>IP</p> <p>Serial interface CH1</p> <p>PI6 is not Schmitt input.</p>	<p>Hi-Z</p>
<p>PJ0 to PJ7</p> <p>8 pins</p>	<p>Port J</p> <p>Port J data</p> <p>Port J direction "0" when reset</p> <p>Data bus</p> <p>RD (Port J)</p> <p>Edge detection</p> <p>Standby release</p> <p>Data bus</p> <p>RD (Port J direction)</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
$\overline{\text{CS0}}$ $\text{SI0}$ 2 pins	<p>Schmitt input</p>	Hi-Z
$\text{SO0}$ 1 pin		Hi-Z
$\overline{\text{SCK0}}$ 1 pin		Hi-Z
$\text{EXTAL}$ $\text{XTAL}$ 2 pins	<ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop mode.</li> </ul>	Oscillation
$\text{TEX}$ $\text{TX}$ 2 pins	<ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs Low level and TX pin outputs High level.</li> </ul>	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	V <sub>pp</sub>	-0.3 to +13	V	Incorporated PROM
	AV <sub>DD</sub>	AV <sub>SS</sub> to +7.0* <sup>1</sup>	V	
	AV <sub>SS</sub>	-0.3 to +0.3	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>2</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>2</sup>	V	
Medium drive output voltage	V <sub>OUTP</sub>	-0.3 to +15.0	V	Port H pin
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	∑I <sub>OH</sub>	-50	mA	Total of output pins
Low level output current	I <sub>OL</sub>	15	mA	Ports excluding large current output (value per pin)
	I <sub>OLC</sub>	20	mA	Large current output port (value per pin* <sup>3</sup> )
Low level total output current	∑I <sub>OL</sub>	130	mA	Total of output pins
Operating temperature	T <sub>opr</sub>	-10 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	600	mW	QFP

\*1 AV<sub>DD</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*2 V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*3 The large current drive transistors are the N-CH transistors of the Port D (PD) and Port H (PH).

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing modes
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing mode or during sleep mode
		2.7	5.5	V	Guaranteed operation range by TEX clock
		2.0	5.5	V	Guaranteed data hold range during stop mode
Analog supply voltage	AV <sub>DD</sub>	4.5	5.5	V	*1
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	Includes the serial CH2 input*2
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	CMOS Schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pin
			5.5	V	CMOS Schmitt input*7
	V <sub>IHTS</sub>	2.2	5.5	V	TTL Schmitt input*4
V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin*5 and TEX pin*6	
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	Includes the serial CH2 input*2
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	CMOS Schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pin
	V <sub>ILTS</sub>	0	0.8	V	TTL Schmitt input*4
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*5 and TEX pin*6
Operating temperature	Topr	-10	+75	°C	

\*1 AV<sub>DD</sub> and V<sub>DD</sub> should be set to the same voltage.

\*2 Normal input port (PC, PD4 to PD7, PF0 to PF3, PG, PI and PJ), MP pin

\*3  $\overline{\text{SCK0}}$ ,  $\overline{\text{RST}}$ ,  $\overline{\text{EC/INT2}}$ , RMC,  $\overline{\text{INT1/NMI}}$ ,  $\overline{\text{SCK1}}$  and SI1

\*4 PG4 and PG5 (When TTL Schmitt input is selected for the product)

\*5 Specifies only when the external clock is input.

\*6 Specifies only when the external event count clock is input.

\*7  $\overline{\text{CS0}}$ , SI0, and PG (For PG4 and PG5, when CMOS Schmitt input is selected for the product.)

## Electrical Characteristics

DC Characteristics ( $V_{DD} = 4.5$  to  $5.5V$ )( $T_a = -10$  to  $+75^\circ C$ ,  $V_{SS} = 0V$  reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	$V_{OH}$	PA to PC, PD4 to PD7, PE2 to PE7, PF4 to PF7, PH ( $V_{OL}$ only) PI1 to PI7	$V_{DD} = 4.5V$ , $I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V$ , $I_{OH} = -1.2mA$	3.5			V
Low level output voltage	$V_{OL}$	PJ, SO0, SCK0	$V_{DD} = 4.5V$ , $I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V$ , $I_{OL} = 3.6mA$			0.6	V
		PD, PH	$V_{DD} = 4.5V$ , $I_{OL} = 12.0mA$			1.5	V
		PD0 to PD3 (SCL0, SCL1 SDA0, SDA1)	$V_{DD} = 4.5V$ , $I_{OL} = 3.0mA$			0.4	V
			$V_{DD} = 4.5V$ , $I_{OL} = 6.0mA$			0.6	V
Input current	$I_{IHE}$	EXTAL	$V_{DD} = 5.5V$ , $V_{IH} = 5.5V$	0.5		40	$\mu A$
	$I_{ILE}$		$V_{DD} = 5.5V$ , $V_{IL} = 0.4V$	-0.5		-40	$\mu A$
	$I_{IHT}$	TEX	$V_{DD} = 5.5V$ , $V_{IH} = 5.5V$	0.1		10	$\mu A$
	$I_{ILT}$		$V_{DD} = 5.5V$ , $V_{IL} = 0.4V$	-0.1		-10	$\mu A$
	$I_{ILR}$		$\overline{RST}$	$V_{DD} = 5.5V$ , $V_{IL} = 0.4V$	-1.5		-400
I/O leakage current	$I_{IZ}$	PA to PG, PI, PJ, MP AN0 to AN3, $\overline{CS0}$ , SI0, SO0 SCK0	$V_{DD} = 5.5V$ , $V_I = 0, 5.5V$			$\pm 10$	$\mu A$
Open drain output leakage current (in N-CH Tr off state)	$I_{LOH}$	PH	$V_{DD} = 5.5V$ , $V_{OH} = 12V$			50	$\mu A$
		PD0 to PD3	$V_{DD} = 5.5V$ , $V_{OH} = 5.5V$			10	$\mu A$
Serial interface CH2 bus switch connection impedance (in output Tr off state)	RBS	SCL0: SCL1 SDA0: SDA1	$V_{DD} = 4.5V$ $V_{SCL0} = V_{SCL1} = 2.25V$ $V_{SDA0} = V_{SDA1} = 2.25V$			120	$\Omega$

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*1	I <sub>DD1</sub>	V <sub>DD</sub>	High-speed mode (1/2 frequency dividing clock) operation		31	50	mA
			V <sub>DD</sub> = 5V ± 0.5V				
	I <sub>DDS1</sub>		Sleep mode		2.3	8	mA
			V <sub>DD</sub> = 5V ± 0.5V				
	I <sub>DD2</sub>		32kHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 47pF)		44	110	μA
			V <sub>DD</sub> = 3V ± 0.3V				
I <sub>DDS2</sub>	Sleep mode		9	35	μA		
	V <sub>DD</sub> = 3V ± 0.3V						
I <sub>DDS3</sub>	Stop mode (EXTAL and TEX pins oscillation stop)			30	μA		
	V <sub>DD</sub> = 5V ± 0.5V						
Input capacity	C <sub>IN</sub>	PC, PD, PE0, PE1, PF, PG, PI1 to PI7 PJ, $\overline{CS0}$ , SI0, $\overline{SCK0}$ , AN0 to AN3, EXTAL, XTAL, TEX, TX, MP, $\overline{RST}$	Clock 1MHz 0V other than the measured pins		10	20	pF

\*1 When all output pins are open.

AC Characteristics

(1) Clock timing

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t <sub>XL</sub> , t <sub>XH</sub>	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)	28			ns
System clock input rise and fall times	t <sub>CR</sub> , t <sub>CF</sub>	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)			200	ns
Event count clock input pulse width	t <sub>EH</sub> , t <sub>EL</sub>	$\overline{EC}$	Fig. 3	4t <sub>sys</sub> *1			ns
Event count clock input rise and fall times	t <sub>ER</sub> , t <sub>EF</sub>	$\overline{EC}$	Fig. 3			20	ns
System clock frequency	fc	TEX TX	Fig. 2 V <sub>DD</sub> = 2.7 to 5.5V (32kHz clock applied condition)		32.768		kHz
Event count clock input pulse width	t <sub>TL</sub> , t <sub>TH</sub>	TEX	Fig. 3	10			μs
Event count clock input rise and fall times	t <sub>TR</sub> , t <sub>TF</sub>	TEX	Fig. 3			20	ms

\*1 t<sub>sys</sub> indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

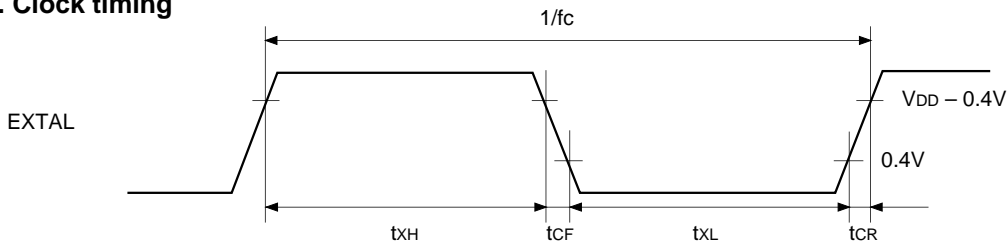


Fig. 2. Clock applied condition

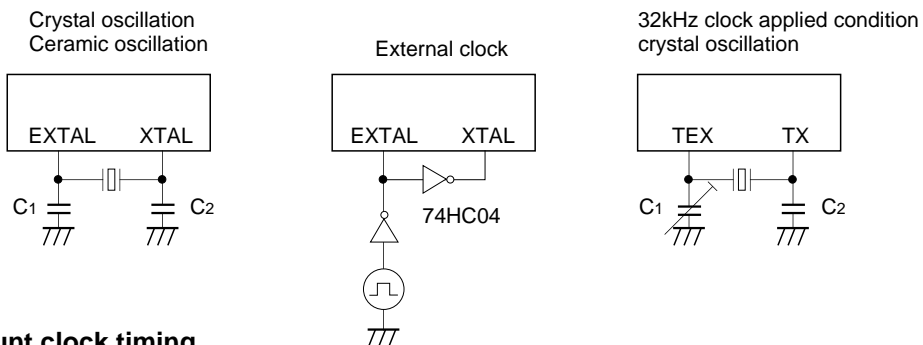
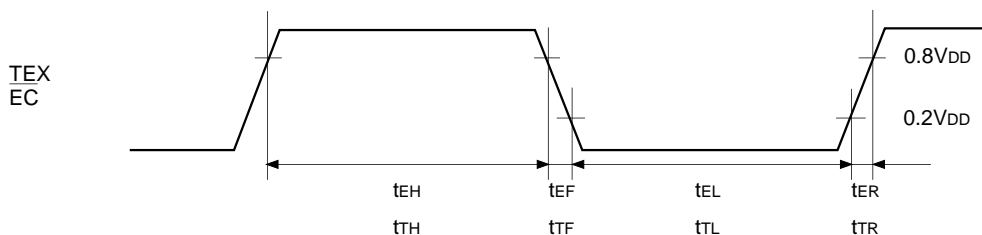


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

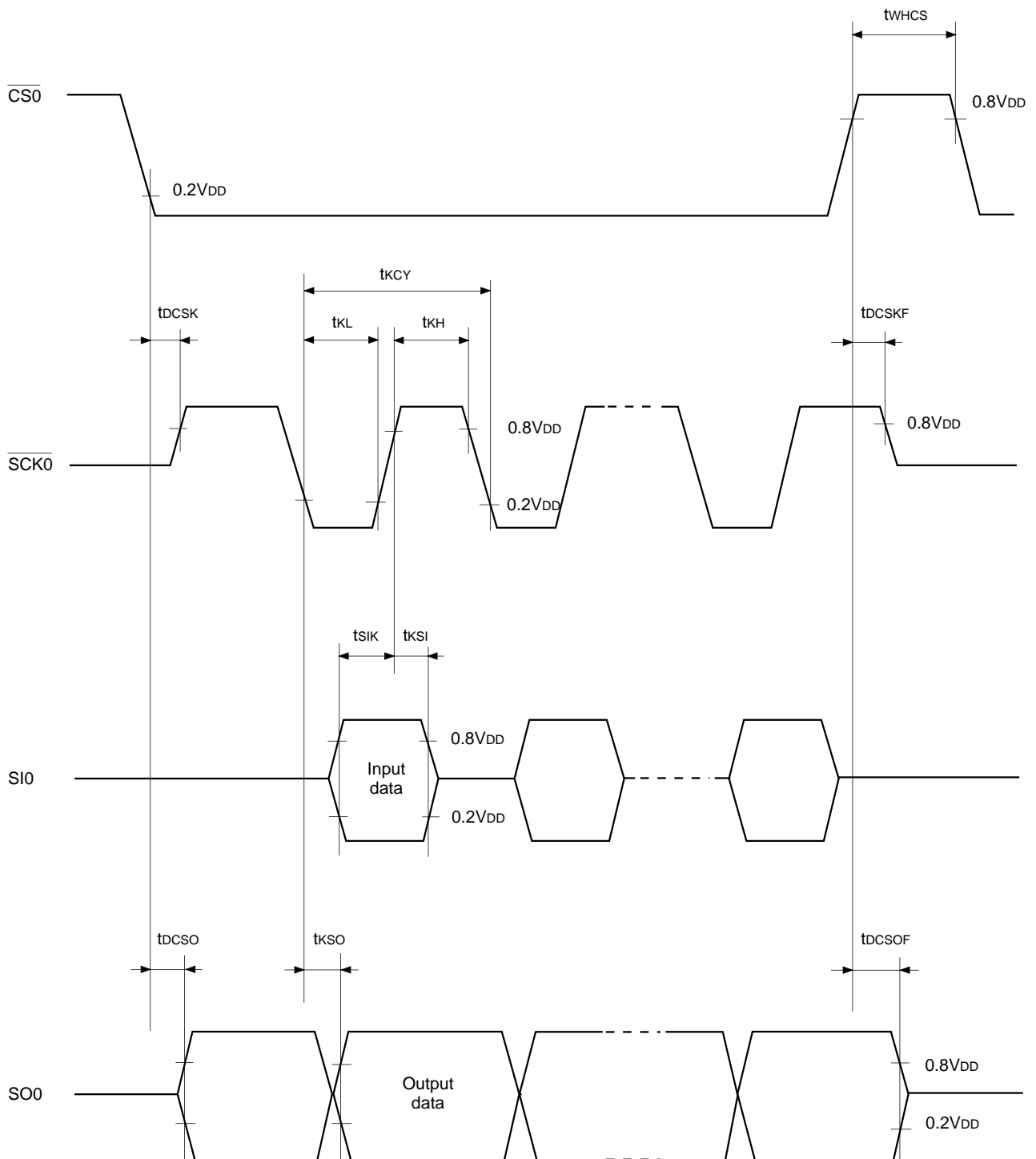
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t <sub>DCSK</sub>	$\overline{SCK0}$	Chip select transfer mode (SCK = output mode)		t <sub>sys</sub> + 200	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t <sub>DCSKF</sub>	$\overline{SCK0}$	Chip select transfer mode (SCK = output mode)		t <sub>sys</sub> + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t <sub>DCSO</sub>	SO0	Chip select transfer mode		t <sub>sys</sub> + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	t <sub>DCSOF</sub>	SO0	Chip select transfer mode		t <sub>sys</sub> + 200	ns
$\overline{CS}$ High level width	t <sub>WHCS</sub>	$\overline{CS0}$	Chip select transfer mode	t <sub>sys</sub> + 200		ns
$\overline{SCK}$ cycle time	t <sub>KCY</sub>	$\overline{SCK0}$	Input mode	2t <sub>sys</sub> + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ High and Low level widths	t <sub>KH</sub> t <sub>KL</sub>	$\overline{SCK0}$	Input mode	t <sub>sys</sub> + 100		ns
			Output mode	8000/fc - 100		ns
SI input setup time (for $\overline{SCK} \uparrow$ )	t <sub>SIK</sub>	SI0	$\overline{SCK}$ input mode	-t <sub>sys</sub> + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$ )	t <sub>KSI</sub>	SI0	$\overline{SCK}$ input mode	2t <sub>sys</sub> + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t <sub>KSO</sub>	SO0	$\overline{SCK}$ input mode		2t <sub>sys</sub> + 200	ns
			$\overline{SCK}$ output mode		100	ns

**Note 1)** t<sub>sys</sub> indicates three values according to the contents of the clock control register (CLC: 00FEH) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

**Note 2)** The load of  $\overline{SCK}$  output mode and SO output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing (CH0)



**Serial transfer (CH1) (SIO mode)**

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

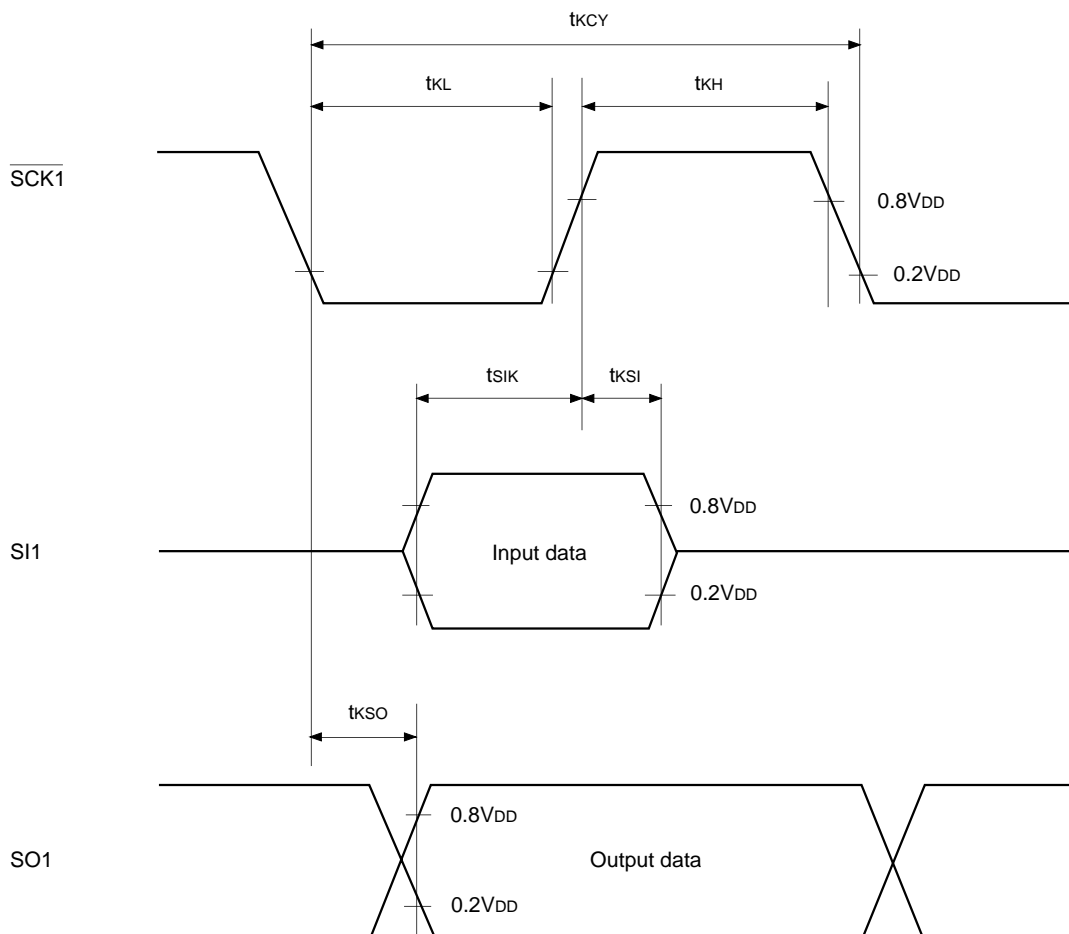
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ High and Low level widths	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 100$		ns
SI1 input setup time (for $\overline{\text{SCK1}} \uparrow$ )	$t_{\text{SIK}}$	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$ )	$t_{\text{KSI}}$	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	$t_{\text{KSO}}$	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

**Note 1)**  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (CLC: 00FE<sub>H</sub>) upper 2 bits (CPU clock selection).

$t_{\text{sys}}$  [ns] =  $2000/f_c$  (Upper 2 bits = "00"),  $4000/f_c$  (Upper 2 bits = "01"),  $16000/f_c$  (Upper 2 bits = "11")

**Note 2)** The load of  $\overline{\text{SCK1}}$  output mode and SO1 output delay time is  $50\text{pF} + 1\text{TTL}$ .

**Fig. 5. Serial transfer CH1 timing (SIO mode)**



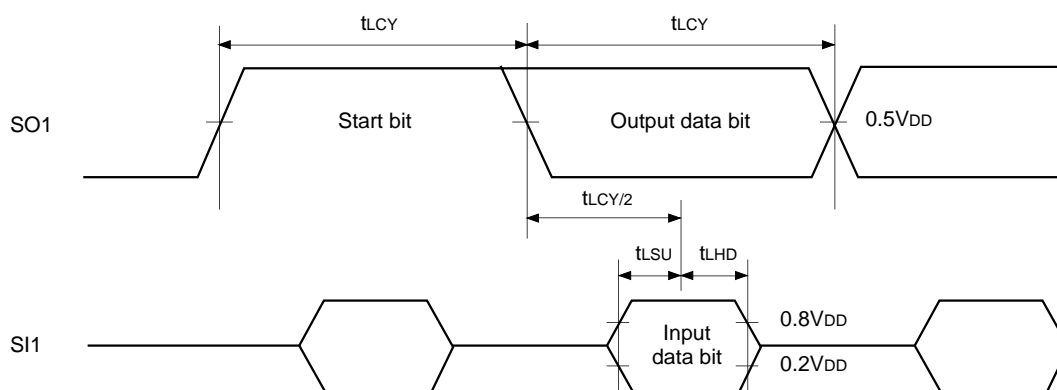
**Serial transfer (CH1) (Special mode)** ( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	$t_{LCY}$	SO1 SI1	*1		104		$\mu\text{s}$
SI1 data setup time	$t_{LSU}$	SI1		2			$\mu\text{s}$
SI1 data hold time	$t_{LHD}$	SI1		2			$\mu\text{s}$

\*1  $t_{LCY}$  is specified only when serial mode register (CH1) (SIOM1: 05FZH) lower 2 bits (SO1 clock selection) has been set at 104 $\mu\text{s}$ .

**Note)** The load of SO1 pin is 50pF + 1TTL.

**Fig. 6. Serial transfer CH1 timing (Special mode)**



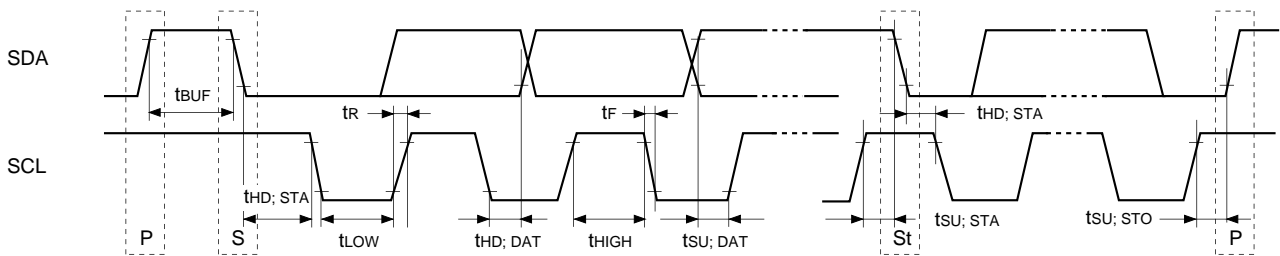
**Serial transfer (CH2)**

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

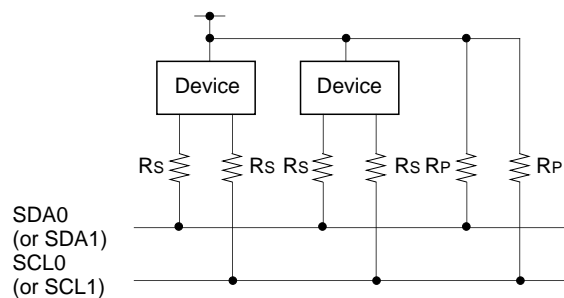
Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f <sub>SCL</sub>	SCL			400	kHz
Bus-free time before starting transfer	t <sub>BUF</sub>	SDA, SCL		2.6		μs
Hold time for starting transfer	t <sub>HD; STA</sub>	SDA, SCL		1.0		μs
Clock Low level width	t <sub>LOW</sub>	SCL		1.0		μs
Clock High level width	t <sub>HIGH</sub>	SCL		1.0		μs
Setup time for repeated transfers	t <sub>SU; STA</sub>	SDA, SCL		1.0		μs
Data hold time	t <sub>HD; DAT</sub>	SDA, SCL		0*1		μs
Data setup time	t <sub>SU; DAT</sub>	SDA, SCL		100		ns
SDA, SCL rise time	t <sub>R</sub>	SDA, SCL			300	ns
SDA, SCL fall time	t <sub>F</sub>	SDA, SCL			300	ns
Setup time for transfer completion	t <sub>SU; STO</sub>	SDA, SCL		1.6		μs

\*1 The SCL fall time (300ns Max.) is not included in the data hold time.

**Fig. 7. Serial transfer timing (CH2)**



**Fig. 8. Device recommended circuit**



- A pull-up resistor (R<sub>P</sub>) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (R<sub>s</sub> = 300Ω or less) can be used to reduce the spike noise caused by CRT flashover.

(3) HSYNC counter

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

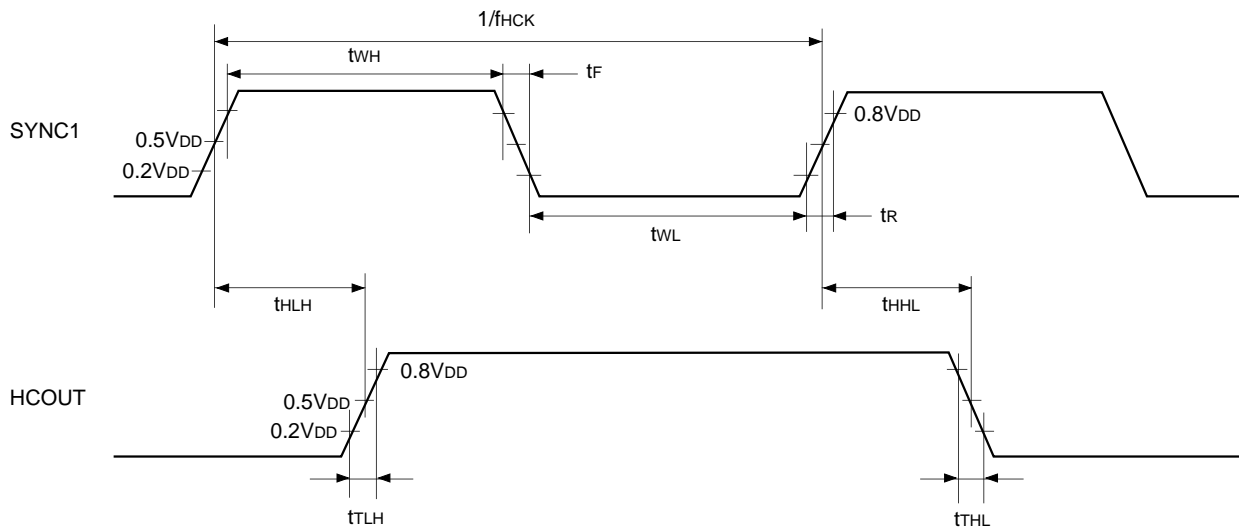
Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	$f_{HCK}$	SYNC1				12	MHz
External clock input pulse width	$t_{WH}, t_{WL}$	SYNC1		33			ns
External clock input rise and fall times	$t_R, t_F$	SYNC1				200	ns
HCOUT output delay time (for SYNC1 $\uparrow$ )	$t_{HLH}, t_{HHL}$	HCOUT	External clock input SYNC1 $t_R = t_F = 6\text{ns}$			$t_{sys} + 220$	ns
HCOUT output rise and fall times	$t_{TLH}$	HCOUT	External clock input SYNC1 $t_R = t_F = 6\text{ns}$			50	ns
	$t_{THL}$					25	ns

**Note1)**  $t_{sys}$  indicates three values according to the contents of the clock control register (CLC: 00FE<sub>H</sub>) upper 2 bits (CPU clock selection).

$t_{sys} [\text{ns}] = 2000/f_c$  (Upper 2 bits = "00"),  $4000/f_c$  (Upper 2 bits = "01"),  $16000/f_c$  (Upper 2 bits = "11").

**Note2)** The load of HCOUT pin is 50pF.

Fig. 9. HSYNC counter timing

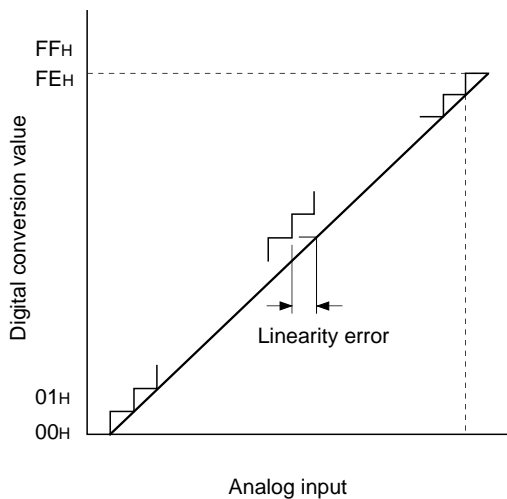


**(4) A/D converter characteristics**

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 4.5$  to  $5.5\text{V}$ ,  $AV_{REF} = 4.0$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$  reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			$\pm 1$	LSB
Absolute error						$\pm 2$	LSB
Conversion time	$t_{CONV}$			$160/f_{ADC}^{*1}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$12/f_{ADC}^{*1}$			$\mu\text{s}$
Reference input voltage	$V_{REF}$	$AV_{REF}$		$AV_{DD} - 0.5$		$AV_{DD}$	V
Analog input voltage	$V_{IAN}$	AN0 to AN11		0		$AV_{REF}$	V
AVREF current	$I_{REF}$	$AV_{REF}$	Operating mode		0.6	1.0	mA
	$I_{REFS}$		Sleep mode Stop mode 32kHz operating mode			10	$\mu\text{A}$

**Fig. 10. Definitions of A/D converter terms**



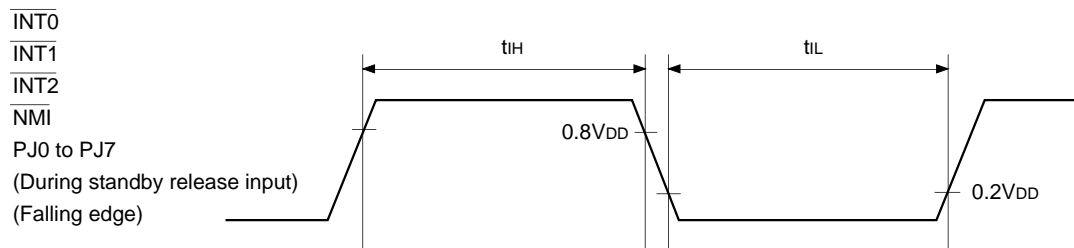
\*1  $f_{ADC}$  indicates the below values due to the ADC operation clock selection (PCC: 05F8H) bit 3 and clock control register (CLC: 00FEH) upper 2 bits.

CLC upper 2 bits	PCC bit 3	
	0 ( $\phi/2$ selection)	1 ( $\phi$ selection)
00 ( $\phi = f_{EX}/2$ )	$f_{ADC} = f_c/2$	$f_{ADC} = f_c$
01 ( $\phi = f_{EX}/4$ )	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ( $\phi = f_{EX}/16$ )	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

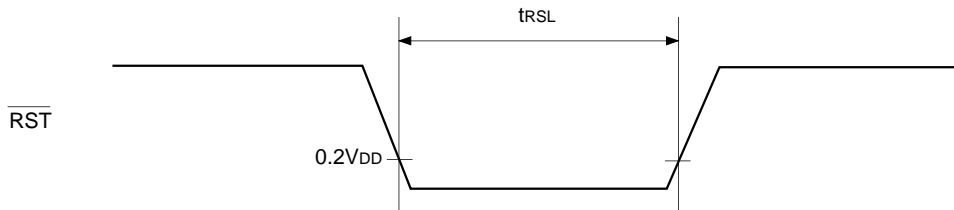
**(5) Interruption, reset input** (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High and Low level widths	t <sub>IH</sub> t <sub>IL</sub>	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ NMI PJ0 to PJ7		1		μs
Reset input Low level width	t <sub>RSL</sub>	$\overline{\text{RST}}$		32/fc		μs

**Fig. 11. Interruption input timing**



**Fig. 12. Reset input timing**



**(6) Others**

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

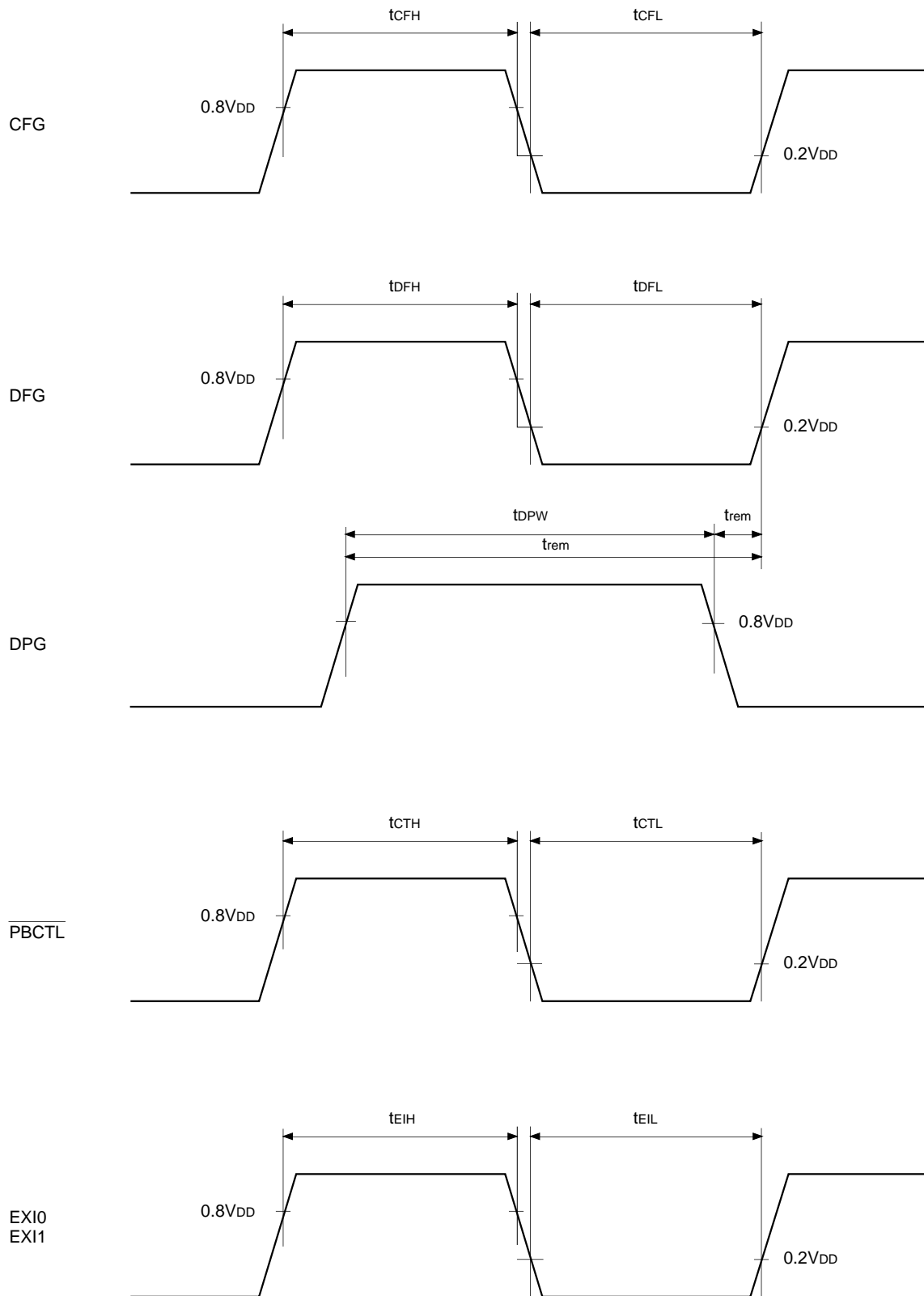
Item	Symbol	Pins	Conditions	Min.	Max.	Unit
CFG input High and Low level widths	t <sub>CFH</sub> t <sub> CFL</sub>	CFG		24t <sub>FRC</sub> + 200		ns
DFG input High and Low level widths	t <sub>DFH</sub> t <sub> DFL</sub>	DFG		16t <sub>FRC</sub> + 200		ns
DPG minimum pulse width	t <sub>DPW</sub>	DPG		8t <sub>FRC</sub> + 200		ns
DPG minimum removal time	t <sub>rem</sub>	DPG		16t <sub>FRC</sub> + 200		ns
PBCTL input High and Low level widths	t <sub>CTH</sub> t <sub> CTL</sub>	$\overline{\text{PBCTL}}$	t <sub>sys</sub> = 2000/fc	8t <sub>FRC</sub> + 200 + t <sub>sys</sub>		ns
EXI input High and Low level widths	t <sub>EIH</sub> t <sub> EIL</sub>	EXI0 EXI1	t <sub>sys</sub> = 2000/fc	8t <sub>FRC</sub> + 200 + t <sub>sys</sub>		ns

**Note 1)** t<sub>FRC</sub> = 1000/fc [ns]

**Note 2)** t<sub>sys</sub> indicates three values according to the contents of the clock control register (CLC: 00FEH) upper 2 bits (CPU clock selection).

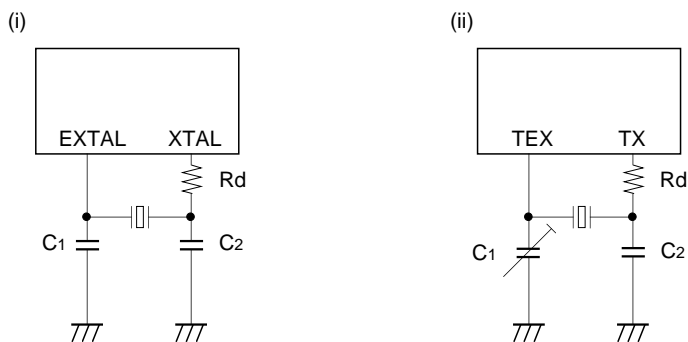
t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 13. Other timings



Supplement

Fig. 14. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C <sub>1</sub> (pF)	C <sub>2</sub> (pF)	R <sub>d</sub> (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

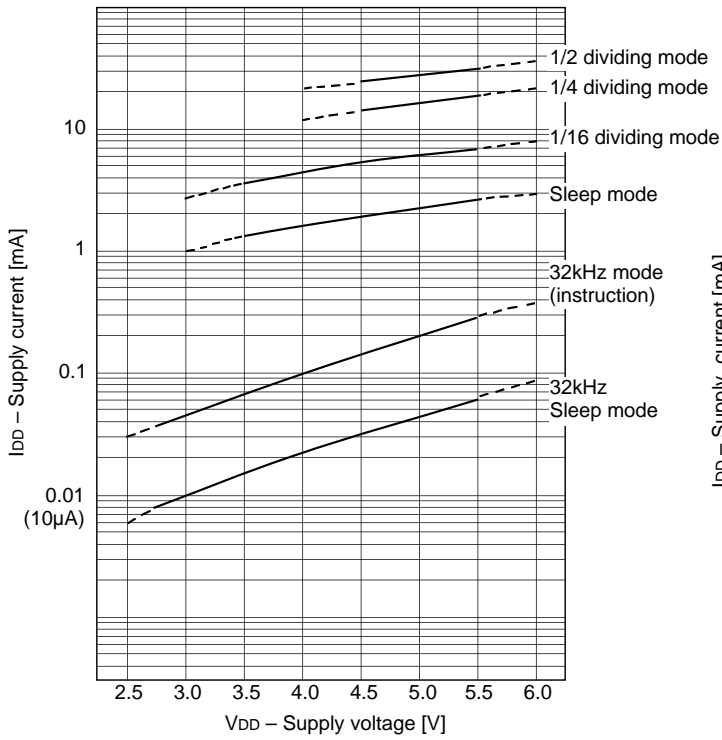
Selection Guide

Option item	Mask product	CXP878P60Q-1- <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>
Package	100-pin plastic QFP	100-pin plastic QFP
ROM capacitance	52K bytes /60K bytes	PROM 60K bytes
Reset pin pull-up resistor	Existent /Non-existent	Existent
Input circuit format*1	CMOS Schmitt /TTL Schmitt	TTL Schmitt

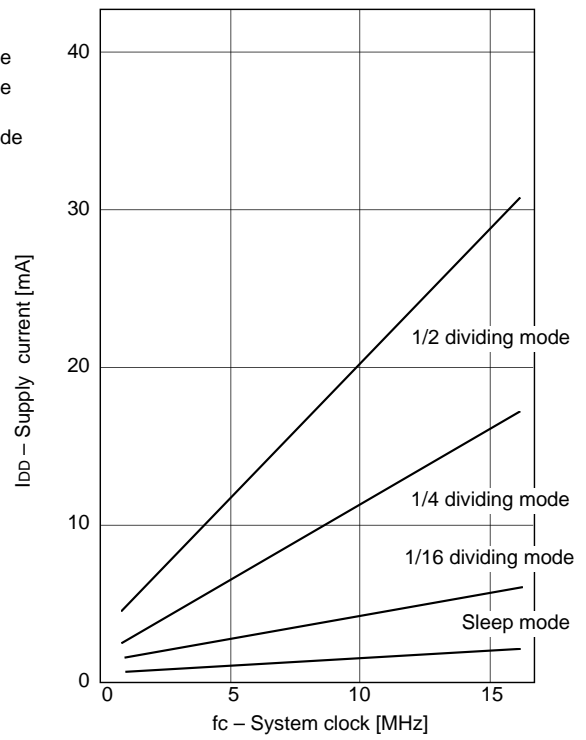
\*1 Pins PG4/SYNC0, PG5/SYNC1 only.

Characteristics Curve

**I<sub>DD</sub> vs. V<sub>DD</sub>**  
(f<sub>c</sub> = 16MHz, T<sub>a</sub> = 25°C, Typical)



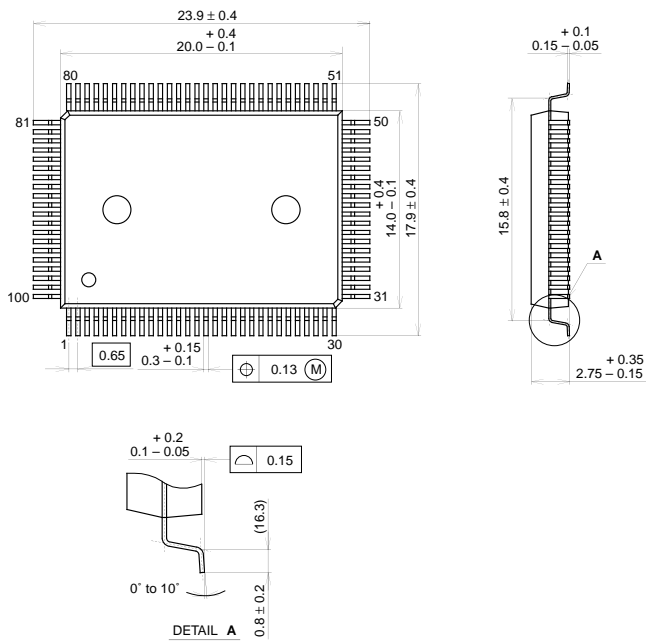
**I<sub>DD</sub> vs. f<sub>c</sub>**  
(V<sub>DD</sub> = 5.0V, T<sub>a</sub> = 25°C, Typical)



Package Outline

Unit: mm

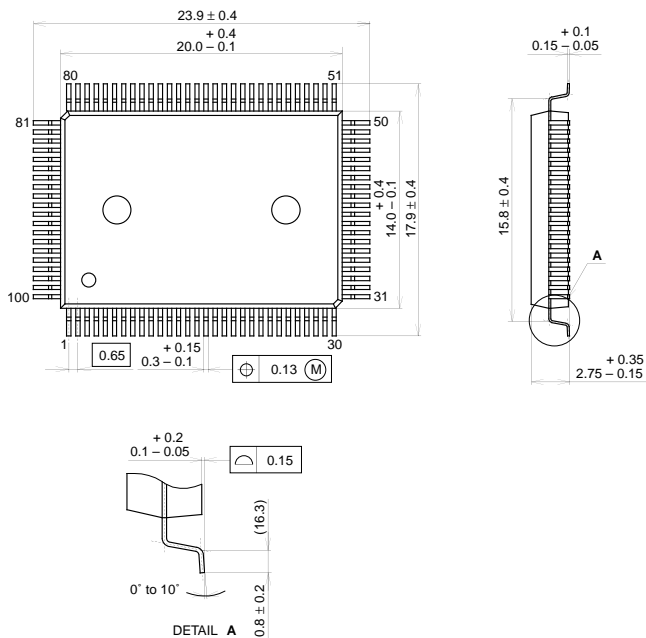
100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01	PACKAGE MATERIAL	EPOXY RESIN
EIAJ CODE	QFP100-P-1420	LEAD TREATMENT	SOLDER PLATING
JEDEC CODE		LEAD MATERIAL	42/COPPER ALLOY
		PACKAGE MASS	1.7g

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01	PACKAGE MATERIAL	EPOXY RESIN
EIAJ CODE	QFP100-P-1420	LEAD TREATMENT	SOLDER PLATING
JEDEC CODE		LEAD MATERIAL	42/COPPER ALLOY
		PACKAGE MASS	1.7g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18 $\mu$ m



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