

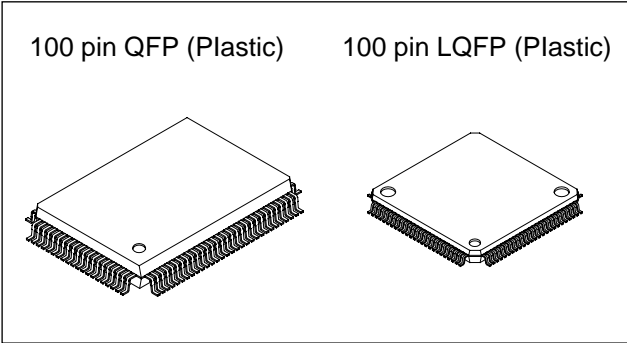
CXP87740A/87748A

CMOS 8-bit Single Chip Microcomputer

Description

The CXP87740A/87748A is a CMOS 8-bit micro-computer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, PWM for tuner, VISS/VASS circuit, 32kHz timer/event counter, remote control receiving circuit, VCR vertical sync separation circuit and the measuring circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also CXP87740A/87748A provides sleep/stop function which enables to lower power consumption and ultra-low speed instruction mode in 32kHz operation.



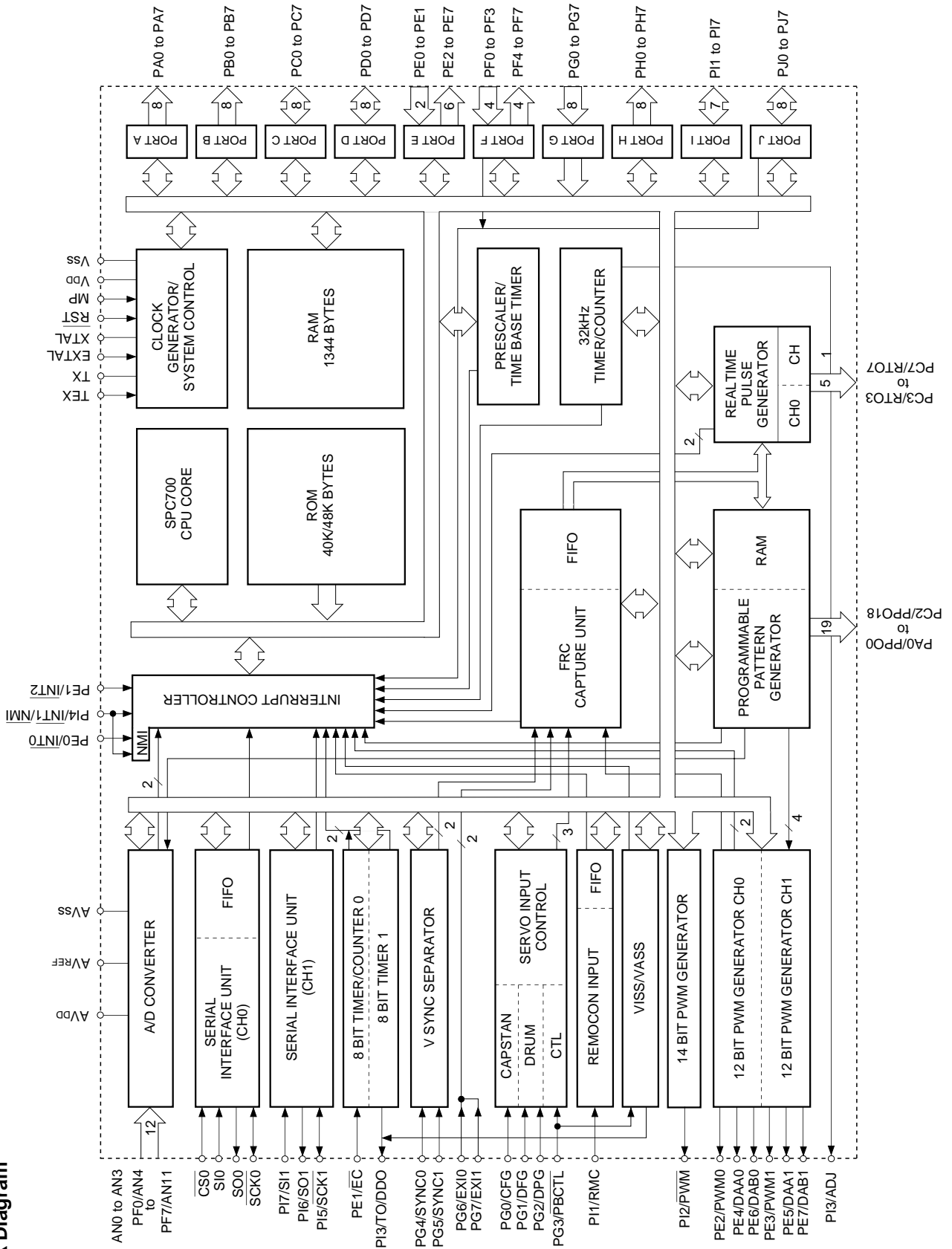
Structure

Silicon gate CMOS IC

Features

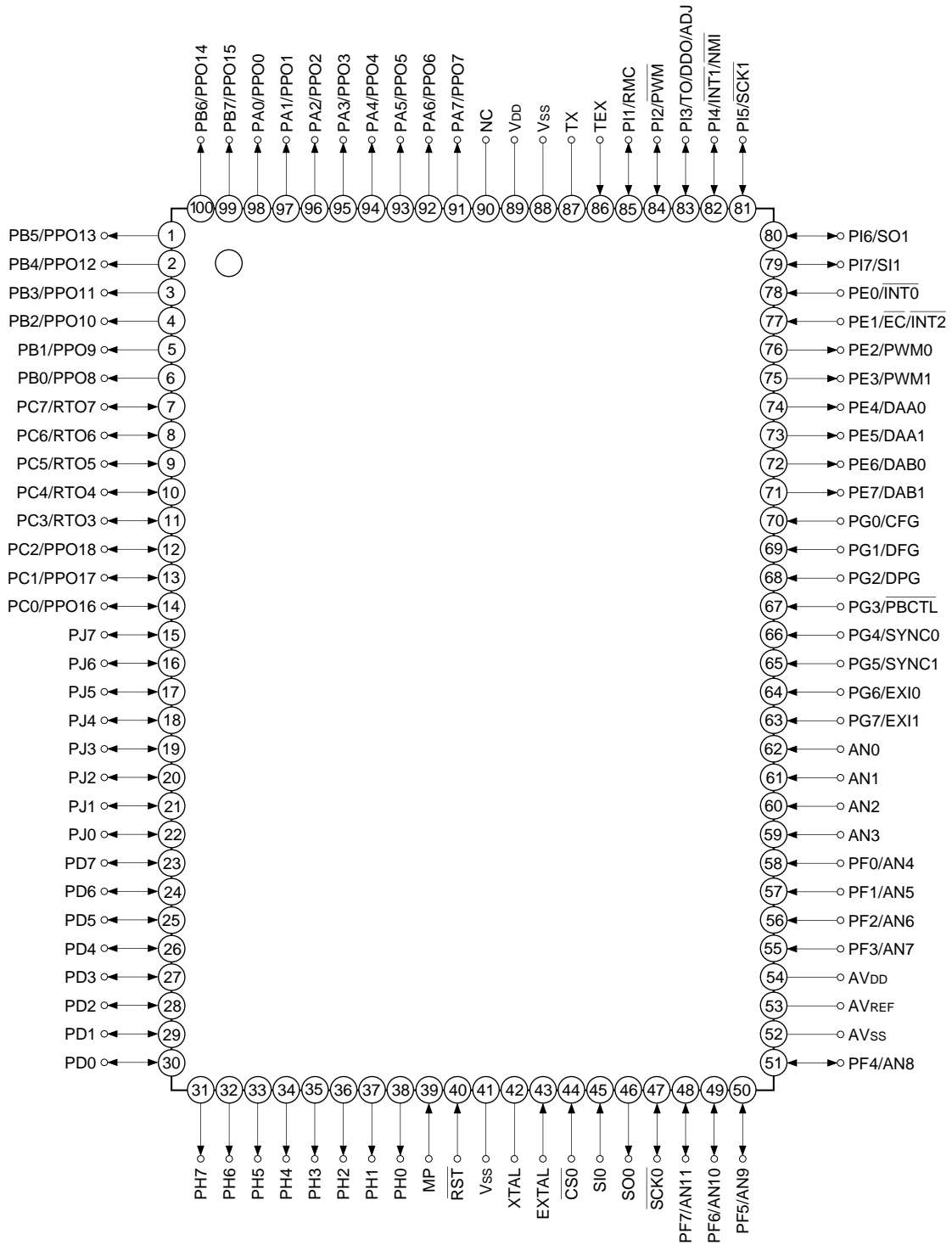
- A wide instruction set (213 instructions) which cover various types of data
 - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle
 - During operation 333ns/12MHz (Supply voltage 3.0 to 5.5V)
 - During operation 250ns/16MHz (Supply voltage 4.5 to 5.5V)
 - During operation 122µs/32kHz
- Incorporated ROM capacity
 - 40K bytes (CXP87740A)
 - 48K bytes (CXP87748A)
- Incorporated RAM capacity
 - 1344 bytes
- Peripheral functions
 - A/D converter
 - 8-bit, 12-channel, successive approximation system (Conversion time 20.0µs/16MHz)
 - Serial interface
 - Incorporated 8-bit and 8-stage FIFO, 1-channel (1 to 8 bytes auto transfer)
 - 8-bit serial I/O, 1-channel
 - Timer
 - 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 32kHz timer/counter
 - High precision timing pattern generator
 - PPG 19 pins 32-stage programmable
 - RTG 5-pins 2-channel
 - PWM/DA gate output
 - 12-bit, 2-channel (Repetitive frequency 62kHz/16MHz)
 - Servo input control
 - Capstan FG, Drum FG/PG, CTL input
 - VSYNC separator
 - Incorporated 26-bit and 8-stage FIFO
 - FRC capture unit
 - 14-bit, 1-channel
 - PWM output
 - Pulse duty auto detection circuit
 - VISS/VASS circuit
 - 8-bit pulse measuring counter, 6-stage FIFO
 - Remote control receiving circuit
 - 8-bit pulse measuring counter, 6-stage FIFO
- Interruption
 - 21 factors, 15 vectors, multi-interruption possible
- Standby mode
 - SLEEP/STOP
- Package
 - 100-pin plastic QFP/LQFP
- Piggyback/evaluation chip
 - CXP87700 100-pin ceramic QFP/LQFP

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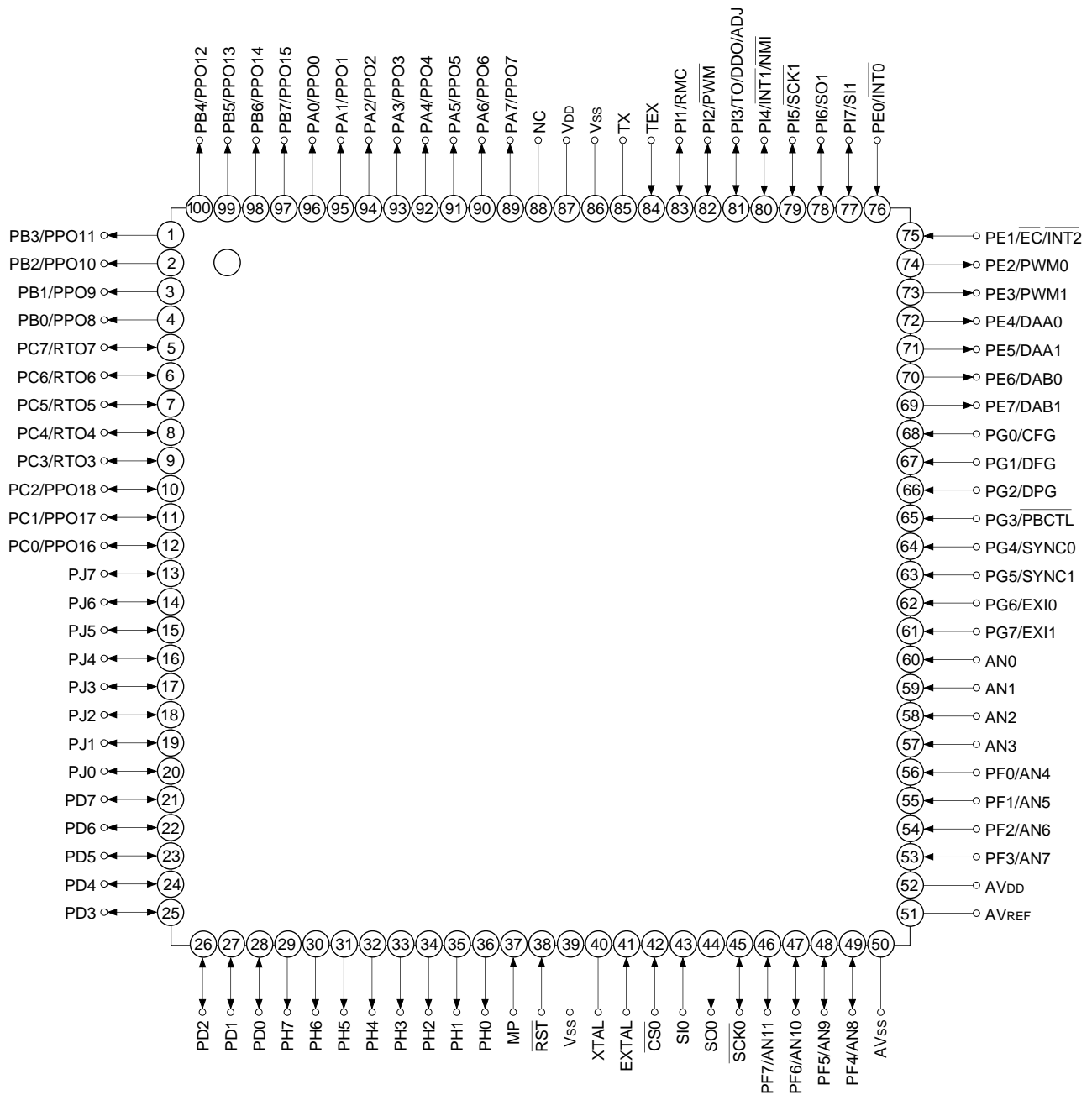
Block Diagram

Pin Configuration 1 (Top View) 100 pin QFP package



- Note)**
1. NC (Pin 90) is always connected to VDD.
 2. Vss (Pins 41 and 88) are both connected to GND.

Pin Configuration 2 (Top View) 100 pin LQFP package



- Note**
1. NC (Pin 88) is always connected to VDD.
 2. Vss (Pins 39 and 86) are both connected to GND.

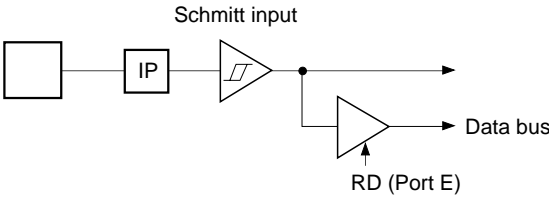
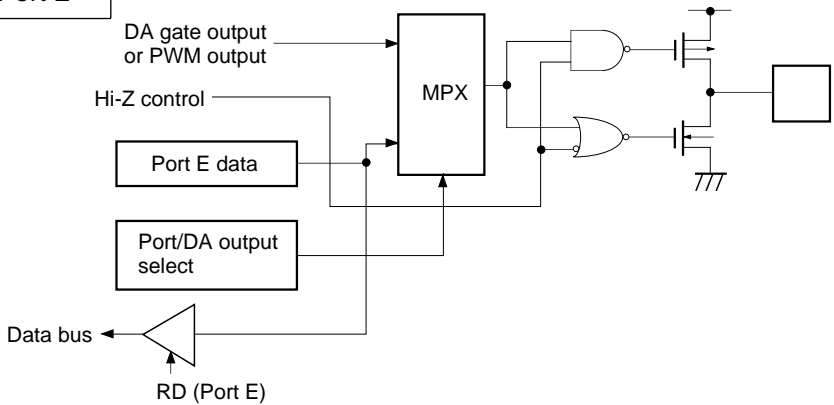
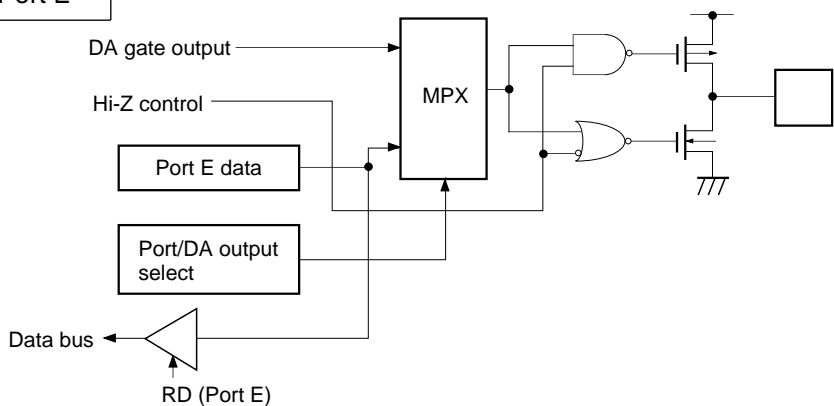
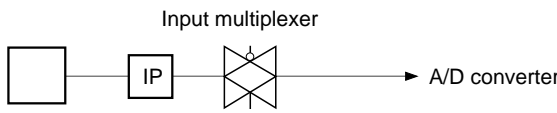
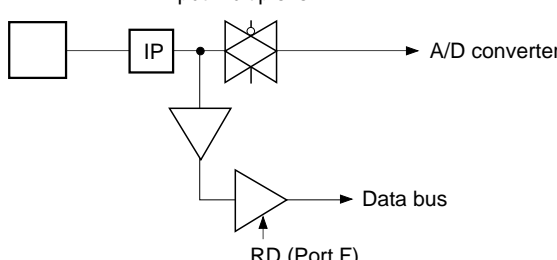
Pin Description

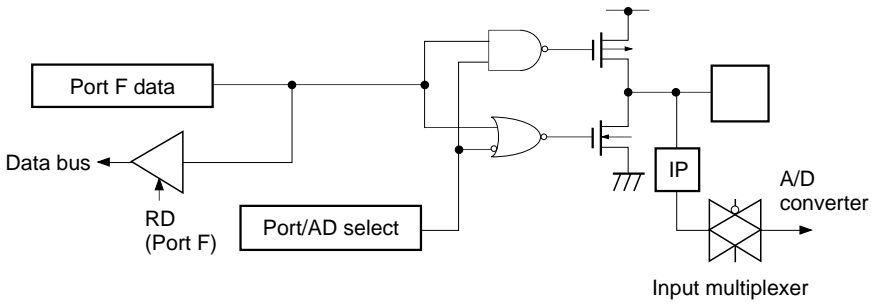
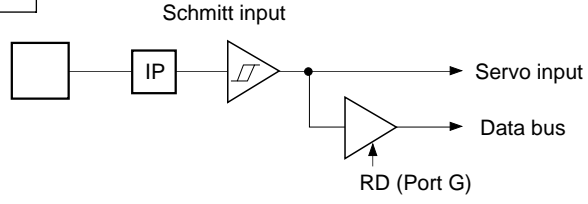
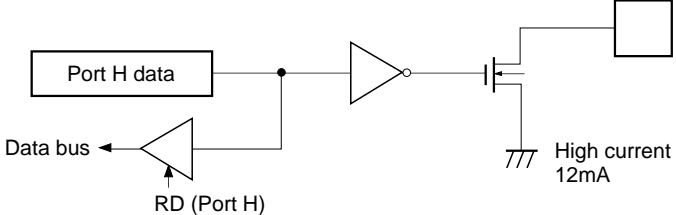
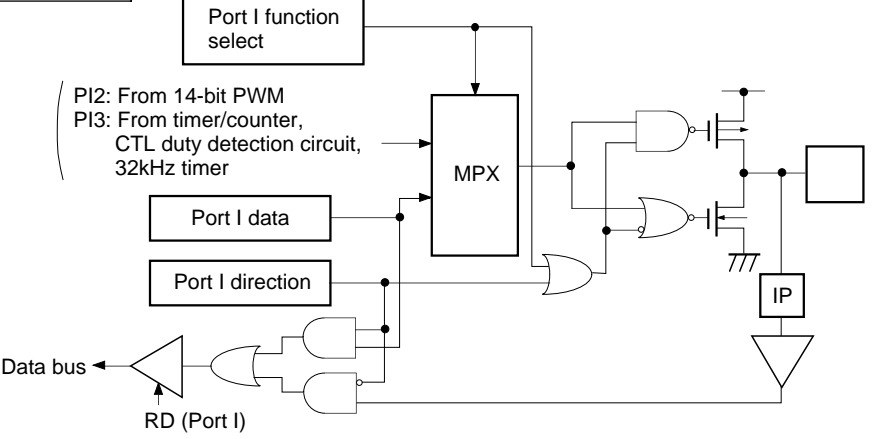
Symbol	I/O	Description		
PA0/PPO0 to PA7/PPO7	Output/ Real time Output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real time pulse output port. (19 pins)	
PB0/PPO8 to PB7/PPO15	Output/ Real time Output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)		
PC0/PPO16 to PC2/PPO18	I/O/ Real time Output	(Port C) 8-bit I/O port, enables to specify I/O by bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)		
PC3/RTO3 to PC7/RTO7	I/O/ Real time Output		Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. Enable to specify I/O by 4-bit unit. Enables to drive 12mA sink current. (8 pins)		
PE0/ $\overline{\text{INT0}}$	Input/input	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Input pin to request external interruption. Active when falling edge.	
PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$	Input/input/input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output/output		PWM output pins. (2 pins)	
PE3/PWM1	Output/output			
PE4/DAA0	Output/output			
PE5/DAA1	Output/output			
PE6/DAB0	Output/output			
PE7/DAB1	Output/output			
			DA gate pulse output pins. (4 pins)	
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)		
PF0/AN4 to PF3/AN7	Input/input	(Port F) Lower 4 bits are input port and upper 4 bits are output port. Lower 4 bits also serve as standby release input pin. (8 pins)		
PF4/AN8 to PF7/AN11	Output/input			
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O pin.		
SO0	Output	Serial data (CH0) output pin.		
SI0	Input	Serial data (CH0) input pin.		
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input pin.		

Symbol	I/O	Description	
PG0/CFG	Input/input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.
PG1/DFG	Input/input		Drum FG input pin.
PG2/DPG	Input/input		Drum PG input pin.
PG3/PBCTL	Input/input		Playback CTL pulse input pin.
PG4/SYNC0	Input/input		Composite sync signal input pin.
PG5/SYNC1	Input/input		
PG6/EXI0	Input/input		
PG7/EXI1	Input/input		External input pin to FRC capture unit.
PH0 to PH7	Output	(Port H) 8-bit output port ; Medium withstand voltage (12V) and high current (12mA), N-ch open drain output. (8 pins)	
PI1/RMC	I/O/input	(Port I) 7-bit I/O port. I/O port can be specified by bit unit. (7 pins)	Remote control receiving circuit input pin.
PI2/PWM	I/O/output		14-bit PWM output pin.
PI3/TO/ DDO/ADJ	I/O/output/ output/output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output pin.
PI4/INT1/ NMI	I/O/input/Input		Input pin to request external interruption and non maskable interruption. Active when falling edge.
PI5/SCK1	I/O/I/O		Serial clock (CH1) I/O pin.
PI6/SO1	I/O/output		Serial data (CH1) output pin.
PI7/SI1	I/O/input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O		(Port J) 8-bit I/O port. Function as standby release input can be specified by bit unit. I/O can be specified by bit unit.
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
RST	Input	System reset pin of active "L" level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AVDD		Positive power supply pin of A/D converter.	
AVREF	Input	Reference voltage input pin of A/D converter.	
AVss		GND pin of A/D converter.	
VDD		Positive power supply pin.	
Vss		GND pin. Connect both Vss pins to GND.	

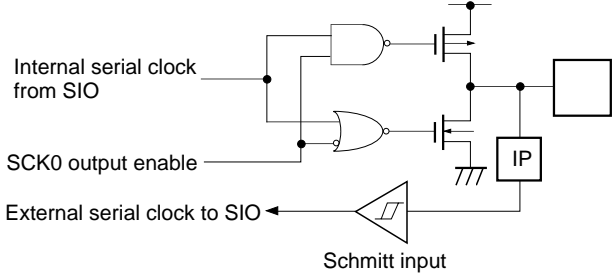
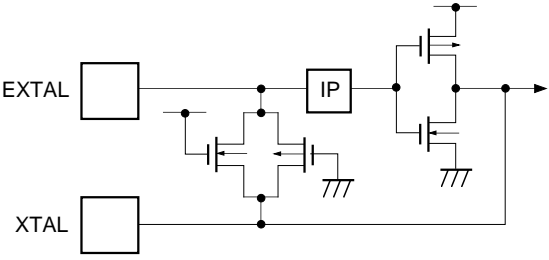
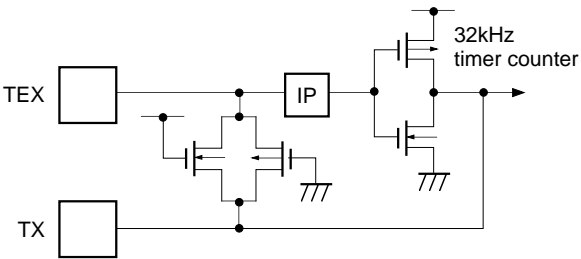
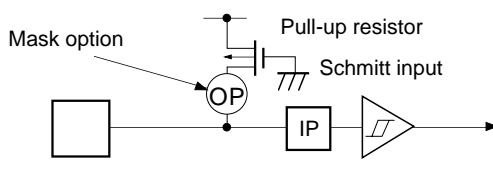
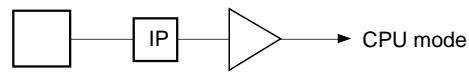
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>Port A Port B</p> <p>PA0/PPO0 to PA7/PPO7 PB0/PPO8 to PB7/PPO15</p> <p>16 pins</p>	<p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>Port C</p> <p>PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7</p> <p>8 pins</p>	<p>(Every bit)</p>	<p>Hi-Z</p>
<p>Port D</p> <p>PD0 to PD7</p> <p>8 pins</p>	<p>(Every 4 bits) (PD0 to 3) (PD4 to 7)</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE0/$\overline{\text{INT0}}$ PE1/$\overline{\text{EC/INT2}}$</p> <p>2 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1</p> <p>4 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE6/DAB0 PE7/DAB1</p> <p>2 pins</p>	<p>Port E</p> 	<p>H level</p>
<p>AN0 to AN3</p> <p>4 pins</p>		<p>Hi-Z</p>
<p>PF0/AN4 to PF3/AN7</p> <p>4 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PF4/AN8 to PF7/AN11</p> <p>4 pins</p>	<p>Port F</p>  <p>Data bus</p> <p>RD (Port F)</p> <p>Port/AD select</p> <p>IP</p> <p>Input multiplexer</p> <p>A/D converter</p>	<p>Hi-Z</p>
<p>PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1</p> <p>8 pins</p>	<p>Port G</p>  <p>Schmitt input</p> <p>IP</p> <p>Servo input</p> <p>Data bus</p> <p>RD (Port G)</p> <p>Note) For PG4/SYNC0, PG5/SYNC1, CMOS schmitt input and TTL schmitt input can be selected with the mask option.</p>	<p>Hi-Z</p>
<p>PH0 to PH7</p> <p>8 pins</p>	<p>Port H</p>  <p>Port H data</p> <p>Data bus</p> <p>RD (Port H)</p> <p>Medium withstand voltage 12V</p> <p>High current 12mA</p>	<p>Hi-Z</p>
<p>PI2/PWM PI3/TO/ DDO/ADJ</p> <p>2 pins</p>	<p>Port I</p>  <p>Port I function select</p> <p>MPX</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>IP</p> <p>High current 12mA</p> <p>(PI2: From 14-bit PWM PI3: From timer/counter, CTL duty detection circuit, 32kHz timer</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
PI1/RMC PI4/INT1/NMI PI7/SI1 3 pins	<p>Port I</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Schmitt input</p> <p>IP</p> <p>(PI1: To remote control circuit PI4: To interruption circuit PI7: To serial CH1</p>	Hi-Z
PI5/SCK1 PI6/SO1 2 pins	<p>Port I</p> <p>Port I function select</p> <p>From serial CH1</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>MPX</p> <p>Note) (PI5 is schmitt input PI6 is inverter input</p> <p>To serial CH1</p> <p>IP</p>	Hi-Z
PJ0 to PJ7 8 pins	<p>Port J</p> <p>Port J data</p> <p>Port J direction</p> <p>Data bus</p> <p>RD (Port J)</p> <p>Edge detection</p> <p>Standby release</p> <p>IP</p>	Hi-Z
$\overline{CS0}$ SIO 2 pins	<p>Schmitt input</p> <p>IP</p> <p>To SIO</p>	Hi-Z
SO0 1 pin	<p>SO0 from SIO</p> <p>SO0 output enable</p> <p>IP</p>	Hi-Z

Pin	Circuit format	When reset
<p>$\overline{\text{SCK0}}$</p> <p>1 pin</p>	 <p>Internal serial clock from SIO</p> <p>SCK0 output enable</p> <p>External serial clock to SIO</p> <p>Schmitt input</p>	<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop. XTAL becomes "H" level. 	<p>Oscillation</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Mask option</p> <p>Pull-up resistor</p> <p>Schmitt input</p>	<p>L level</p>
<p>MP</p> <p>1 pin</p>	 <p>CPU mode</p>	<p>Hi-Z</p>

Absolute Maximum Ratings

(V_{SS}=0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ²	V	
Medium withstand output voltage	V _{OUTP}	-0.3 to +15.0	V	PH pin
High level output current	I _{OH}	-5	mA	
High level total output current	∑I _{OH}	-50	mA	Total of output pins
Low level output current	I _{OL}	15	mA	Other than high current output pins: per pin
	I _{OLC}	20	mA	High current port pin* ³ : per pin
Low level total output current	∑I _{OL}	130	mA	Total of output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP package type
		380		LQFP package type

*¹ AV_{DD} and V_{DD} should be set to a same voltage.

*² V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*³ The high current operation transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	fc = 16MHz Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.0	5.5	V	
		2.7	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.7	5.5	V	Guaranteed operation range by TEX clock
		2.5	5.5	V	Guaranteed data hold operation range during STOP
Analog power supply	AV _{DD}	3.0	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS schmitt input*3
	V _{IHTS}	2.2	V _{DD}	V	TTL schmitt input*4, *7
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*5, *7 TEX pin*6, *7
		V _{DD} - 0.2	V _{DD} + 0.2	V	EXTAL pin*5, *8 TEX pin*6, *8
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2, *7
		0	0.2V _{DD}	V	*2, *8
	V _{ILS}	0	0.2V _{DD}	V	CMOS schmitt input*3
	V _{ILTS}	0	0.8	V	TTL schmitt input*4, *7
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*5, *7 TEX pin*6, *7
		-0.3	0.2	V	EXTAL pin*5, *8 TEX pin*6, *8
Operating temperature	Topr	-20	+75	°C	

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 Normal input port (each pin of PC, PD, PE0 to PE1, PF0 to PF3, PG, PI and PJ), MP pin.

*3 Each pin of CS₀, SI₀, SCK₀, RST, PE0/INT₀, PE1/EC/INT₂, PG (For PG4 and PG5, when CMOS schmitt input is selected with mask option), PI1/RMC, PI4/INT1/NMI, PI5/SCK1 and PI7/SI1.

*4 Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)

*5 It specifies only when the external clock is input.

*6 It specifies only when the event count clock is input.

*7 This case applies to the range of 4.5 to 5.5V supply voltage (V_{DD}).

*8 This case applies to the range of 3.0 to 3.6V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics ($V_{DD} = 4.5$ to $5.5V$)

($T_a = -20$ to $+75^{\circ}C$, $V_{SS} = 0V$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (VOL only)	$V_{DD} = 4.5V, I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V, I_{OH} = -1.2mA$	3.5			V
Low level output voltage	V_{OL}	PI1 to PI7 PJ, SO0, SCK0	$V_{DD} = 4.5V, I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V, I_{OL} = 3.6mA$			0.6	V
		PD, PH	$V_{DD} = 4.5V, I_{OL} = 12.0mA$			1.5	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.5		40	μA
	I_{ILE}		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.5		-40	μA
	I_{IHT}	TEX	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.1		10	μA
	I_{ILT}		$V_{DD} = 5.5V,$ $V_{IL} = 0.4V$	-0.1		-10	μA
	I_{ILR}			\overline{RST}^{*1}	-1.5		-400
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP, AN0 to AN3, CS0, SI0, SO0, SCK0, \overline{RST}^{*1}	$V_{DD} = 5.5V,$ $V_I = 0, 5.5V$			± 10	μA
Open drain output leakage current (N-CH Tr OFF in state)	I_{LOH}	PH	$V_{DD} = 5.5V$ $V_{OH} = 12V$			50	μA
Supply current*2	I_{DD1}	V_{DD}	16MHz crystal oscillation ($C_1 = C_2 = 15pF$)		24	45	mA
			$V_{DD} = 5V \pm 0.5V^{*3}$				
	I_{DDS1}		SLEEP mode		1.3	8	mA
			$V_{DD} = 5V \pm 0.5V$				
	I_{DD2}		32kHz crystal oscillation ($C_1 = C_2 = 47pF$)		35	100	μA
			$V_{DD} = 3V \pm 0.3V$				
I_{DDS2}	SLEEP mode		6	30	μA		
	$V_{DD} = 3V \pm 0.3V$						
I_{DDS3}	STOP mode (EXTAL and TEX pins oscillation stop)				10	μA	
	$V_{DD} = 5V \pm 0.5V$						
Input capacity	C_{IN}	Other than $V_{DD}, V_{SS}, AV_{DD},$ and AV_{SS}	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 \overline{RST} pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2 When entire output pins are open.

*3 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

DC Characteristics (V_{DD} = 3.0 to 3.6V)

(T_a = -20 to +75°C, V_{SS} = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V _{OL} only)	V _{DD} = 3.0V, I _{OH} = -0.15mA	2.7			V
			V _{DD} = 3.0V, I _{OH} = 0.5mA	2.3			V
Low level output voltage	V _{OL}	PI1 to PI7	V _{DD} = 3.0V, I _{OL} = 1.2mA			0.3	V
			V _{DD} = 3.0V, I _{OL} = 1.6mA			0.5	V
		PJ, SO0, SCK0	V _{DD} = 3.0V, I _{OL} = 5mA			1.0	V
Input current	I _{IHE}	EXTAL	V _{DD} = 3.6V, V _{IH} = 3.6V	0.3		20	μA
	I _{ILE}		V _{DD} = 3.6V, V _{IL} = 0.3V	-0.3		-20	μA
	I _{IHT}	TEX	V _{DD} = 3.6V, V _{IH} = 3.6V	0.1		10	μA
	I _{ILT}		V _{DD} = 3.6V, V _{IL} = 0.3V	-0.1		-10	μA
	I _{ILR}	RST*1	V _{DD} = 3.6V, V _{IL} = 0.3V	-0.9		-200	μA
I/O leakage current	I _{Iz}	PA to PG, PI, PJ, MP, AN0 to AN3, CS0, SI0, SO0, SCK0, RST*1	V _{DD} = 3.6V, V _I = 0, 3.6V			±10	μA
Open drain output leakage current	I _{LOH}	PH	V _{DD} = 3.6V, V _{OH} = 12V			50	μA
Supply current*2	I _{DD1}	V _{DD}	12MHz crystal oscillation (C ₁ = C ₂ = 15pF)		11	25	mA
	I _{DDS1}		V _{DD} = 3.3V ± 0.3V*3				
			SLEEP mode		0.5	2.5	mA
I _{DDS3}	STOP mode (EXTAL and TEX pins oscillation stop)				10	μA	
Input capacity	C _{IN}	Other than V _{DD} , V _{SS} , AV _{DD} , and AV _{SS}	Clock 1MHz		10		pF
			0V other than the measured pins		20		

*1 RST pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2 When entire output pins are open.

*3 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 3.0 to 5.5V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit	
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	VDD = 4.5 to 5.5V	1	16	MHz
					1	12	
System clock input pulse width	tXL, tXH	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)	VDD = 4.5 to 5.5V	28		ns
					37.5		
System clock input rise and fall times	tCR, tCF	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns	
Event count clock input pulse width	tEH, tEL	EC	Fig. 3	tsys × 4*		ns	
Event count clock input rise and fall times	tER, tEF	EC	Fig. 3		20	ns	
System clock frequency	fc	TEX TX	Fig. 2 VDD = 2.7 to 5.5V (32kHz clock applied condition)	32.768		kHz	
Event count clock input pulse width	tTL, tTH	TEX	Fig. 3	10		μs	
Event count clock input rise and fall times	tTR, tTF	TEX	Fig. 3		20	ms	

* tsys indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

Fig. 1. Clock timing

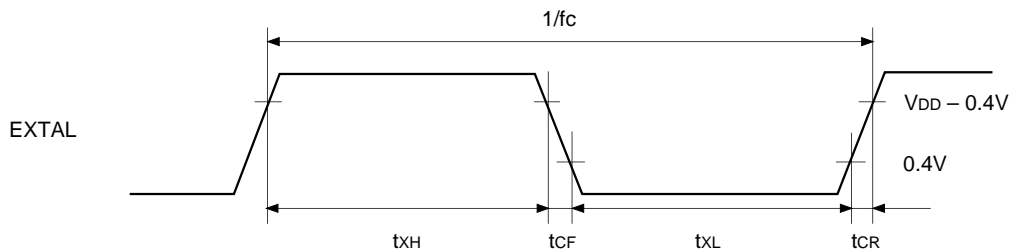


Fig. 2. Clock applied condition

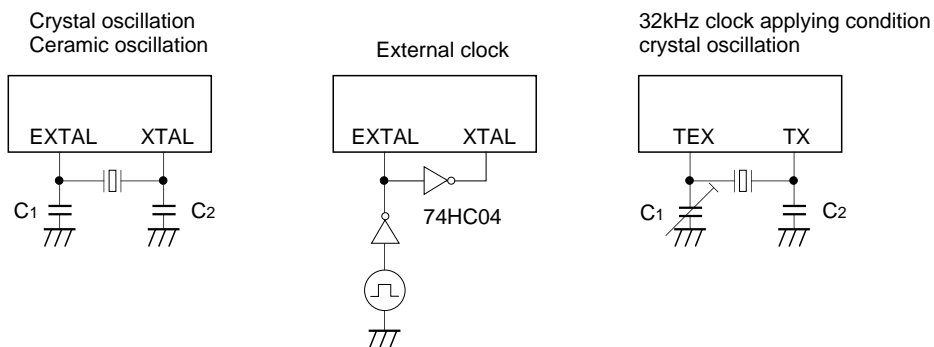
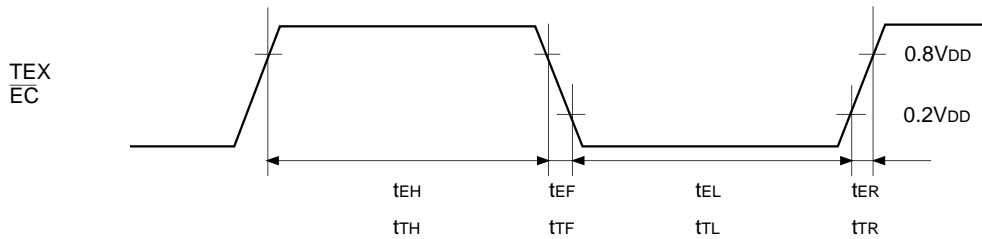


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
CS0 ↓ → SCK0 delay time	t _{DCSK}	SCK0	Chip select transfer mode (SCK0 = output mode)		t _{sys} +200	ns
CS0 ↑ → SCK0 floating delay time	t _{DCSKF}	SCK0	Chip select transfer mode (SCK0 = output mode)		t _{sys} +200	ns
CS0 ↓ → SO0 delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} +200	ns
CS0 ↑ → SO0 floating delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} +200	ns
CS0 high level width	t _{WHCS}	CS0	Chip select transfer mode	t _{sys} + 200		ns
SCK0 cycle time	t _{KCY}	SCK0	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
SCK0 high and low level widths	t _{KH} t _{KL}	SCK0	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 50		ns
SI0 input setup time (against SCK0 ↑)	t _{SIK}	SI0	SCK0 input mode	100		ns
			SCK0 output mode	200		ns
SI0 input hold time (against SCK0 ↑)	t _{KSI}	SI0	SCK0 input mode	t _{sys} + 200		ns
			SCK0 output mode	100		ns
SCK0 ↓ → SO0 delay time	t _{KSO}	SO0	SCK0 input mode		t _{sys} + 200	ns
			SCK0 output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

Note 2) The load of SCK0 output mode and SO0 output delay time is 50pF + 1TTL.

Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, VSS = 0V)

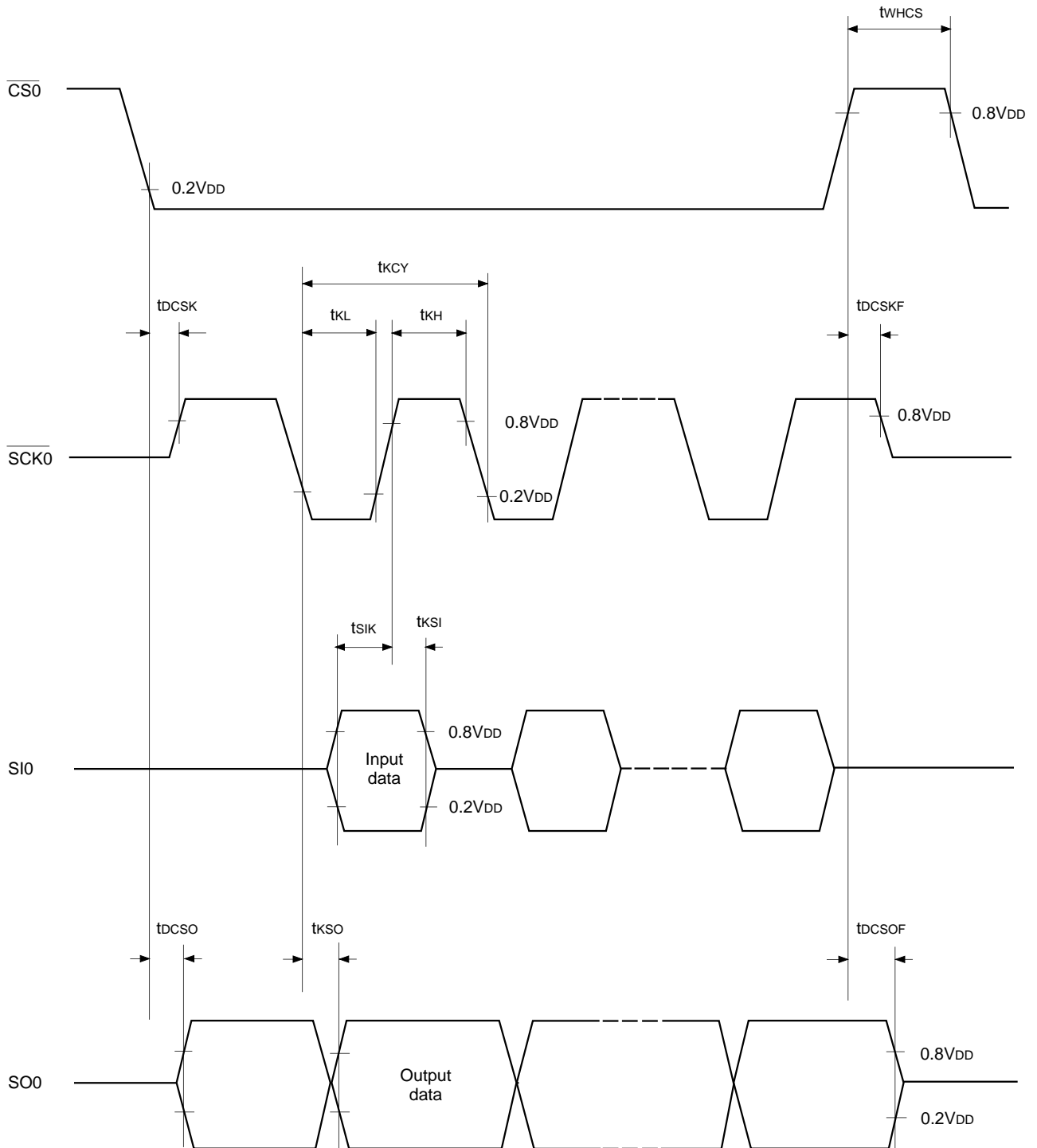
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t _{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		t _{sys} + 250	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ floating delay time	t _{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		t _{sys} + 200	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 250	ns
$\overline{CS0} \uparrow \rightarrow SO0$ floating delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0}$ high level width	t _{WHCS}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{SCK0}$ cycle time	t _{KCY}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level widths	t _{KH} t _{KL}	$\overline{SCK0}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 100		ns
SI0 input setup time (against $\overline{SCK0} \uparrow$)	t _{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (against $\overline{SCK0} \uparrow$)	t _{KSI}	SI0	$\overline{SCK0}$ input mode	t _{sys} + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t _{KSO}	SO0	$\overline{SCK0}$ input mode		t _{sys} + 250	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

Note 2) The load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF.

Fig. 4. Serial transfer CH0 timing



Serial transfer (CH1)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	8000/fc – 50		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ ↑)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF + 1TTL.

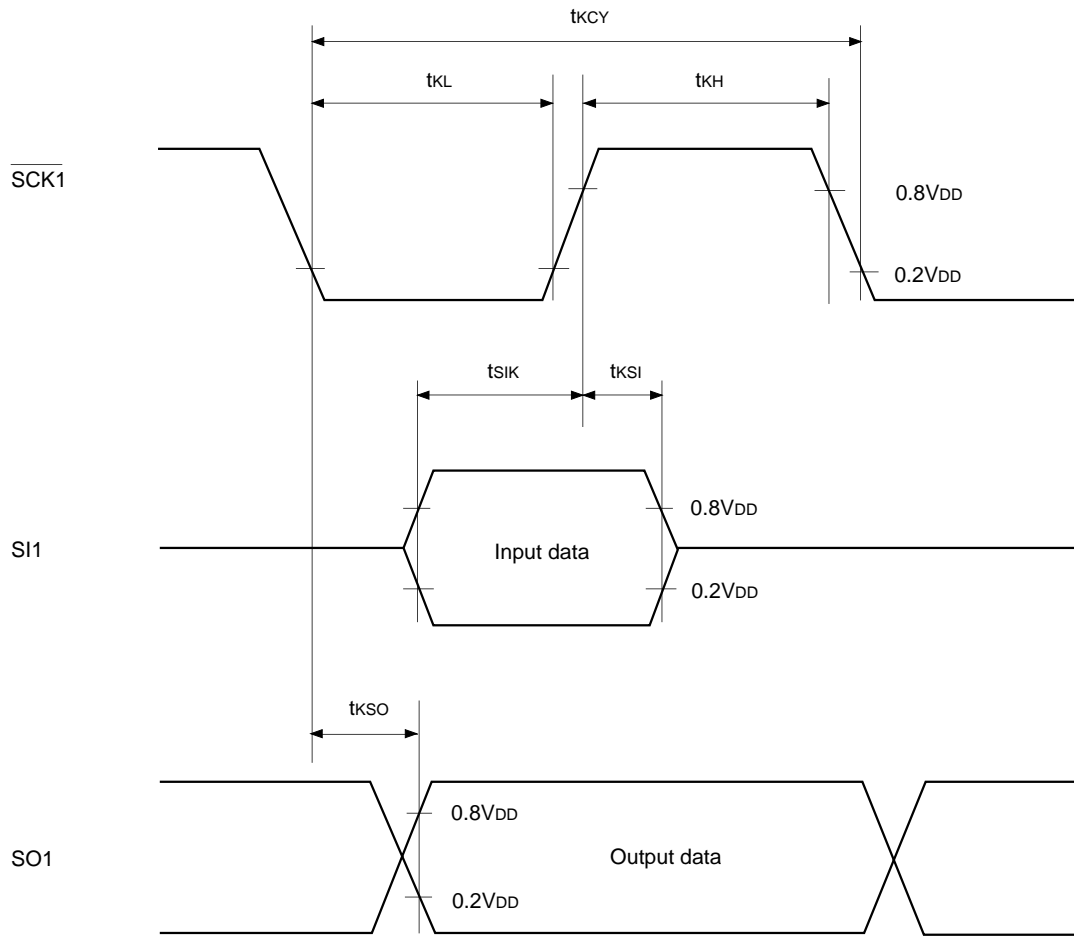
Serial transfer (CH1)

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	8000/fc – 100		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ ↑)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		250	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing



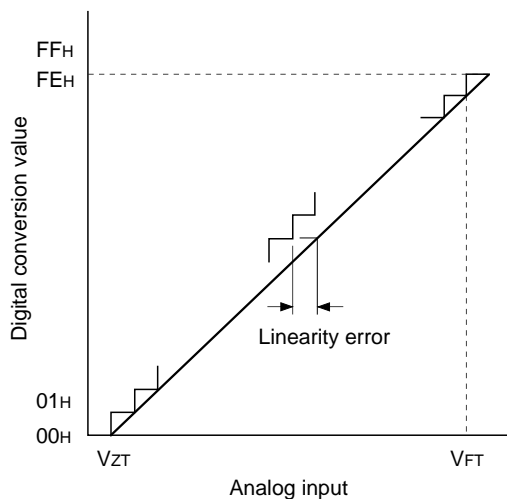
(3) A/D converter characteristics (Ta = -20 to +75°C, VDD = AVDD = 4.5 to 5.5V, AVREF = 4.0 to AVDD, VSS = AVSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C VDD = AVDD = AVREF = 5.0V VSS = AVSS = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	tCONV			160/fADC*			µs
Sampling time	tSAMP			12/fADC*			µs
Reference input voltage	VREF	AVREF		AVDD - 0.5		AVDD	V
Analog input voltage	VIAN	AN0 to AN11		0			V
AVREF current	IREF	AVREF	Operating mode		0.6	1.0	mA
	IREFS		SLEEP mode STOP mode 32kHz operating mode			10	µA

(Ta = -20 to +75°C, VDD = AVDD = 3.0 to 3.6V, AVREF = 2.7 to AVDD, VSS = AVSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C VDD = AVDD = AVREF = 3.3V VSS = AVSS = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	tCONV			160/fADC*			µs
Sampling time	tSAMP			12/fADC*			µs
Reference input voltage	VREF	AVREF		AVDD - 0.3		AVDD	V
Analog input voltage	VIAN	AN0 to AN11		0			V
AVREF current	IREF	AVREF	Operating mode		0.4	0.7	mA
	IREFS		SLEEP mode STOP mode 32kHz operating mode			10	µA

Fig. 6. Definitions of A/D converter terms



* The value of fADC is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).
 When PS2 is selected, fADC = fc/2
 When PS1 is selected, fADC = fc

(4) Interruption, reset input

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{NMI}}$ PJ0 to PJ7		1		μs
Reset input low level width	t_{RSL}	$\overline{\text{RST}}$		$32/f_c$		μs

Fig. 7. Interruption input timing

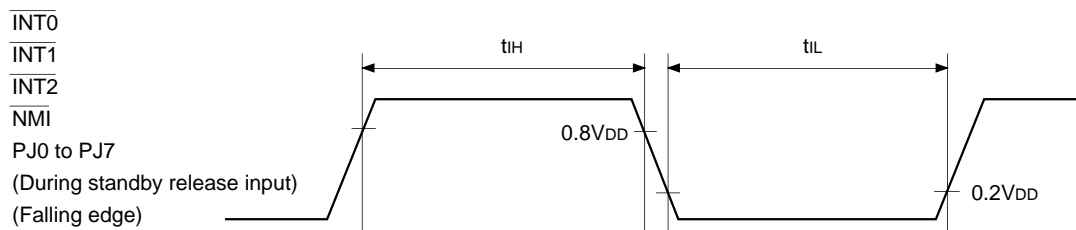
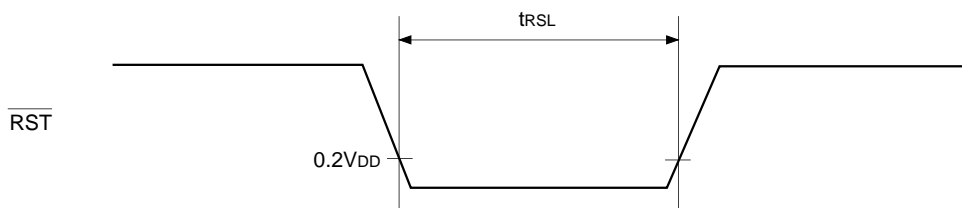


Fig. 8. Reset input timing



(5) Others

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$)

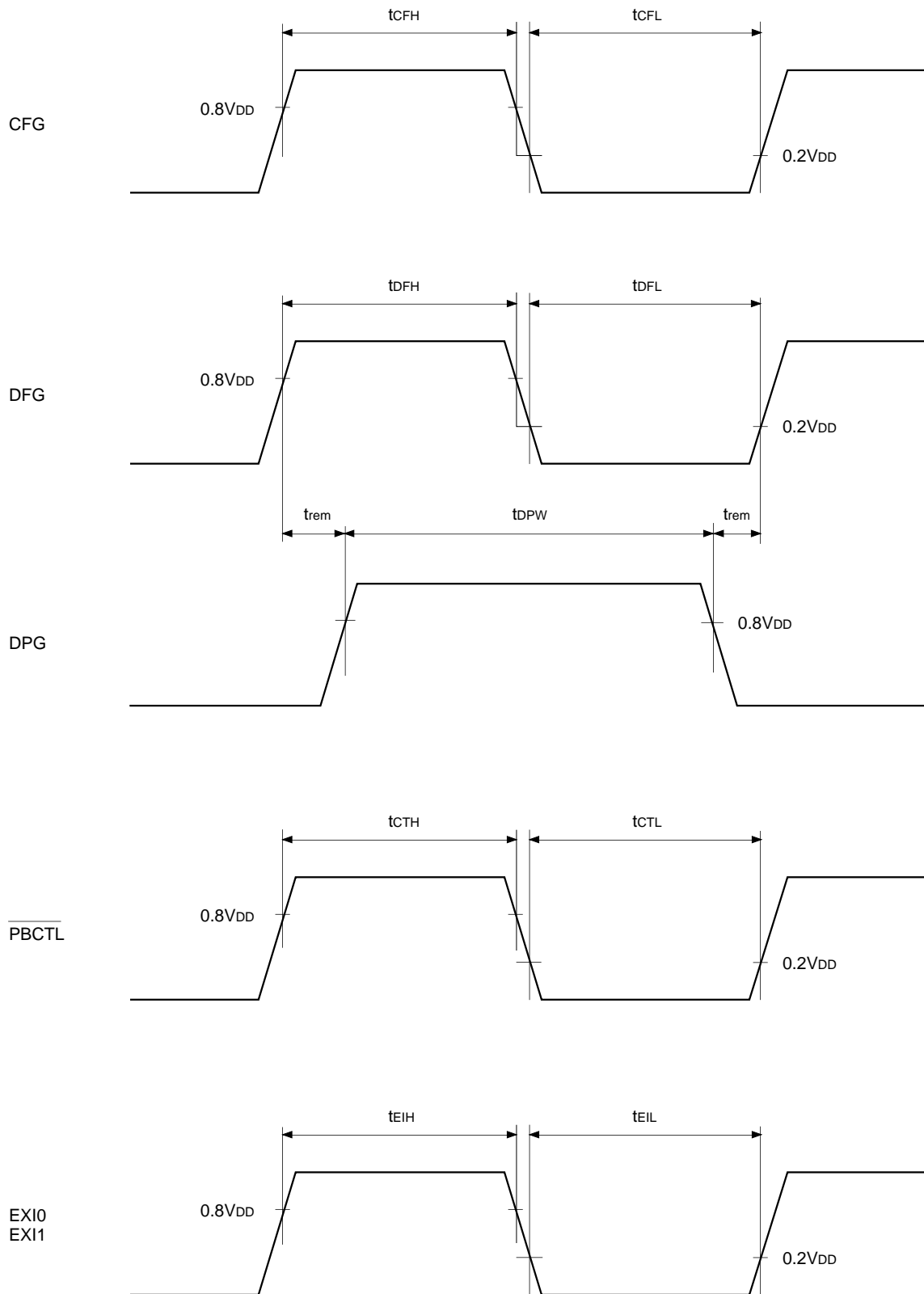
Item	Symbol	Pins	Conditions	Min.	Max.	Unit
CFG input high and low level widths	t_{CFH} t_{CFL}	CFG		$t_{FRC} \times 24 + 200$		ns
DFG input high and low level widths	t_{DFH} t_{DFL}	DFG		$t_{FRC} \times 8 + 200$		ns
DPG minimum pulse width	t_{DPW}	DPG		50		ns
DPG minimum removal time	t_{rem}	DPG		50		ns
$\overline{\text{PBCTL}}$ input high and low level widths	t_{CTH} t_{CTL}	$\overline{\text{PBCTL}}$	$t_{sys} = 2000/f_c$	$t_{FRC} \times 8 + 200 + t_{sys}$		ns
EXI input high and low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	$t_{sys} = 2000/f_c$	$t_{FRC} \times 8 + 200 + t_{sys}$		ns

Note) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2-bit = "00"), 4000/ f_c (Upper 2-bit = "01"), 16000/ f_c (Upper 2-bit = "11")

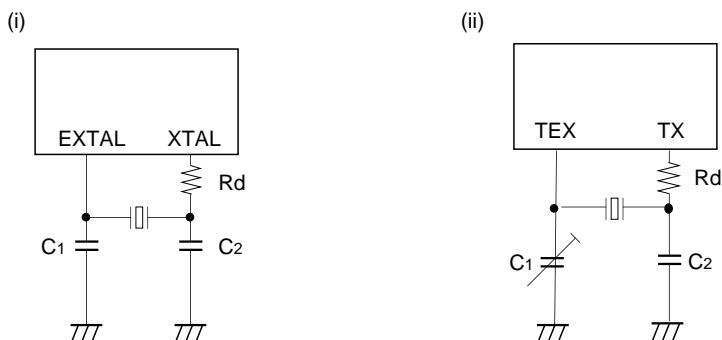
t_{FRC} [ns] = 1000/ f_c

Fig. 9. Other timings



Supplement

Fig. 10. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00				
		12.00	5	5		
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16	12	0	(i)
		10.00	16	12		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

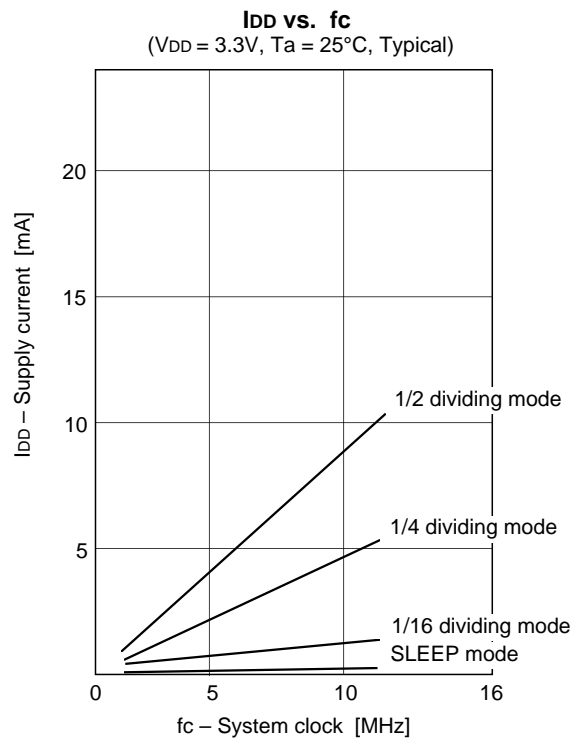
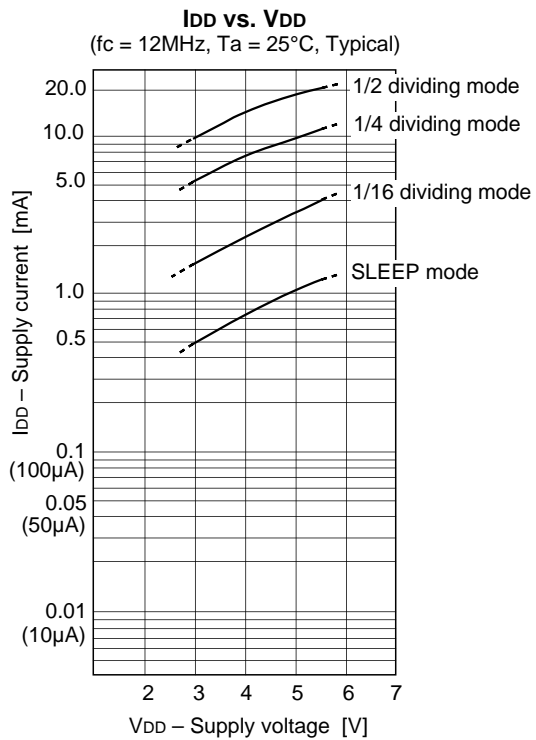
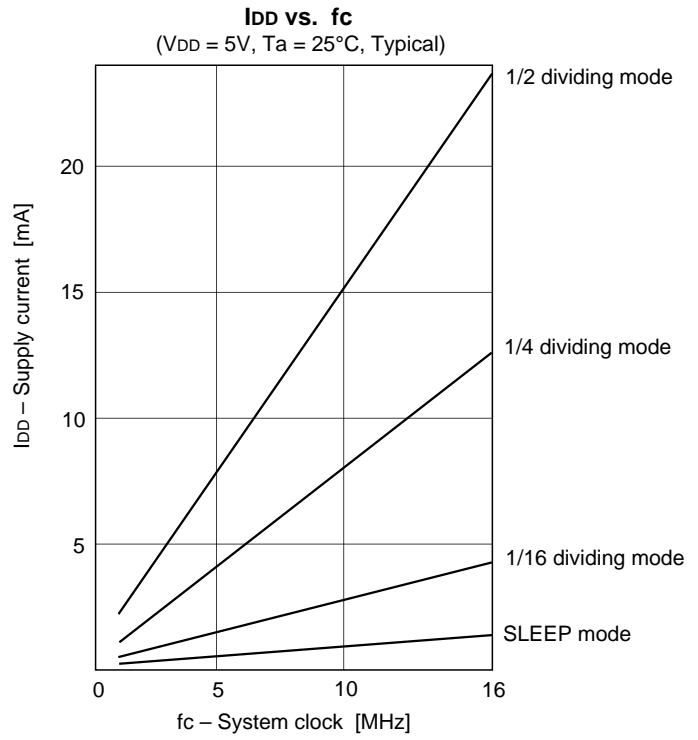
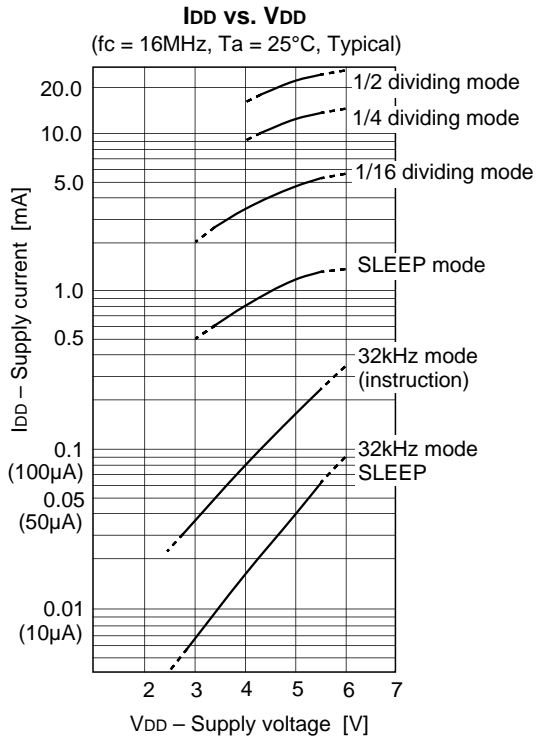
Those marked with an asterisk (*) signify types with built-in ground capacitance (C1, C2).

Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
Input circuit format*	C-MOS schmitt	TTL schmitt

* In PG4/SYNC0 pin and PG5/SYNC1 pin, the input circuit format can be selected to every pin. However, TTL schmitt can not be selected when the supply voltage (VDD) ranges from 3.5V to 5.5V.

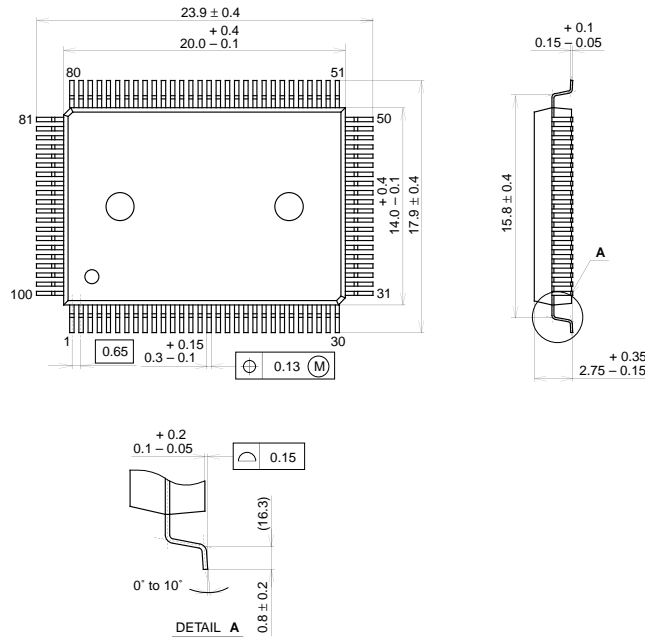
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

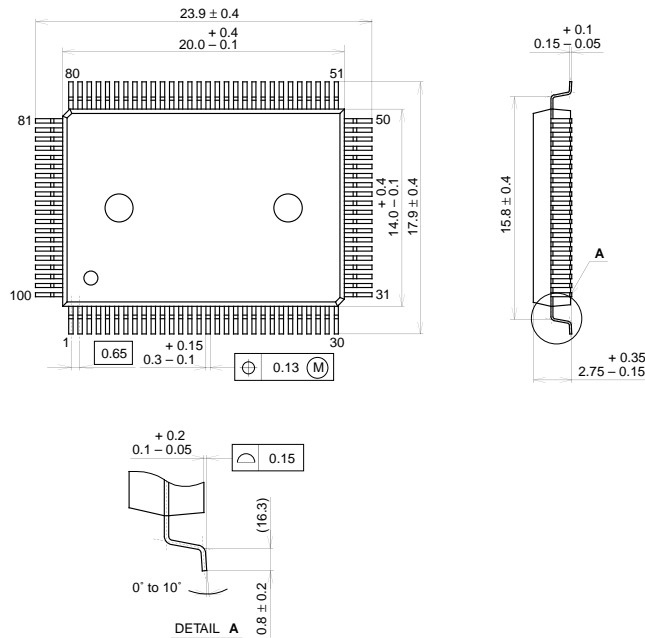


SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

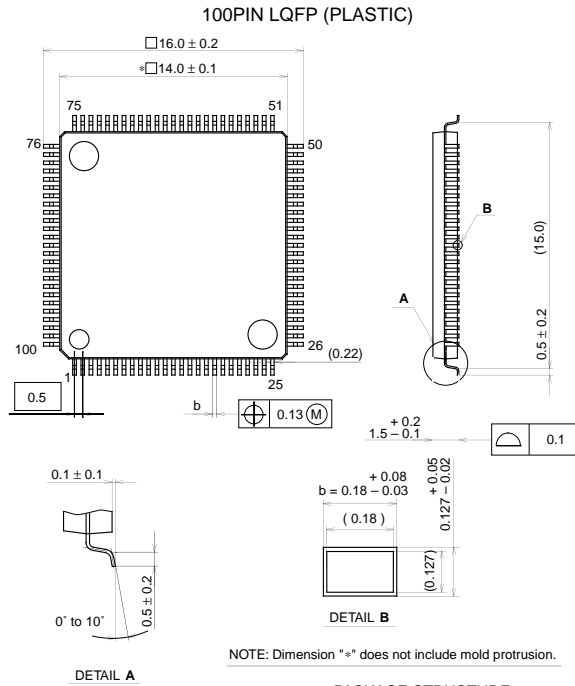
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm

Package Outline

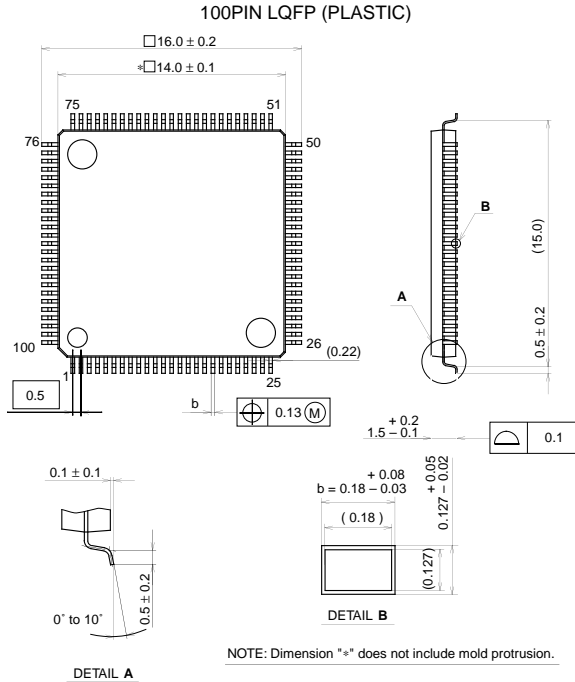
Unit: mm



PACKAGE STRUCTURE

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g



PACKAGE STRUCTURE

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm



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