SONY

CXP87500

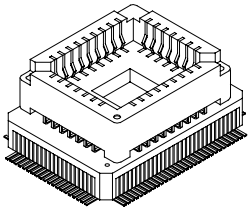
CMOS 8-bit Single Chip Microcomputer

Piggyback/ evaluator type

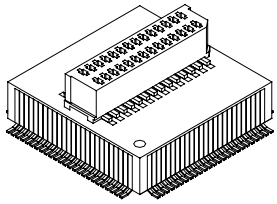
Description

The CXP87500 is a CMOS 8-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP87532/87540.

100 pin PQFP (Ceramic)



QFP supported



LQFP supported

Features

- A wide instruction set (213 instructions) which covers various types of data
  - 16-bit operation/multiplication and division/ boolean bit operation instructions
- Minimum instruction cycle 326ns at 12.288MHz operation
- Applicable EPROM LCC type 27C512
  (Maximum 40Kbytes are available)
- Incorporated RAM capacity 1344bytes
- Peripheral functions
  - Arithmetic coprocessor: Signed multiplication and division, signed sum of products. high speed execution of many bits shift rotation operation
  - A/D converter: 8-bit, 8-channel, successive approximation method (Conversion time of 13µs/12.288MHz) Incorporated 3-stage FIFO for A/D conversion data
  - Serial interface: Incorporated buffer RAM (auto transfer for 1 to 128bytes), 2-channel
  - Timer: 8-bit timer; 8-bit timer/counter; 19-bit time base timer
  - High precision timing pattern generator: PPG 11-pin, 32-stage programmable
  - PWM output: 12-bit, 2-channel (repetitive frequency 48kHz); 8-bit, 3-channel (repetitive frequency 48kHz)
  - Servo input control: Capstan FG, drum FG/PG, reel FG input
  - FRC capture unit: Incorporated 28-bit and 8-stage FIFO
- Interruption: 12 factors, 12 vectors, multi-interruption possible
- Standby mode: Sleep/stop
- Package: 100-pin ceramic PQFP

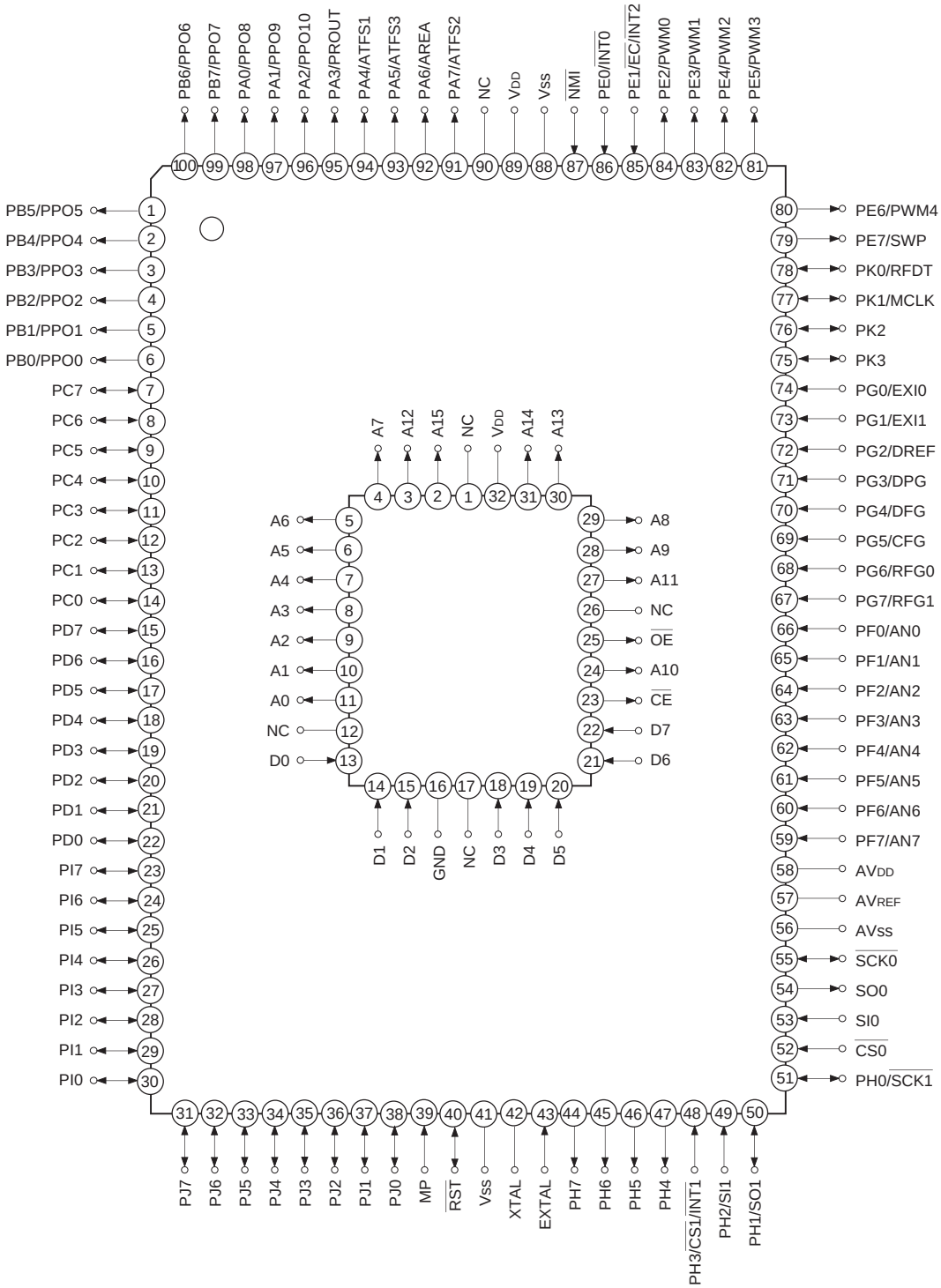
Note) Mask option depends on the type of the CXP87500. Refer to the Products List for details.

Structure

Silicon gate CMOS IC

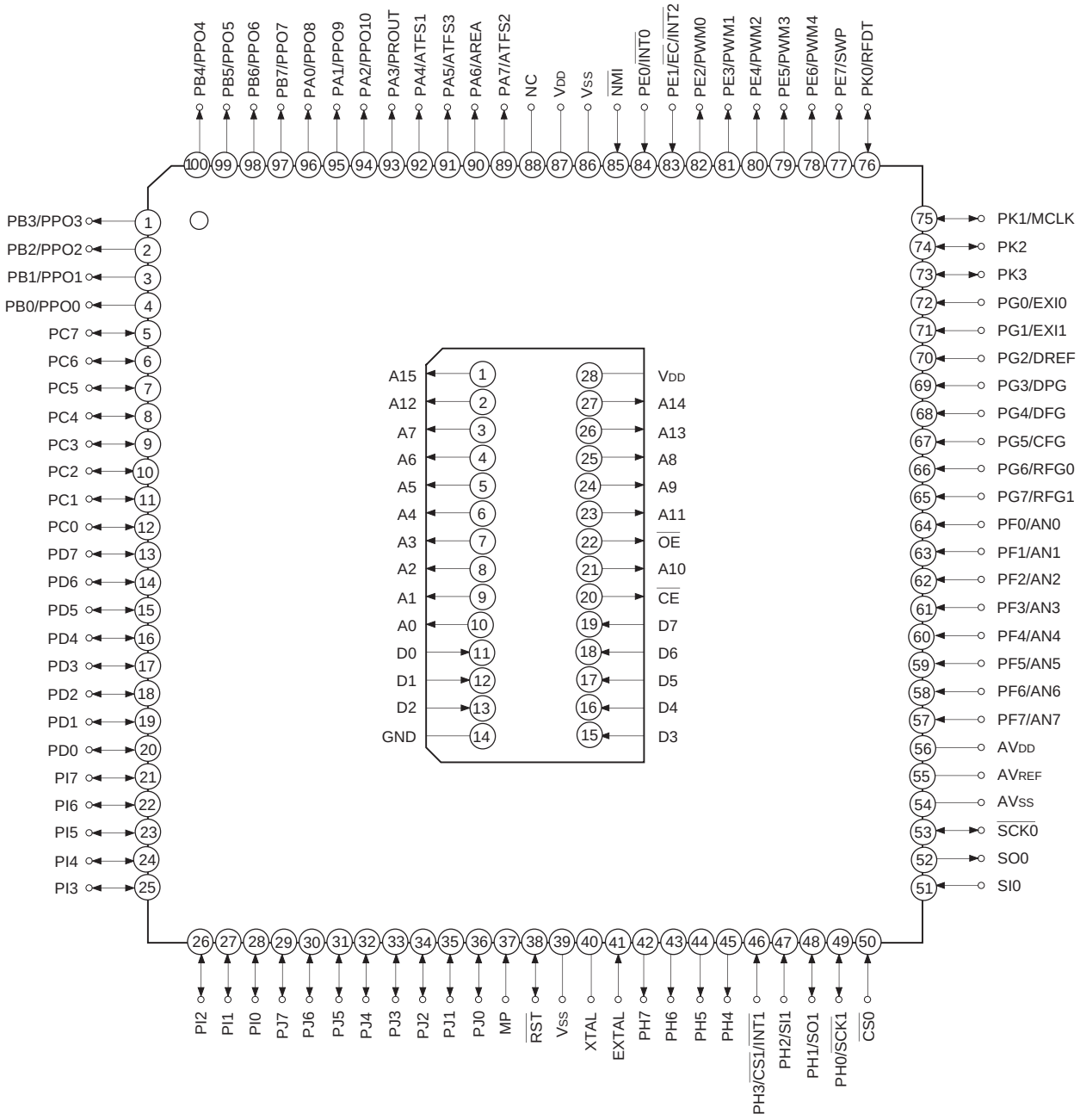
E93X12B81-PS

Pin Assignment in Piggyback Mode (QFP package)



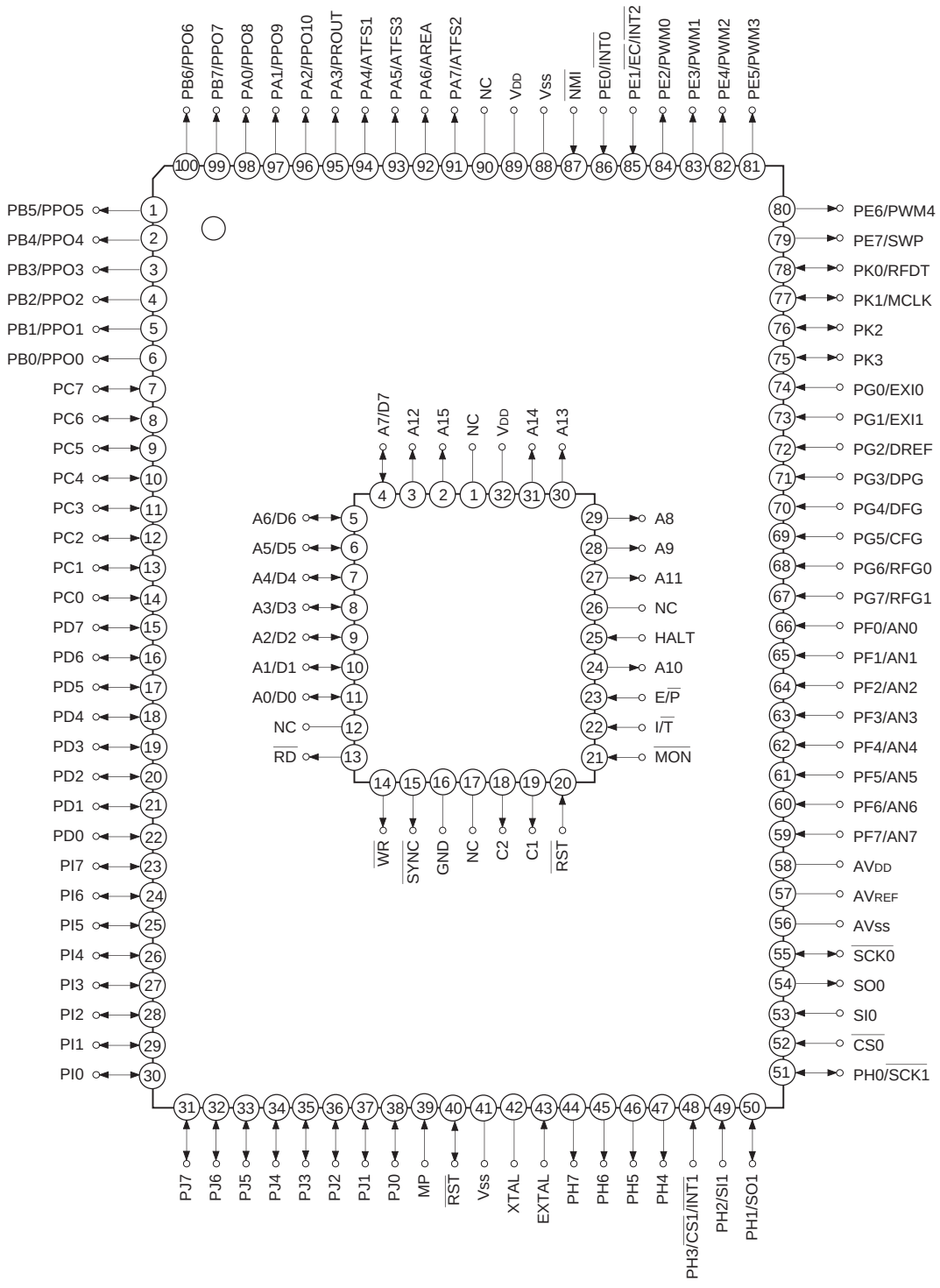
Note) 1. NC (Pin 90) is always connected to V_{DD}.
2. V_{SS} (Pins 41 and 88) are both connected to GND.
3. MP (Pin 39) is always connected to GND.

Pin Assignment in Piggyback Mode (LQFP package)



Note) 1. NC (Pin 88) is always connected to V_{DD}.
2. V_{SS} (Pins 39 and 86) are both connected to GND.
3. MP (Pin 37) is always connected to GND.

Pin Assignment in Evaluator Mode (QFP package)



Note) 1. NC (Pin 90) is always connected to V_{DD}.
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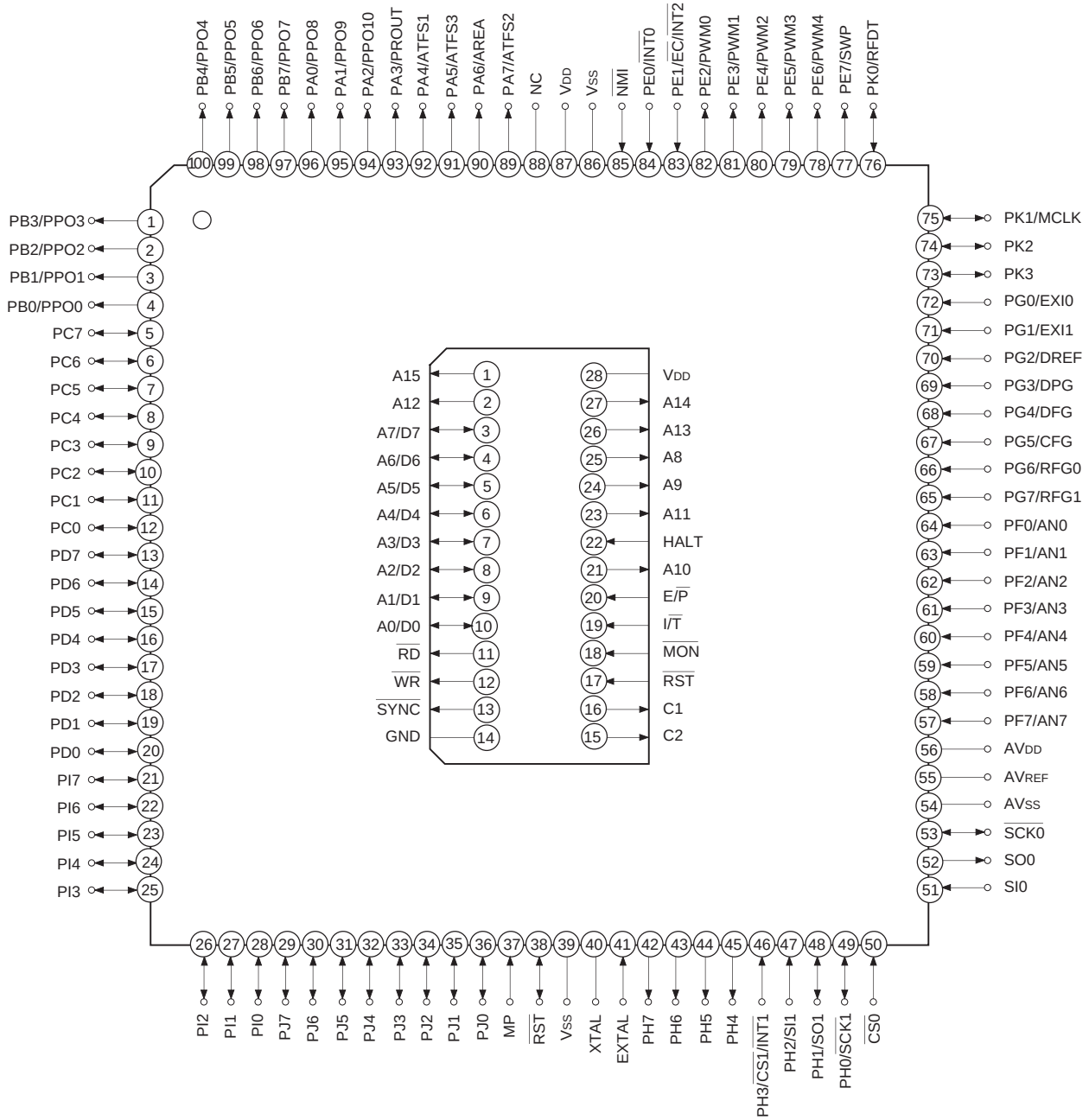
Pin Assignment in Evaluator Mode (LQFP package)

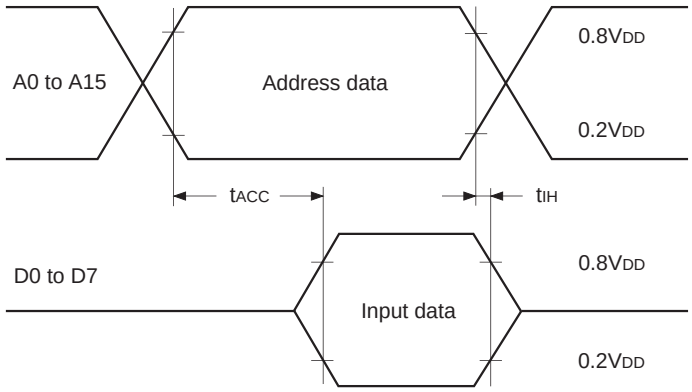


Note) 1. NC (Pin 88) is always connected to V_{DD}.
2. V_{SS} (Pins 39 and 86) are both connected to GND.
3. MP (Pin 37) is always connected to GND.

EPROM Read Timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		100	ns
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

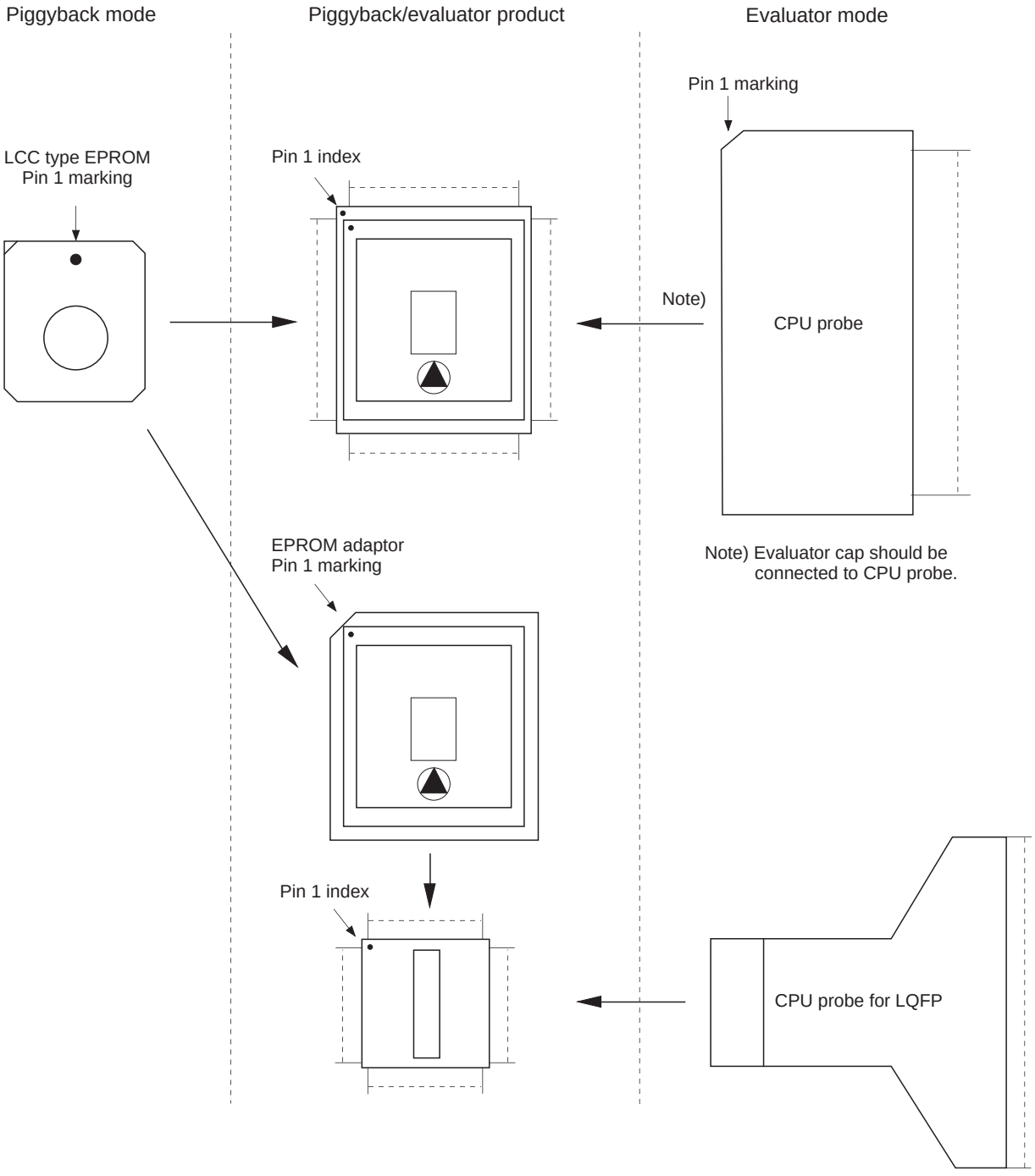


Products List

Optional item		Products		
		Mask		Piggyback/evaluator
		CXP87532	CXP87540	CXP87500-U01Q CXP87500-U01R
Package		100-pin plastic QFP/LQFP		100-pin ceramic PQFP
ROM capacity		32Kbytes	40Kbytes	EPROM 40Kbytes
Pull-up resistance for reset pin		Existent/Non-existent		Existent
Power on reset circuit		Existent/Non-existent		Existent
Input circuit format*1	PG0 to PG7, PK1	CMOS schmitt/TTLschmitt		TTL schmitt
	PK0	Buffer amplifier/Normal input		Buffer amplifier

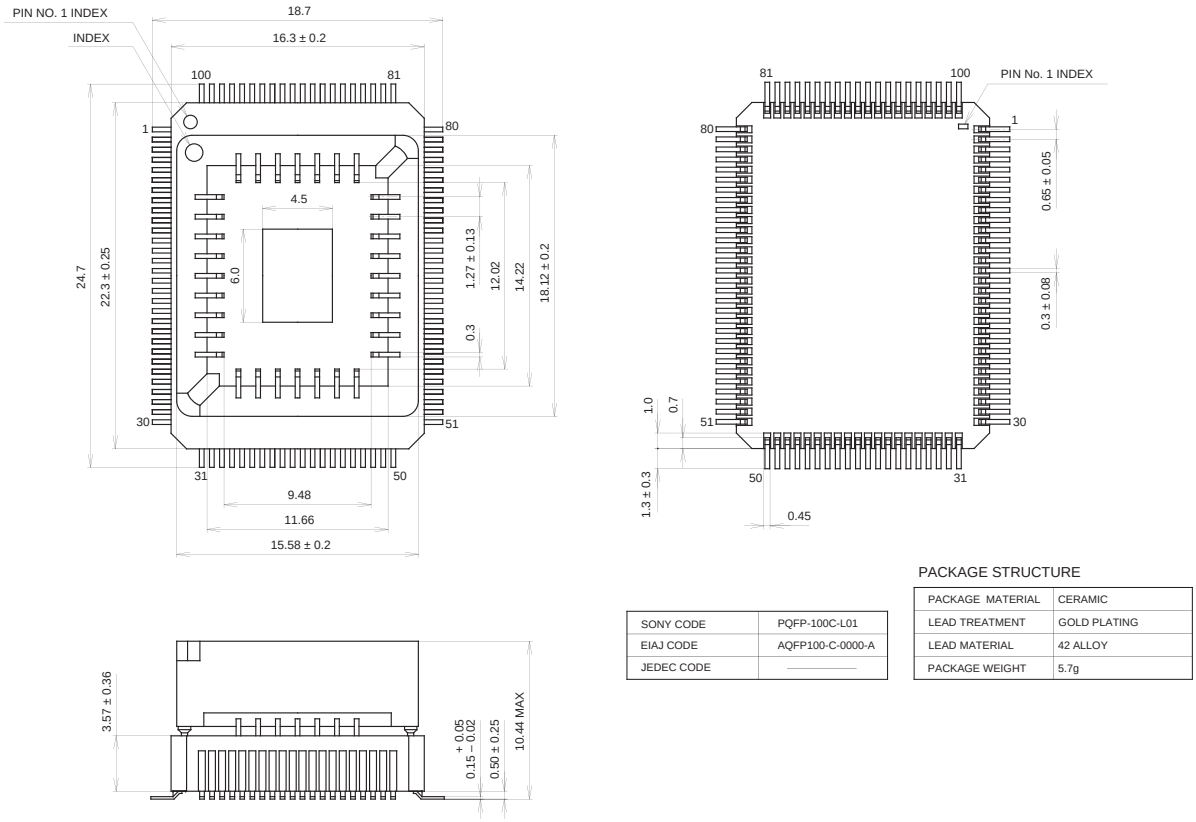
*1 On PK1/MCLK pin and PG0/EXI0 to PG7/RFG1 pin, the input circuit format of CMOS schmitt or TTL schmitt can be selected to every pin.
On PK0/RFDT pin, buffer amplifier or normal input circuit format can be selected.

Piggyback mode/evaluator mode can be switched as shown below.



Package Outline Unit: mm

100PIN PQFP (CERAMIC)

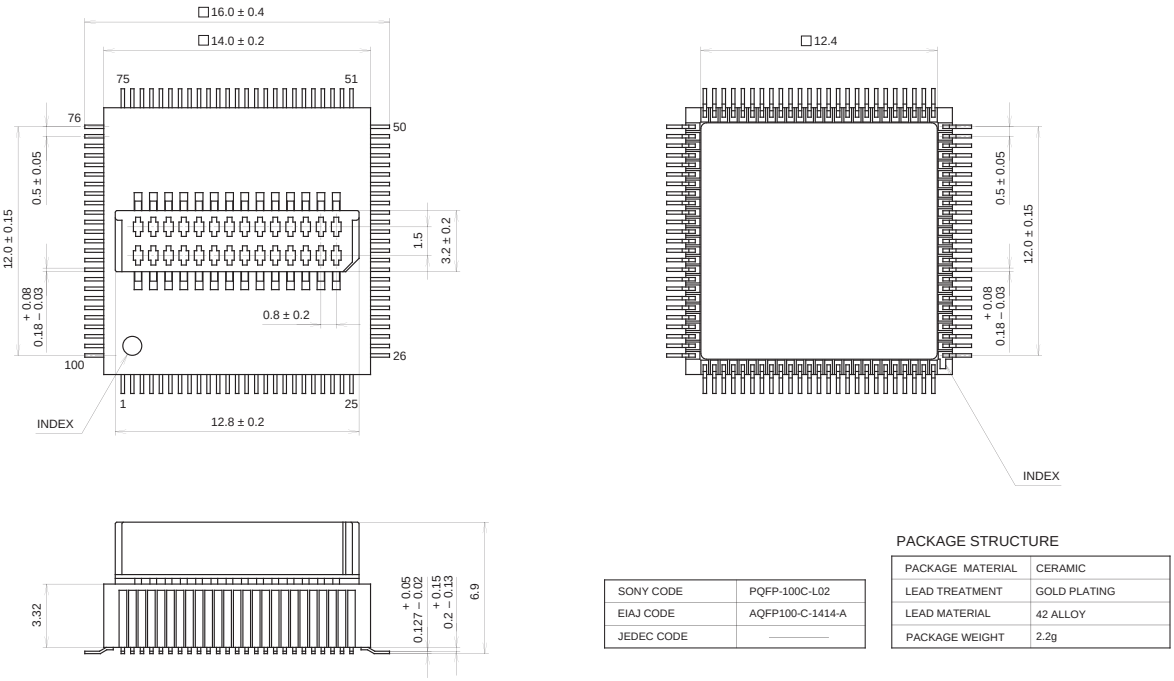


PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	————

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

100PIN PQFP (CERAMIC)



PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L02
EIAJ CODE	AQFP100-C-1414-A
JEDEC CODE	————

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	2.2g

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