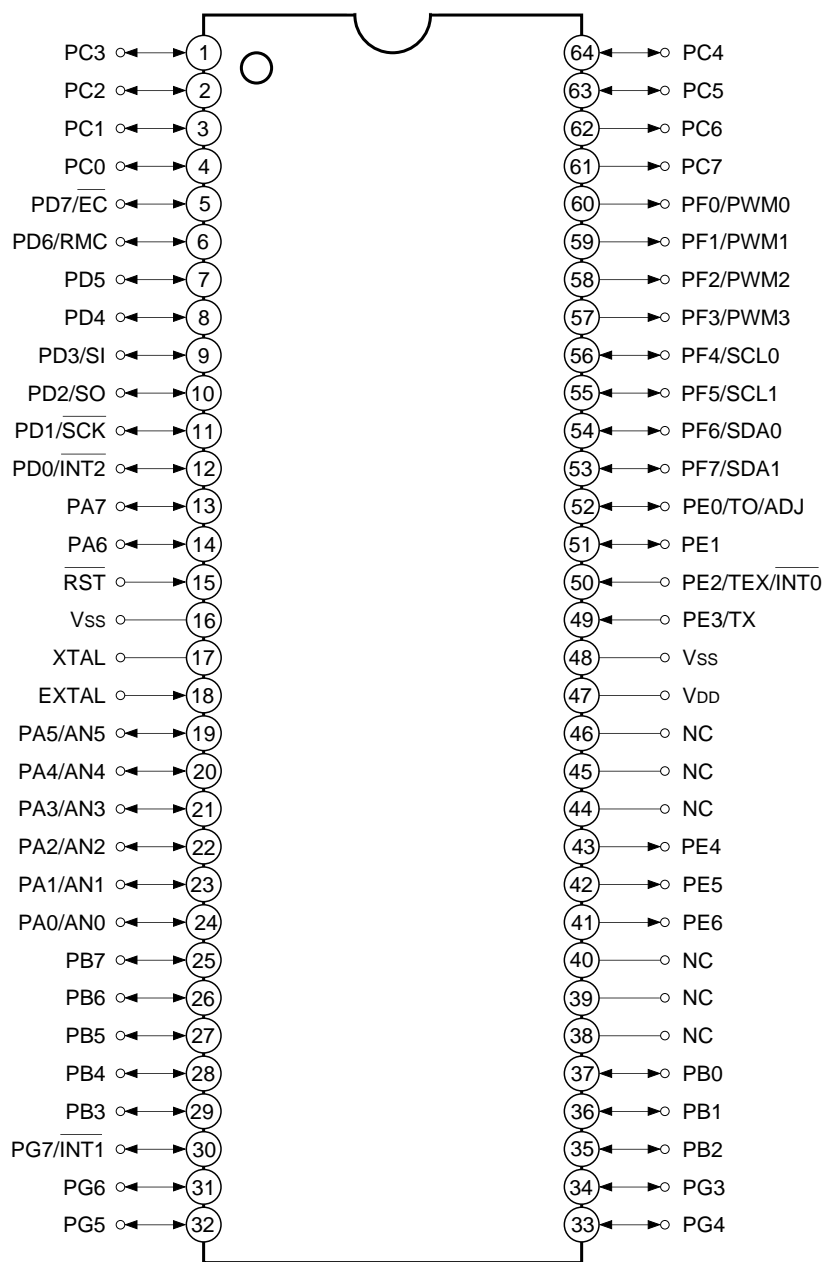
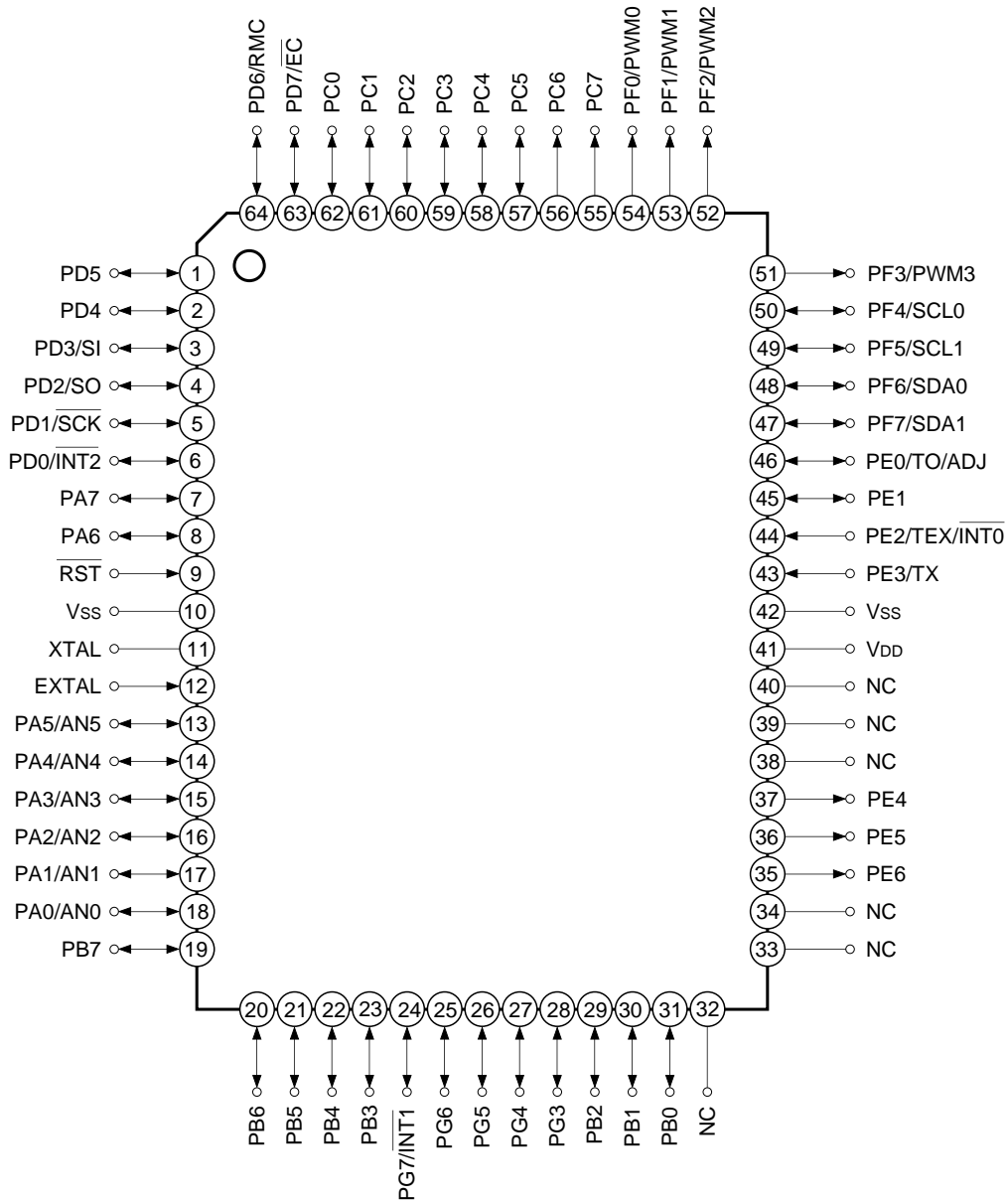


Pin Assignment (Top View) 64-pin SDIP



- Note)**
1. NC (Pins 38, 39, 40, 44 and 46) are left open.
  2. Vss (Pins 16 and 48) are both connected to GND.
  3. Pin 45 is the NC pin. However, connect it to VDD because it is the EXLC pin (input) for the piggyback/evaluator and OTP devices.

Pin Assignment (Top View) 64-pin QFP



- Note)**
1. NC (Pins 32, 33, 34, 38 and 40) are left open.
  2. Vss (Pins 10 and 42) are both connected to GND.
  3. Pin 39 is the NC pin. However, connect it to VDD because it is the EXLC pin (input) for the piggyback/evaluator and OTP devices.

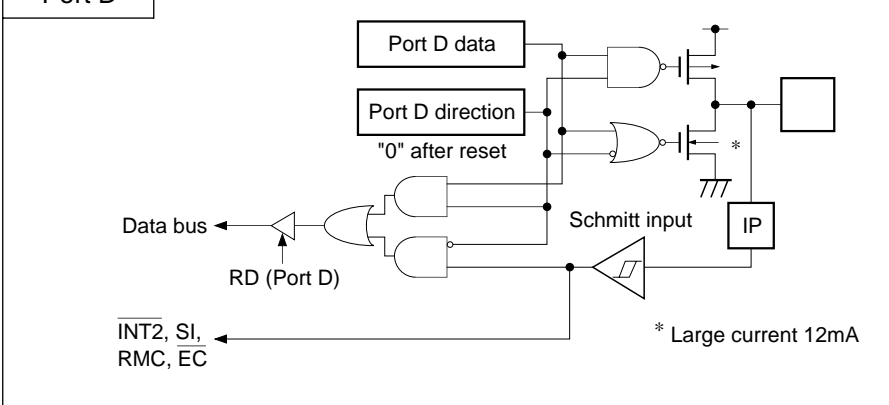
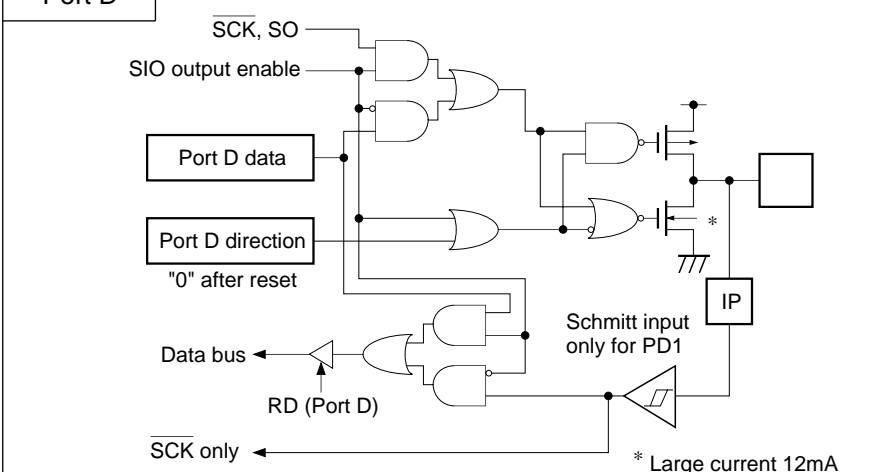
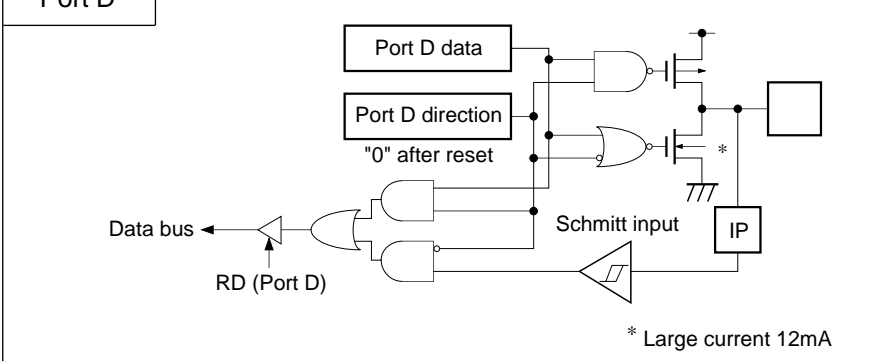
Pin Description

Symbol	I/O	Description		
PA0/AN0 to PA5/AN5	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Analog inputs to A/D converter. (6 pins)	
PA6 to PA7	I/O			
PB0 to PB7	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)		
PC0 to PC5	I/O	(Port C) Lower 6 bits are I/O ports; I/O can be set in a unit of single bits. Upper 2bits are output port and large current (12mA) N-channel open drain output. Upper 2 bits are medium voltage drive (12V), lower 6 bits are 5V drive. (8 pins)		
PC6 to PC7	Output			
PD0/ $\overline{\text{INT2}}$	I/O/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sink current. (8 pins)	External interruption request input. Active at the falling edge.	
PD1/ $\overline{\text{SCK}}$	I/O/I/O		Serial clock I/O.	
PD2/SO	I/O/Output		Serial data output.	
PD3/SI	I/O/Input		Serial data input.	
PD4 to PD5	I/O			
PD6/RMC	I/O/Input		Remote control reception circuit input.	
PD7/ $\overline{\text{EC}}$	I/O/Input		External event input for timer/counter.	
PE0/TO/ADJ	I/O/Output/ Output		Rectangular wave output for 8-bit timer/counter.	32kHz oscillation frequency dividing output.
PE1	I/O	(Port E) Bits 0 and 1 are I/O port; I/O can be set in a unit of single. Bits 2 and 3 are input port. Bits 4, 5 and 6 are output port. (7 pins)		
PE2/TEX/ $\overline{\text{INT0}}$	Input/Input/ Input		Connects a crystal for 32kHz timer/counter clock oscillation. When used as an event counter, input to TEX pin and leave TX pin open.	External interruption request input. Active at the falling edge
PE3/TX	Input/Output			
PE4 to PE6	Output			

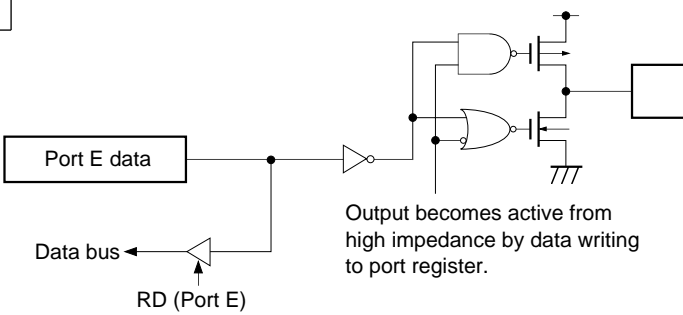
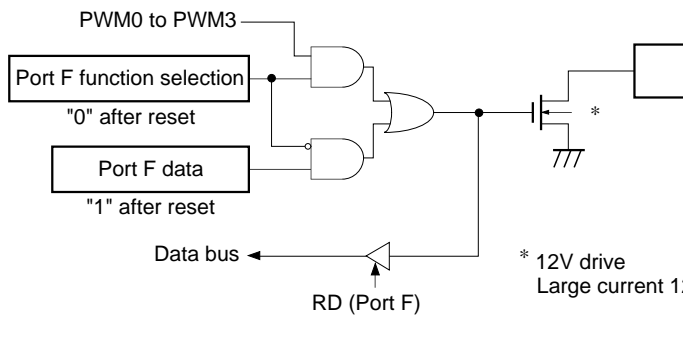
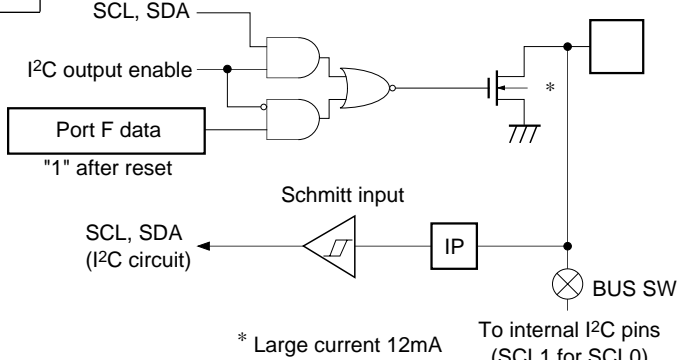
Symbol	I/O	Description	
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port and large current (12mA) N-channel open drain output. Lower 4 bits are medium voltage drive (12V); upper 4 bits are 5V drive. (8 pins)	8-bit PWM output. (4 pins)
PF4/SCL0 to PF5/SCL1	Output/I/O		I <sup>2</sup> C bus interface transfer clock I/O. (2 pins)
PF6/SDA0 to PF7/SDA1	Output/I/O		I <sup>2</sup> C bus interface transfer data I/O. (2 pins)
PG3 to PG6	I/O	(Port G) 5-bit I/O port. I/O can be set in a unit of single bits. (5 pins)	
PG7/ $\overline{\text{INT1}}$	I/O/Input	External interruption request input. Active at the falling edge.	
EXTAL	Input	Connects a crystal for system clock oscillation. When a clock is supplied externally, input to EXTAL pin and input a reversed phase clock to XTAL pin.	
XTAL	Output		
$\overline{\text{RST}}$	Input	System reset; active at Low level.	
NC		No connected. Connect this pin to V <sub>DD</sub> under normal operation.	
V <sub>DD</sub>		Positive power supply.	
V <sub>SS</sub>		GND. Connect two V <sub>SS</sub> pins to GND.	

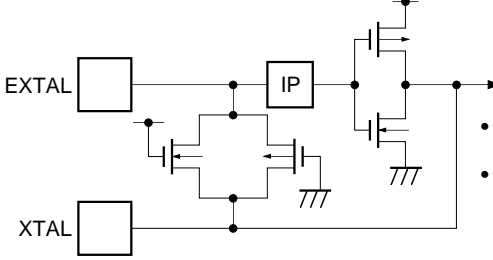
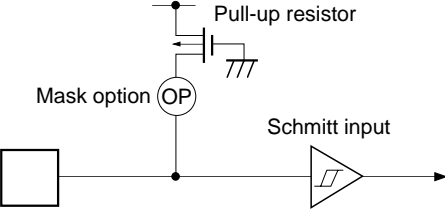
Input/Output Circuit Formats for Pins

Pin	Circuit format	After reset
<p>PA0/AN0 to PA5/AN5</p> <p>6 pins</p>	<p>Port A</p> <p>Port A data</p> <p>Port A direction "0" after reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A function selection "0" after reset A/D converter</p> <p>Input multiplexer</p> <p>IP</p> <p>Input protection circuit</p>	<p>Hi-Z</p>
<p>PA6 PA7</p> <p>2 pins</p>	<p>Port A</p> <p>Port A data</p> <p>Port A direction "0" after reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Schmitt input</p> <p>IP</p>	<p>Hi-Z</p>
<p>PB0 to PB7 PC0 to PC5 PG3 to PG6 PG7/INT1</p> <p>19 pins</p>	<p>Port B</p> <p>Port C</p> <p>Port G</p> <p>Ports B, C, G data</p> <p>Ports B, C, G direction "0" after reset</p> <p>Data bus</p> <p>RD (Ports B, C, G)</p> <p>Schmitt input only for PG7</p> <p>IP</p> <p>INT1</p>	<p>Hi-Z</p>
<p>PC6 PC7</p> <p>2 pins</p>	<p>Port C</p> <p>Port C data</p> <p>Data bus</p> <p>RD (Port C)</p> <p>* 12V drive Large current 12mA</p>	<p>Hi-Z</p>

Pin	Circuit format	After reset
<p>PD0/<math>\overline{\text{INT2}}</math>                      PD3/SI                      PD6/RMC                      PD7/<math>\overline{\text{EC}}</math></p> <p>4 pins</p>	<p>Port D</p>  <p>* Large current 12mA</p>	<p>Hi-Z</p>
<p>PD1/<math>\overline{\text{SCK}}</math>                      PD2/SO</p> <p>2 pins</p>	<p>Port D</p>  <p>* Large current 12mA</p>	<p>Hi-Z</p>
<p>PD4                      PD5</p> <p>2 pins</p>	<p>Port D</p>  <p>* Large current 12mA</p>	<p>Hi-Z</p>

Pin	Circuit format	After reset
<p>PE0/TO/ADJ</p> <p>1 pin</p>	<p>Port E</p> <p>Internal reset signal</p> <p>Port E data "1" after reset</p> <p>TO*1</p> <p>ADJ16K*1</p> <p>ADJ2K*1</p> <p>MPX</p> <p>00</p> <p>01</p> <p>10</p> <p>11</p> <p>Port E function selection (upper)</p> <p>Port E function selection (lower)</p> <p>"00" after reset</p> <p>Port E direction "1" after reset</p> <p>Data bus</p> <p>RD (Port E)</p> <p>*1 ADJ signals are frequency dividing outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.</p> <p>*2 Pull-up transistor approx. 150kΩ</p>	<p>High level (with the resistor of pull-up transistor ON when reset)</p>
<p>PE1</p> <p>1 pin</p>	<p>Port E</p> <p>Port E data "1" after reset</p> <p>Port E direction "1" after reset</p> <p>Data bus</p> <p>RD (Port E)</p>	<p>High level</p>
<p>PE2/TEX/<math>\overline{\text{INT0}}</math> PE3/TX</p> <p>2 pins</p>	<p>Port E</p> <p>32kHz oscillation circuit control</p> <p>"1" after reset Schmitt input</p> <p><math>\overline{\text{INT0}}</math></p> <p>Data bus</p> <p>RD (Port E)</p> <p>Data bus</p> <p>RD (Port E)</p> <p>Schmitt input</p> <p>Clock input</p> <p>PE2/TEX/<math>\overline{\text{INT0}}</math></p> <p>IP</p> <p>PE3/TX</p> <p>IP</p>	<p>Oscillation stop Port input</p>

Pin	Circuit format	After reset
<p>PE4 PE5 PE6</p> <p>3 pins</p>	<p>Port E</p>  <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>PF0/PWM0 to PF3/PWM3</p> <p>4 pins</p>	<p>Port F</p>  <p>* 12V drive Large current 12mA</p>	<p>Hi-Z</p>
<p>PF4/SCL0 PF5/SCL1 PF6/SDA0 PF7/SDA1</p> <p>4 pins</p>	<p>Port F</p>  <p>* Large current 12mA</p> <p>To internal I<sup>2</sup>C pins (SCL1 for SCL0)</p>	<p>Hi-Z</p>

Pin	Circuit format	After reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Diagram shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop. (This device does not enter the stop mode.)</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>		<p>Low level (when reset)</p>

**Absolute Maximum Ratings**

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0*1	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0*1	V	
Medium drive output voltage	V <sub>OUTP</sub>	-0.3 to +15.0	V	
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	∑I <sub>OH</sub>	-50	mA	Total of all output pins
Low level output current	I <sub>OL</sub>	15	mA	Ports excluding large current output (value per pin)
	I <sub>OLC</sub>	20	mA	Large current output ports (value per pin*2)
Low level total output current	∑I <sub>OL</sub>	130	mA	Total of all output pins
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	1000	mW	SDIP-64P-01
		600	mW	QFP-64P-L01

\*1 V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*2 The large current output port is Port C (PC6, PC7), Port D (PD) and Port F (PF).

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

**Recommended Operating Conditions**

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clocks
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or sleep mode
		2.7	5.5	V	Guaranteed operation range for TEX
		—	—	V	Guaranteed data hold range for stop*1
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*2
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	*3
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> +0.3	V	EXTAL pin*4, TEX pin*5
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*2
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	*3
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*4, TEX pin*5
Operating temperature	T <sub>opr</sub>	-20	+75	°C	

\*1 This device does not enter the stop mode.

\*2 PA0 to PA5, PB0 to PB7, PC0 to PC5, PD2, PE0, PE1, PE3, PG3 to PG6, SCL0, SCL1, SDA0, SDA1 pins

\*3 PA6, PA7, INT2, SCK, SI, PD4, PD5, RMC, EC, INT0, INT1, RST pins

\*4 Specifies only during external clock input.

\*5 Specifies only during external event count input.

Electrical Characteristics

DC characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit				
High level output voltage	VOH	PA, PB, PC0 to PC5, PD, PE0 to PE1, PE4 to PE6, PG	VDD = 4.5V, IOH = -0.5mA	4.0			V				
			VDD = 4.5V, IOH = -1.2mA	3.5			V				
Low level output voltage	VOL	PA to PD, PE0 to PE1, PE4 to PE6, PF0 to PF3, PG	VDD = 4.5V, IOL = 1.8mA			0.4	V				
			VDD = 4.5V, IOL = 3.6mA			0.6	V				
		PC6, PC7, PD, PF	VDD = 4.5V, IOL = 12.0mA			1.5	V				
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	VDD = 4.5V, IOL = 3.0mA			0.4	V				
			VDD = 4.5V, IOL = 4.0mA			0.6	V				
Input current	I <sub>IHE</sub>	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA				
	I <sub>I<sub>LE</sub></sub>							VDD = 5.5V, VIL = 0.4V	-0.5	-40	μA
	I <sub>IHT</sub>	TEX	VDD = 5.5V, VIH = 5.5V	0.1		10	μA				
	I <sub>ILT</sub>							VDD = 5.5V, VIL = 0.4V	-0.1	-10	μA
	I <sub>ILR</sub>										
I/O leakage current	I <sub>Iz</sub>	PA to PE, PG, RST*1	VDD = 5.5V, VI = 0, 5.5V			±10	μA				
Open drain I/O leakage current (in N-ch Tr off state)	I <sub>LOH</sub>	PC6, PC7, PF0 to PF3	VDD = 5.5V, VOH = 12.0V			50	μA				
		PF4 to PF7	VDD = 5.5V, VOH = 5.5V			10	μA				
I <sup>2</sup> C bus switch connection impedance (in output Tr off state)	R <sub>Bs</sub>	SCL0: SCL1 SDA0: SDA1	VDD = 4.5V VSCL0 = VSCL1 = 2.25V VSDA0 = VSDA1 = 2.25V			120	Ω				
Supply current*2	I <sub>DD1</sub>	VDD	1/2 frequency dividing clock operation	18	28	mA					
			VDD = 5.5V, 16MHz crystal oscillation (C1 = C2 = 15pF)								
	I <sub>DD2</sub>		VDD = 3.3V, 32MHz crystal oscillation (C1 = C2 = 47pF)	30	80	μA					
	I <sub>DDS1</sub>		Sleep mode	1.2	2.1	mA					
			VDD = 5.5V, 16MHz crystal oscillation (C1 = C2 = 15pF)								
I <sub>DDS2</sub>	VDD = 3.3V, 32MHz crystal oscillation (C1 = C2 = 47pF)	12	35	μA							
I <sub>DDS3</sub>	Stop mode*3 VDD = 5.5V, termination of 16MHz and 32MHz oscillation	—	—	—	μA						

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	PA to PD, PE0 to PE3, PF4 to PF7, PG3 to PG7, EXTAL, TEX, $\overline{\text{RST}}$	Clock 1MHz 0V for no measured pins		10	20	μF

\*1 For  $\overline{\text{RST}}$  pin, specifies the input current when pull-up resistor is selected, and specifies the leakage current when non-resistor is selected.

\*2 When all output pins are left open.

\*3 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	8		16	MHz
System clock input pulse width	t <sub>XL</sub> , t <sub>XH</sub>	EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise and fall times	t <sub>CR</sub> , t <sub>CF</sub>	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t <sub>EH</sub> , t <sub>EL</sub>	$\overline{EC}$	Fig. 3	4tsys*1			ns
Event count input clock rise and fall times	t <sub>ER</sub> , t <sub>EF</sub>	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	fc	TEX TX	VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied conditions)		32.768		kHz
Event count input clock input pulse width	t <sub>TL</sub> , t <sub>TH</sub>	TEX	Fig. 3	10			μs
Event count input clock rise and fall times	t <sub>TR</sub> , t <sub>TF</sub>	TEX	Fig. 3			20	ms

\*1 Indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

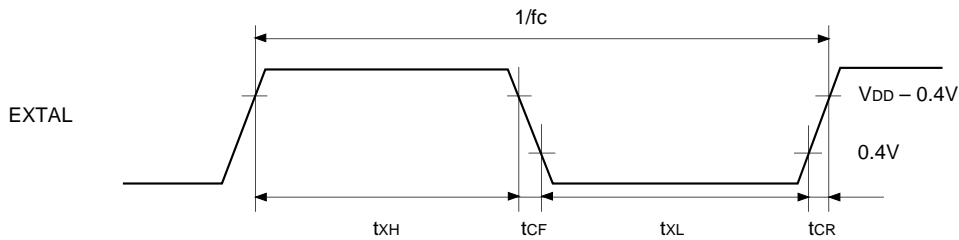


Fig. 1. Clock timing

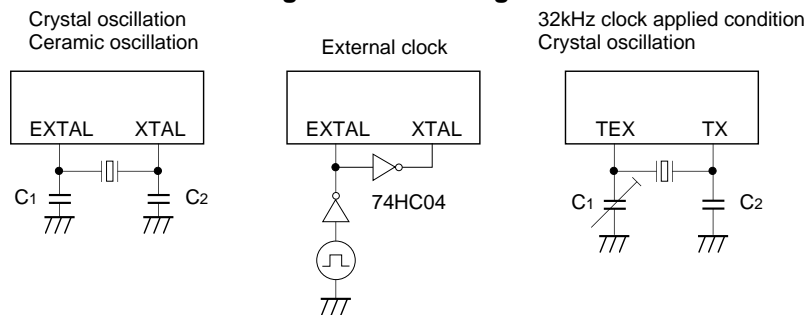


Fig.2. Clock applied conditions

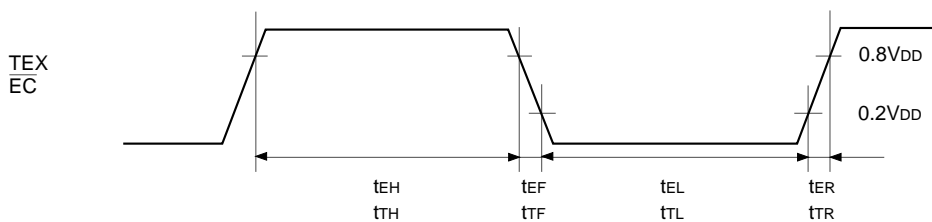


Fig. 3. Event count clock timing

(2) Serial transfer

(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ High and Low level width	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$ input mode	400		ns
			$\overline{\text{SCK}}$ output mode	4000/fc - 50		ns
SI input setup time (for $\overline{\text{SCK}} \uparrow$ )	$t_{\text{SIK}}$	SI	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI hold time (for $\overline{\text{SCK}} \uparrow$ )	$t_{\text{KSI}}$	SI	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	$t_{\text{KSO}}$	SO	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

**Note)** The load of  $\overline{\text{SCK}}$  output mode and SO output delay time is 50pF + 1TTL.

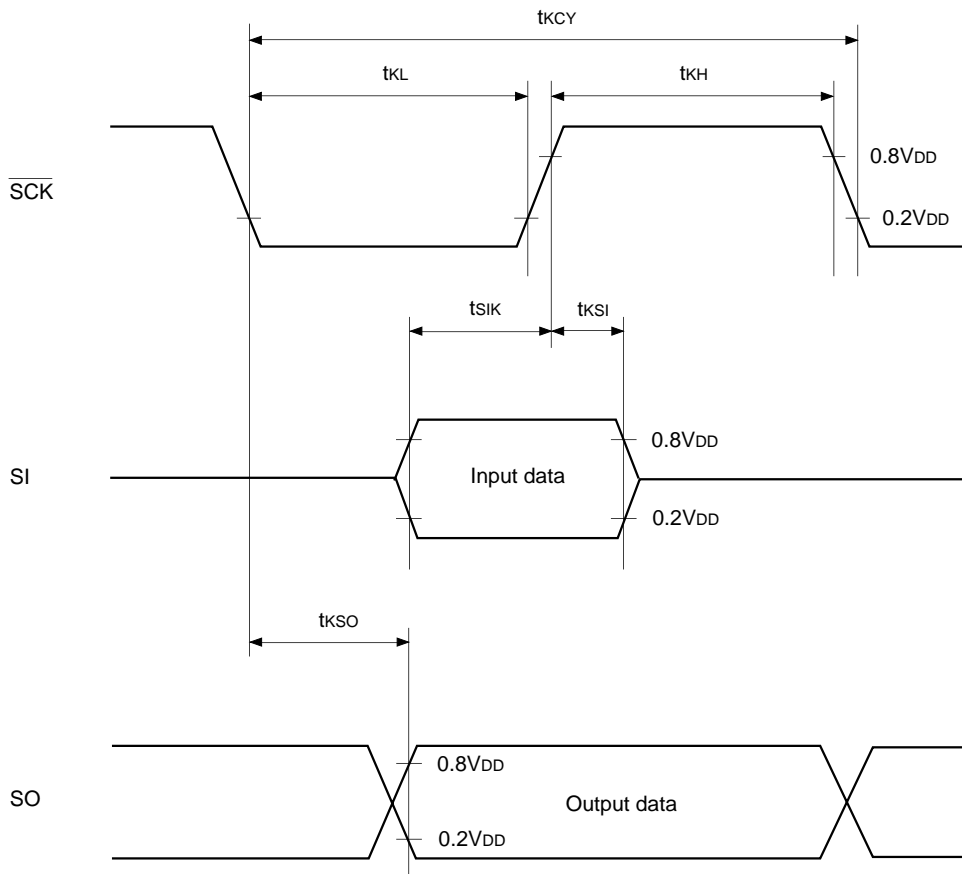
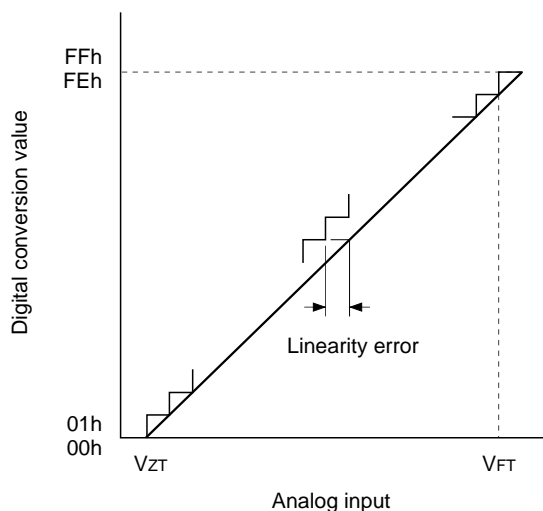


Fig. 4. Serial transfer timing

**(3) A/D converter characteristics**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = 0\text{V}$			$\pm 3$	LSB
Zero transition voltage	$V_{ZT}^{*1}$			-10	10	70	mV
Full-scale transition voltage	$V_{FT}^{*2}$			4910	4970	5030	mV
Conversion time	$t_{CONV}$			$26/f_{ADC}^{*3}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$6/f_{ADC}^{*3}$			$\mu\text{s}$
Analog input voltage	$V_{IAN}$	AN0 to AN5		0		$V_{DD}$	V



\*1  $V_{ZT}$ : Value at which the digital conversion value changes from 00h to 01h and vice versa.

\*2  $V_{FT}$ : Value at which the digital conversion value changes from FEh to FFh and vice versa.

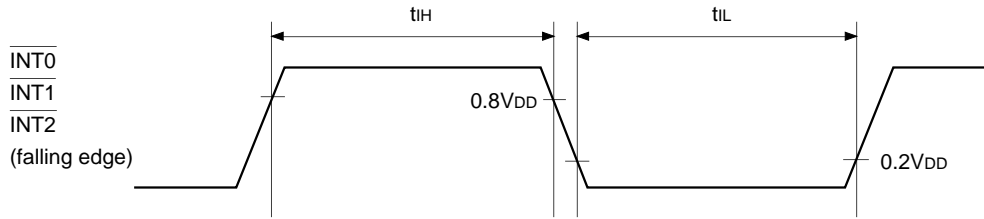
\*3  $f_{ADC}$  indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F6h):

$$f_{ADC} = f_c \text{ (CKS = "0")}, f_c/2 \text{ (CKS = "1")}$$

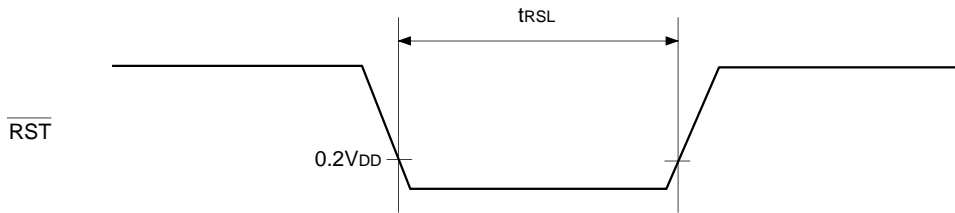
**Fig. 5. Definitions of A/D converter terms**

**(4) Interruption, reset input** (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High, Low level width	t <sub>IH</sub> t <sub>IL</sub>	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$		1		μs
Reset input Low level width	t <sub>RSL</sub>	$\overline{\text{RST}}$		32/fc		μs



**Fig. 6. Interruption input timing**



**Fig. 7.  $\overline{\text{RST}}$  input timing**

(5) I<sup>2</sup>C bus timing

(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCL clock frequency	f <sub>SCL</sub>	SCL		0	100	kHz
Bus-free time before starting transfer	t <sub>BUF</sub>	SDA, SCL		4.7		μs
Hold time for starting transfer	t <sub>HD; STA</sub>	SDA, SCL		4.0		μs
Clock Low level width	t <sub>LOW</sub>	SCL		4.7		μs
Clock High level width	t <sub>HIGH</sub>	SCL		4.0		μs
Setup time for repeated transfers	t <sub>SU; STA</sub>	SDA, SCL		4.7		μs
Data hold time	t <sub>HD; DAT</sub>	SDA, SCL		0*1		μs
Data setup time	t <sub>SU; DAT</sub>	SDA, SCL		250		ns
SDA, SCL rise time	t <sub>R</sub>	SDA, SCL			1	μs
SDA, SCL fall time	t <sub>F</sub>	SDA, SCL			300	ns
Setup time for transfer completion	t <sub>SU; STO</sub>	SDA, SCL		4.7		μs

\*1 The data hold time should be 300ns or more because the SCL rise time (300ns Max.) is not included in it.

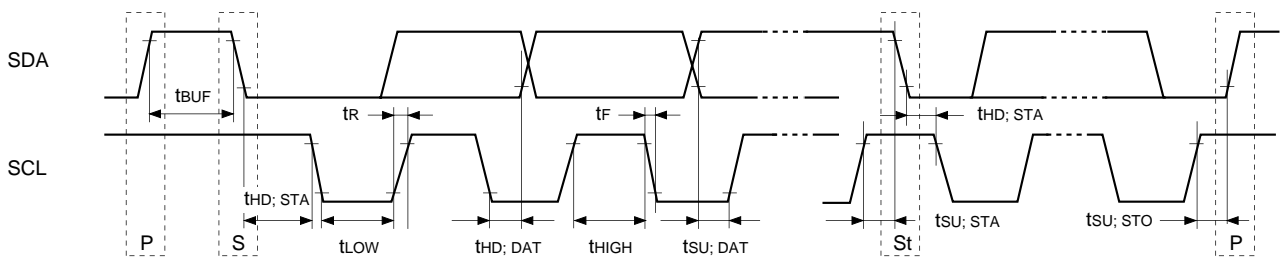


Fig. 8. I<sup>2</sup>C bus transfer timing

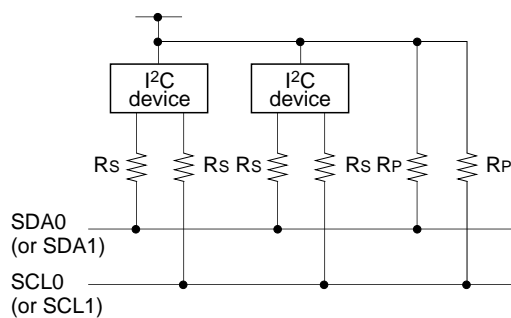


Fig. 9. I<sup>2</sup>C device recommended circuit

- A pull-up resistor (Rp) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce the spike noise caused by CRT flashover.

Appendix

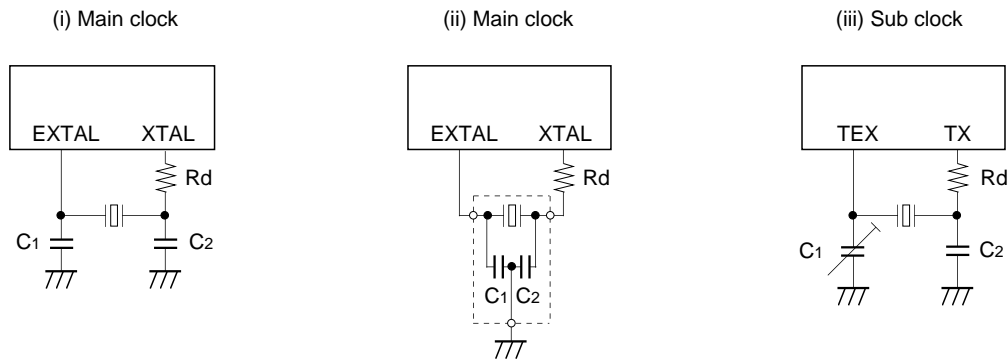


Fig. 10. Recommended oscillation circuit

Manufacture	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd ( $\Omega$ )	Circuit example
MURATA MFG CO., LTD.	CSA10.0MTZ	10.0	30	30	0* <sup>1</sup>	(i)
	CSA12.0MTZ	12.0				
	CSA16.00MXZ040	16.0	5	5		
	CST10.0MTW*	10.0	30	30		(ii)
	CST12.0MTW*	12.0				
	CST16.00MXW0C1*	16.0				
RIVER ELETEC CORPORATION	HC-49/U03	8.0	18	18	330* <sup>1</sup>	(i)
		12.0	12	12		
		16.0	10	10		
KINSEKI LTD.	HC-49/U (-S)	8.0	10	10	0* <sup>1</sup>	
		12.0	5	5		
		16.0	Open	Open		
	P3	32.768kHz	30	33	120k	(iii)

\*Models with an asterisk have the built-in ground capacitance (C1, C2).

\*<sup>1</sup> The series resistor for XTAL ( $R_d = 500\Omega$  or less) can reduce the effect of the noise caused by the electrostatic discharge.

Mask Option Table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

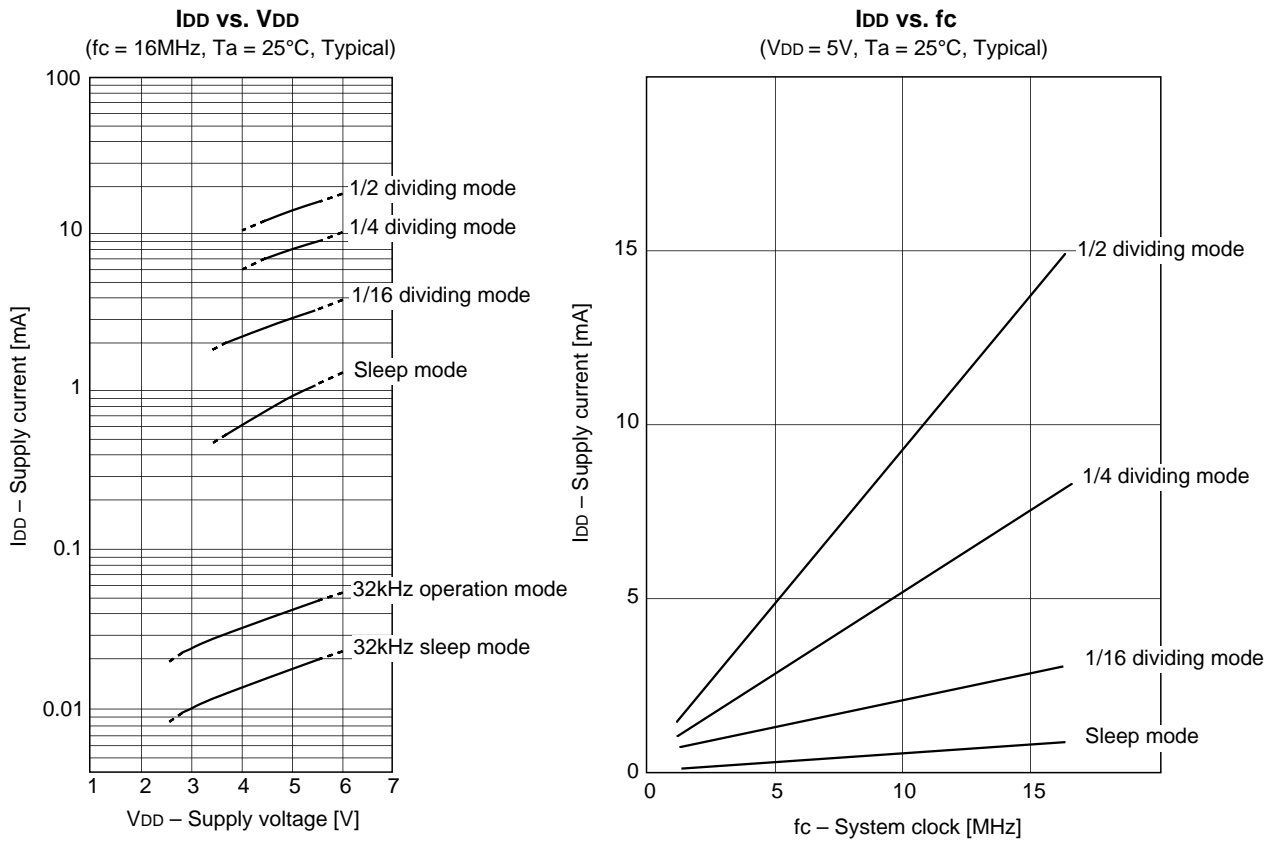
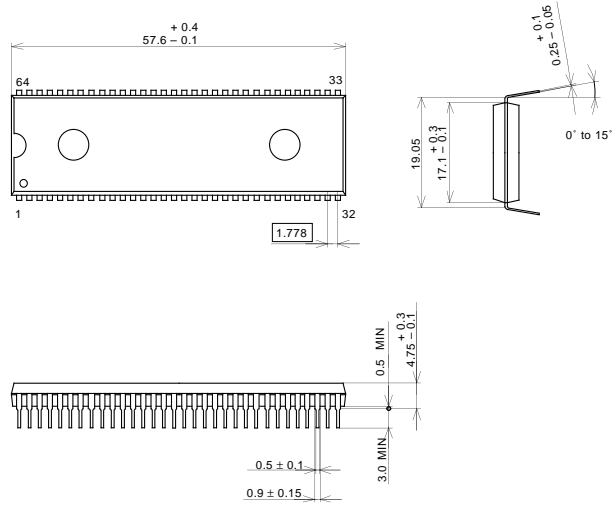


Fig. 11. Characteristic curves

Package Outline

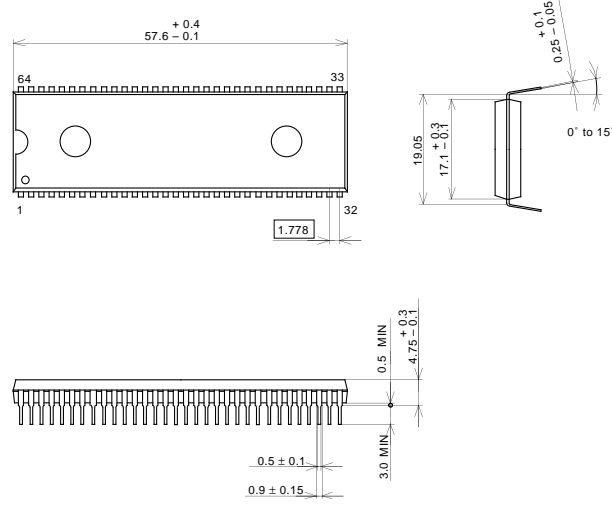
Unit: mm

64PIN SDIP (PLASTIC)



SONY CODE		SDIP-64P-01	
EIAJ CODE	P-SDIP64-17.1x57.6-1.778	PACKAGE MATERIAL	EPOXY RESIN
JEDEC CODE		LEAD TREATMENT	SOLDER PLATING
		LEAD MATERIAL	42/COPPER ALLOY
		PACKAGE MASS	8.6g

64PIN SDIP (PLASTIC)



SONY CODE		SDIP-64P-01	
EIAJ CODE	P-SDIP64-17.1x57.6-1.778	PACKAGE MATERIAL	EPOXY RESIN
JEDEC CODE		LEAD TREATMENT	SOLDER PLATING
		LEAD MATERIAL	42/COPPER ALLOY
		PACKAGE MASS	8.6g

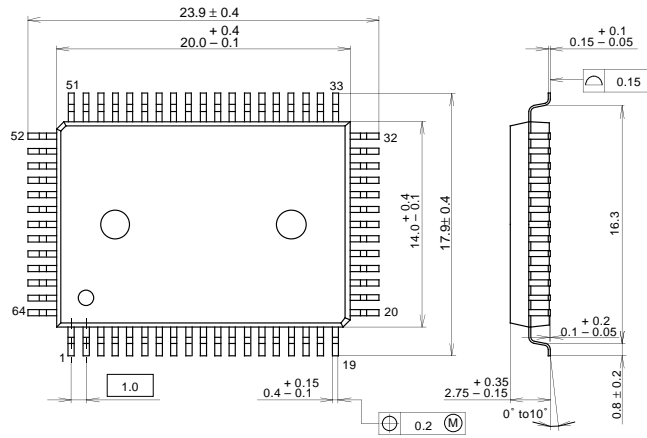
**LEAD SPECIFICATIONS**

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm

Package Outline

Unit: mm

64PIN QFP (PLASTIC)

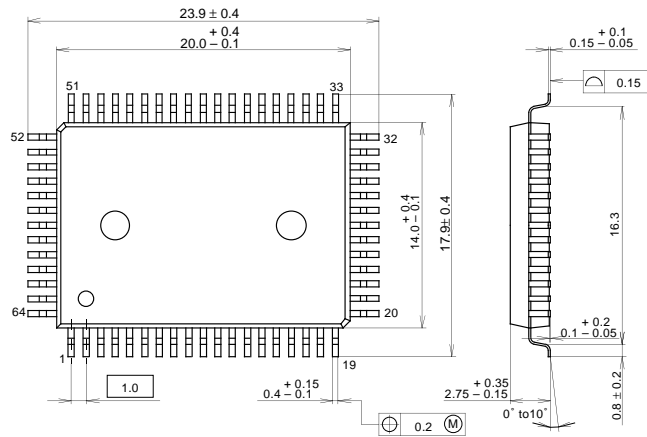


PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

64PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm



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