

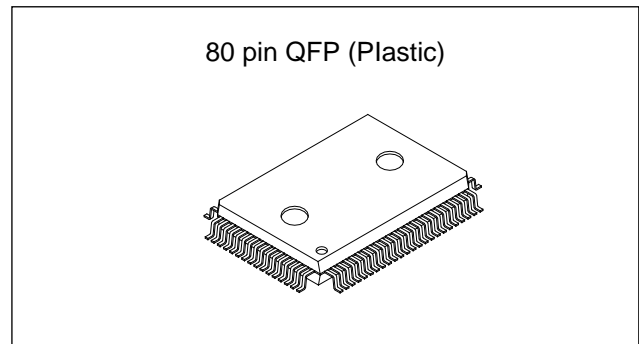
## CMOS 8-bit Single-chip Microcomputer

### Description

The CXP861P16 is a highly integrated CMOS 8-bit single-chip microcomputer which is mainly composed of an 8-bit CPU, PROM, RAM and I/O ports. This microcomputer features many other high-performance circuits in a single-chip CMOS design, including an A/D converter, clock synchronized serial interface, UART, stepping motor controller, PWM generator, 16-bit timer/counter, and watchdog timer.

Also, the CXP861P16 provides the power-on reset function as well as the sleep/stop function which enables to lower power consumption.

This IC is the PROM-incorporated version of the CXP86116 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.



### Structure

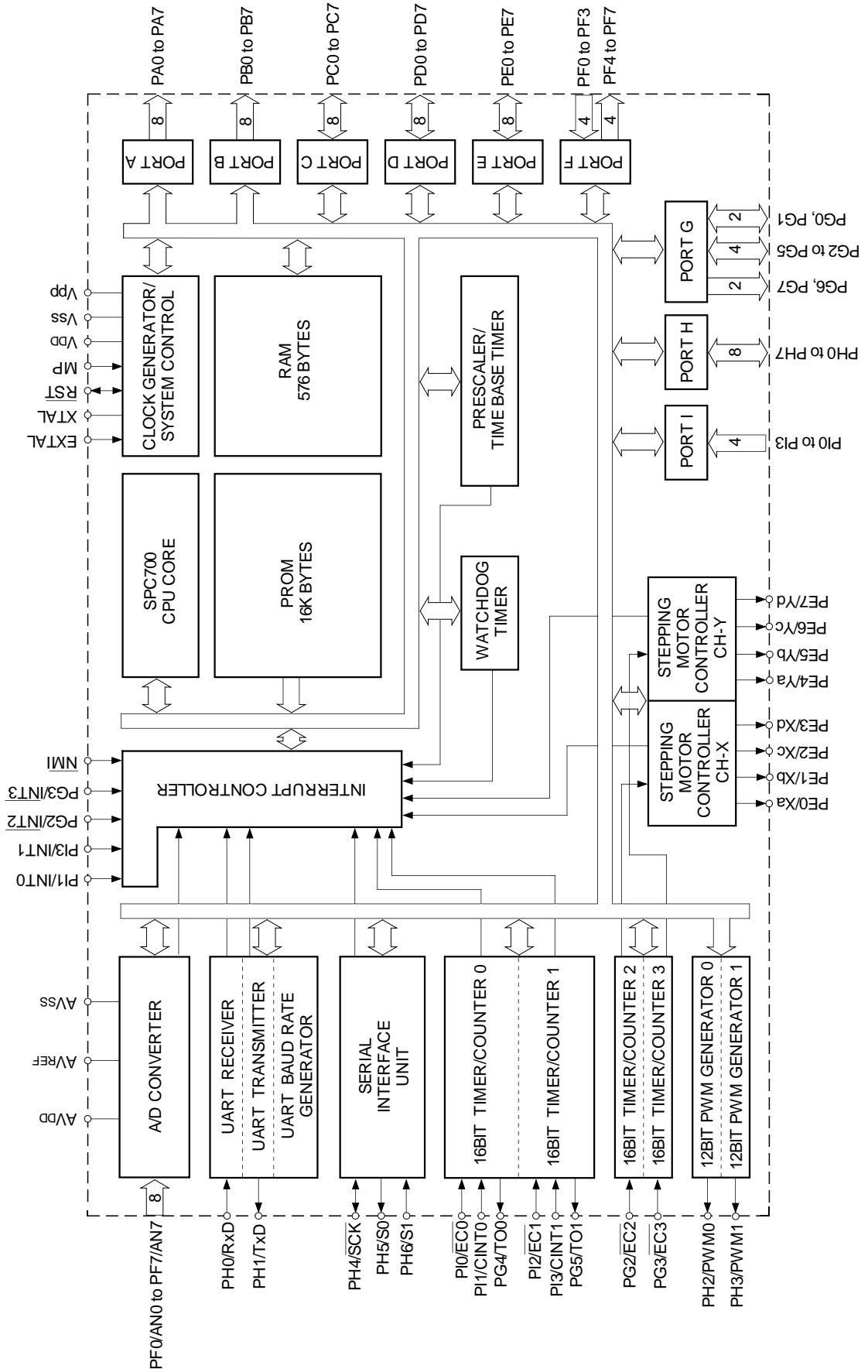
Silicon gate CMOS IC

### Features

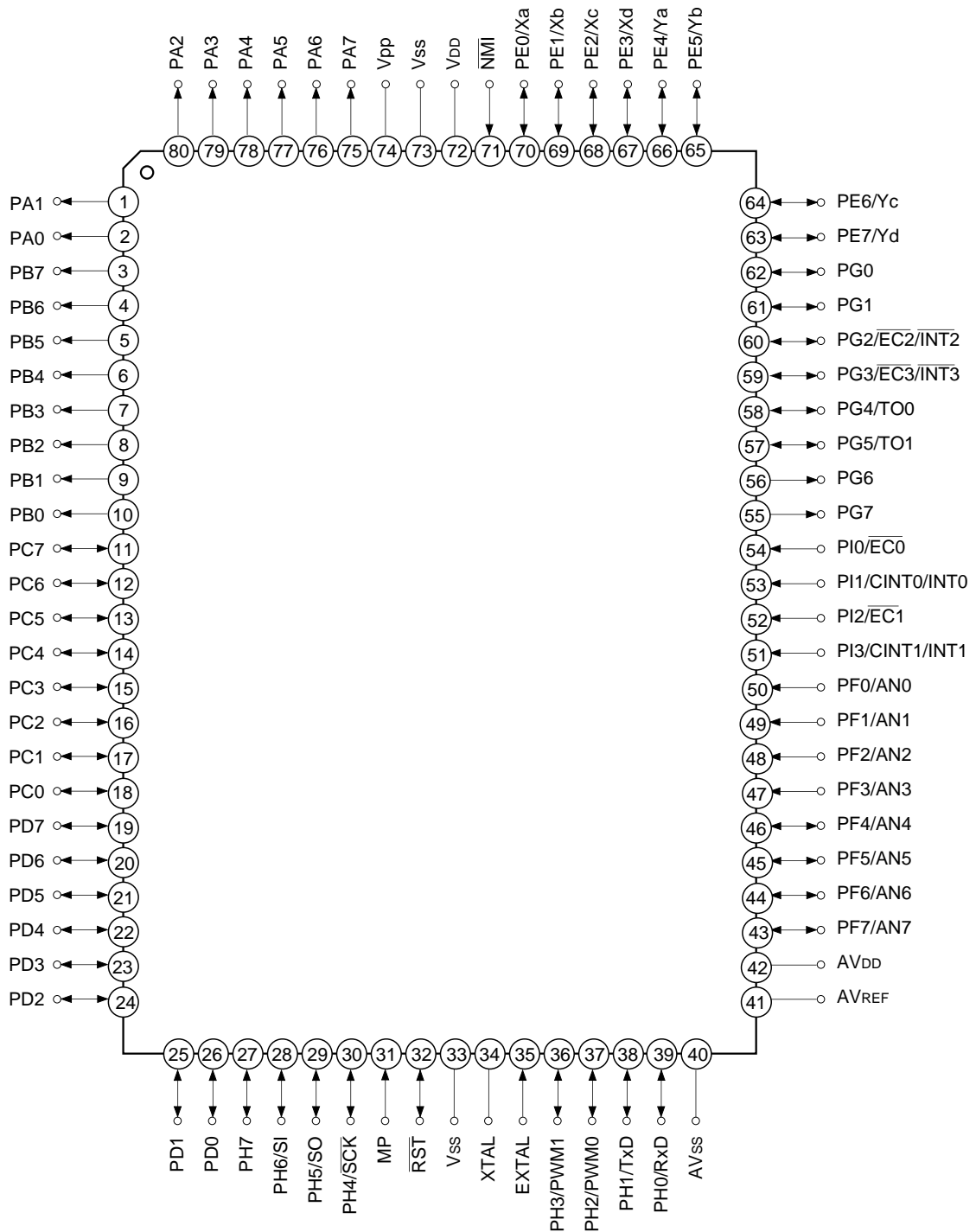
- Instruction set which supports a wide array of data types 213 types
  - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation
- Minimum instruction cycle      During operation 400ns/instruction 10MHz
- Incorporated PROM capacity    16K bytes
- Incorporated RAM capacity      576 bytes
- Peripheral functions
  - A/D converter                    8-bit, 8-channel, successive comparison type (conversion time: 32 $\mu$ s at 10MHz)
  - Serial interface                Universal Asynchronous Receiver Transmitter (baud-rate generator incorporated)  
8-bit clock synchronized type
  - Stepping motor controller    2-channel stepping motor excitation output
  - PWM output                     2-channel 12-bit output
  - Timer                              2-channel 16-bit capture timer/counter  
2-channel 16-bit timer/counter (step rate generation function incorporated)  
19-bit time-base timer
  - Watchdog timer
- Interrupts                            17 factors, 15 vectors, multiple interrupt processing
- Standby mode                      SLEEP/STOP
- Package                             80-pin plastic QFP

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Block Diagram



Pin Configuration (Top View)



- Note)**
1. Vpp (Pin 74) is always connected to VDD.
  2. Vss (Pins 33 and 73) are both connected to GND.
  3. MP (Pin 31) is always connected to Vss.

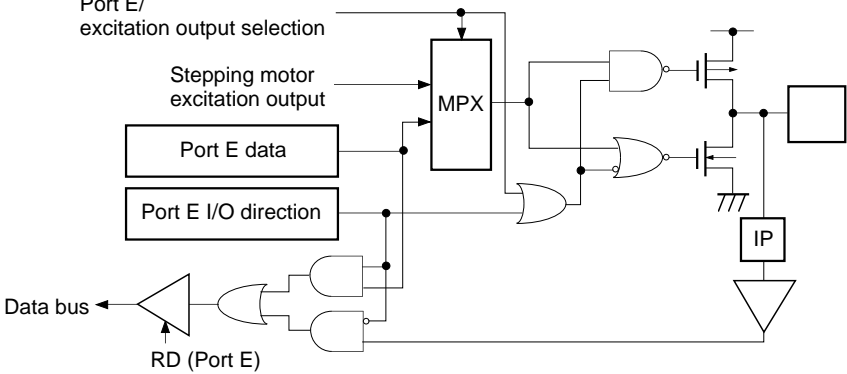
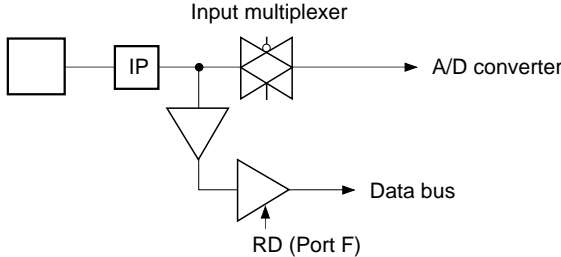
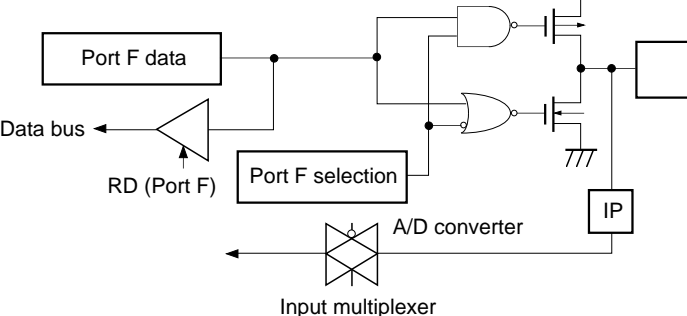
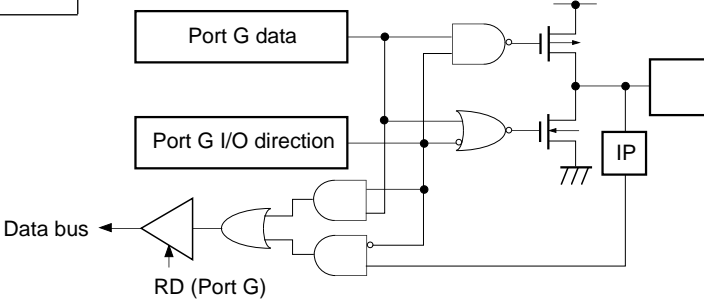
Pin Description

Symbol	I/O	Description		
PA0 to PA7	Output	(Port A) 8-bit output port. 12mA sink current can be driven. (8 pins)		
PB0 to PB7	Output	(Port B) 8-bit output port. (8 pins)		
PC0 to PC7	I/O	(Port C) 8-bit I/O port. Enable to specify input/output by 4-bit unit. (8 pins)		
PD0 to PD7	I/O	(Port D) 8-bit I/O port. Enable to specify input/output by 4-bit unit. (8 pins)		
PE0/Xa to PE3/Xd	I/O/output	(Port E) 8-bit I/O port. I/O can be selected in a unit of 4 bits. (8 pins)	Output for stepping motor control circuit CH-X. (4 pins)	
PE4/Ya to PE7/Yd	I/O/output		Output for stepping motor control circuit CH-Y. (4 pins)	
PF0/AN0 to PF3/AN3	Input/input	(Port F) Input port for the lower 4 bits; output port for the upper 4 bits. (8 pins)	Analog input to A/D converter. (8 pins)	
PF4/AN4 to PF7/AN7	Output/input			
PG0 PG1	I/O	(Port G) I/O port for the lower 6 bits; output port for the upper 2 bits. Enable to specify input/output by bit unit. (8 pins)		
PG2/EC2/INT2 PG3/EC3/INT3	I/O/input/input		External event input for timer/counter 2 and 3.	Input for external interrupt request.
PG4/TO0 PG5/TO1	I/O/output		Output for capture and timer/counter. (2 pins)	
PG6 PG7	Output			
PH0/RxD	I/O/input	(Port H) 8-bit I/O port. Enable to specify input/output by bit unit. (8 pins)	Input for UART reception data.	
PH1/TxD	I/O/output		Output for UART transmission data.	
PH2/PWM0	I/O/output		PWM output. (2 pins)	
PH3/PWM1	I/O/output			
PH4/SCK	I/O/I/O		I/O for serial clock.	
PH5/SO	I/O/output		Output for serial data.	
PH6/SI	I/O/input		Input for serial data.	
PH7	I/O			

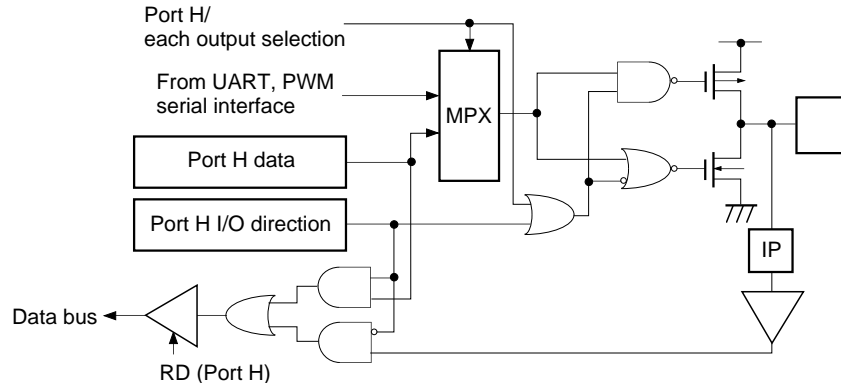
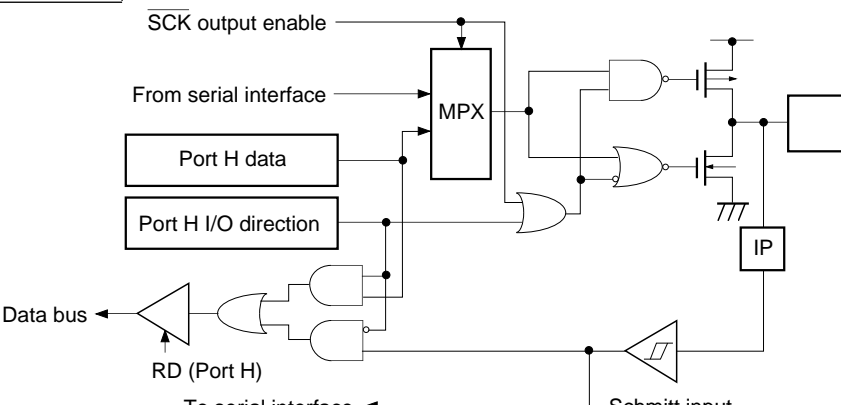
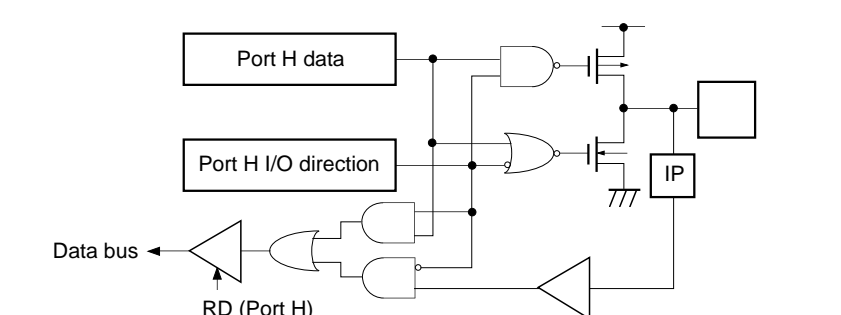
Symbol	I/O	Description	
PI0/ $\overline{EC0}$	Input/input/input	(Port I) 4-bit input port. (4 pins)	External event input for timer/counter 0.
PI1/CINT0 / INT0			Capture input for timer/counter 0.      Input for external interruption request.
PI2/ $\overline{EC1}$			External event input for timer/counter 1.
PI3/CINT1/ INT1			Capture input for timer/counter 1.      Input for external interruption request.
$\overline{NMI}$	Input	Non-maskable interruption request for active at falling edge.	
EXTAL	Input	Crystal connection for system clock oscillation. Input the clock to EXTAL pin and at the same time input the clock with reversed phase to XTAL pin when clock is input externally.	
XTAL	Output		
$\overline{RST}$	I/O	System reset for active at low level. $\overline{RST}$ pin becomes I/O pin, and outputs low level at the power on with power-on reset function executed. (mask option)	
MP	Input	Always connect to Vss.	
AVDD		Positive power supply for A/D converter.	
AVREF	Input	Reference supply voltage input for A/D converter.	
AVss		GND for A/D converter.	
VDD		Positive power supply.	
Vpp		Positive power supply for built-in PROM writing. Connect to VDD for normal operation.	
Vss		GND. Connect both of Vss to GND.	

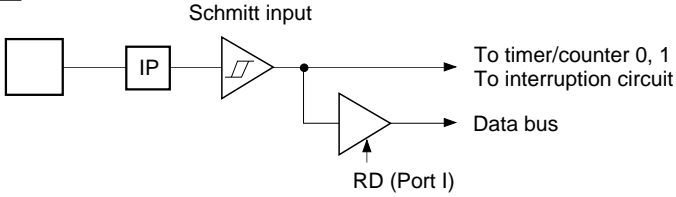
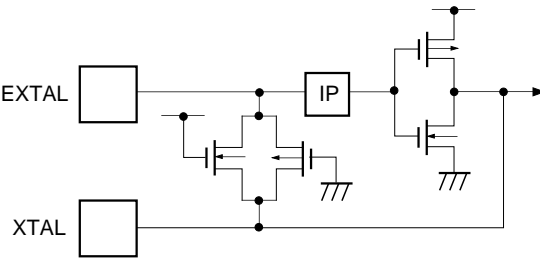
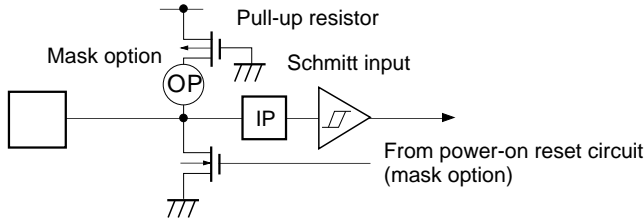
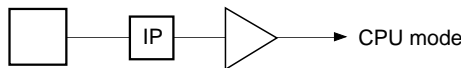
I/O Circuit Formats for Pins

Pin	Circuit format	When reset
Port A Port B PA0 to PA7 PB0 to PB7 16 pins		Hi-Z
Port C PC0 to PC7 8 pins		Hi-Z
Port D PD0 to PD5 6 pins		Hi-Z
Port D PD6 PD7 2 pins		Hi-Z

Pin	Circuit format	When reset
<p>PE0/Xa PE1/Xb PE2/Xc PE3/Xd PE4/Ya PE5/Yb PE6/Yc PE7/Yd</p> <p>8 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PF0/AN0 to PF3/AN3</p> <p>4 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PF4/AN4 to PF7/AN7</p> <p>4 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PG0 PG1</p> <p>2 pins</p>	<p>Port G</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PG2/<math>\overline{EC2}</math>/<math>\overline{INT2}</math> PG3/<math>\overline{EC3}</math>/<math>\overline{INT3}</math></p> <p>2 pins</p>	<p>Port G</p> <p>Port G data</p> <p>Port G I/O direction</p> <p>Data bus</p> <p>RD (Port G)</p> <p>To timer/counter 2, 3</p> <p>To interruption circuit</p> <p>Schmitt input</p> <p>IP</p>	<p>Hi-Z</p>
<p>PG4/TO0 PG5/TO1</p> <p>2 pins</p>	<p>Port G</p> <p>Port G/ timer output selection</p> <p>From timer/counter 0, 1</p> <p>MPX</p> <p>Port G data</p> <p>Port G I/O direction</p> <p>Data bus</p> <p>RD (Port G)</p> <p>IP</p>	<p>H level</p>
<p>PG6 PG7</p> <p>2 pins</p>	<p>Port G</p> <p>Port G data</p> <p>Data bus</p> <p>RD (Port G)</p>	<p>Hi-Z</p>
<p>PH0/RxD PH6/SI</p> <p>2 pins</p>	<p>Port H</p> <p>Port H data</p> <p>Port H I/O direction</p> <p>Data bus</p> <p>RD (Port H)</p> <p>To UART</p> <p>To serial interface</p> <p>Schmitt input</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PH1/TxD PH2/PWM0 PH3/PWM1 PH5/SO</p> <p>4 pins</p>	<p>Port H</p> 	<p>Hi-Z</p>
<p>PH4/<math>\overline{\text{SCK}}</math></p> <p>1 pin</p>	<p>Port H</p> 	<p>Hi-Z</p>
<p>PH7</p> <p>1 pin</p>	<p>Port H</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p> <math>\overline{PI0}/\overline{EC0}</math>  <math>PI1/CINT0/INT0</math>  <math>PI2/\overline{EC1}</math>  <math>PI3/CINT1/INT1</math> </p> <p>4 pins</p>	<p>Port I</p> 	<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Diagram shows the circuit configuration during oscillation.</li> <li>• Feedback resistor is removed during stop.</li> </ul>	<p>Oscillation</p>
<p><math>\overline{RST}</math></p> <p>1 pin</p>		<p>L level</p>
<p>MP</p> <p>1 pin</p>		<p>Hi-Z</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V)

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	V <sub>pp</sub>	-0.3 to +13.0	V	Incorporated PROM
	AV <sub>DD</sub>	AV <sub>SS</sub> to +7.0* <sup>1</sup>	V	
	AV <sub>SS</sub>	-0.3 to +0.3	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>2</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>2</sup>	V	
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	∑I <sub>OH</sub>	-50	mA	Total output pins
Low level output current	I <sub>OL</sub>	15	mA	Other than high current output pins: per pin
	I <sub>OLC</sub>	20	mA	High current port pin* <sup>3</sup> : per pin
Low level total output current	∑I <sub>OL</sub>	130	mA	Total output pins
Operating temperature	T <sub>opr</sub>	-10 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	600	mW	

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

\*<sup>1</sup> AV<sub>DD</sub> and V<sub>DD</sub> should be set to a same voltage.

\*<sup>2</sup> V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*<sup>3</sup> The high current operation transistors are the N-CH transistors of the PA port.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.5	5.5		Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.5	5.5		Guaranteed data hold operation range during STOP
	V <sub>pp</sub>	V <sub>pp</sub> = V <sub>DD</sub>		V	*6
Analog power supply	AV <sub>DD</sub>	4.5	5.5	V	*1
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*2
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	CMOS schmitt input*3
	V <sub>IHT</sub>	2.0	V <sub>DD</sub>	V	TTL input*4
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin*5
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*2
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	CMOS schmitt input*3
	V <sub>ILT</sub>	0	0.8	V	TTL input*4
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*5
Operating temperature	T <sub>opr</sub>	-10	+75	°C	

\*1 AV<sub>DD</sub> and V<sub>DD</sub> should be set to a same voltage.

\*2 Normal input port (each pin of PD, PE, PF0 to PF3, PG0, PG1, PG4, PG5, PH1 to PH3, PH5, PH7), MP pin.

\*3 Each pin of  $\overline{\text{NMI}}$ , PH6/SI, PH4/ $\overline{\text{SCK}}$ , PH0/RxD,  $\overline{\text{RST}}$ , PI0/ $\overline{\text{EC0}}$ , PI1/CINT0/INT0, PI2/ $\overline{\text{EC1}}$ , PI3/CINT1/INT1, PG2/ $\overline{\text{EC2}}$ /INT2, PG3/ $\overline{\text{EC3}}$ /INT3.

\*4 Each pin of PC.

\*5 It specifies only when the external clock is input.

\*6 V<sub>pp</sub> and V<sub>DD</sub> should be set to the same voltage.

## Electrical Characteristics

## DC Characteristics

(Ta = -10 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V <sub>OH</sub>	PA to PE, PF4 to PH7 PG, PH RST (V <sub>OL</sub> only)	V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -0.5mA	4.0			V
			V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -1.2mA	3.5			V
V <sub>OL</sub>	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.8mA				0.4		V
	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.6mA				0.6		V
Low level output voltage	V <sub>OL</sub>	PA	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 12.0mA			1.5	V
		Input current	I <sub>IHE</sub>	EXTAL	V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V	0.5	40
I <sub>I LE</sub>	V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V				-0.5	-40	μA
I <sub>ILR</sub>	RST		V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V	-1.5	-400	μA	
I/O leakage current	I <sub>IZ</sub>	PA to PI, MP	V <sub>DD</sub> = 5.5V V <sub>1</sub> = 0, 5.5V			±10	μA
Supply current*1	I <sub>DD</sub>	V <sub>DD</sub>	Crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 12pF) of 12MHz		20	45	mA
			V <sub>DD</sub> = 5V ± 0.5V*2				
	I <sub>DD S1</sub>		SLEEP mode		0.8	5	mA
			V <sub>DD</sub> = 5V ± 0.5V				
I <sub>DD S2</sub>	STOP mode				30	μA	
	V <sub>DD</sub> = 5V ± 0.5V						
Input capacity	C <sub>IN</sub>	Other than V <sub>DD</sub> , V <sub>SS</sub> , AV <sub>DD</sub> , AV <sub>SS</sub> pins	Clock 1MHz 0V other than the measured pins		10	20	pF

\*1 When entire output pins are open.

\*2 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	$f_c$	XTAL EXTAL	Fig. 1, Fig. 2	1	10	MHz
System clock input pulse width	$t_{XL}$ , $t_{XH}$	EXTAL	Fig. 1, Fig. 2 (External clock drive)	40		ns
System clock input rising and falling times	$t_{CR}$ , $t_{CF}$	EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns
Event clock input pulse width	$t_{EH}$ , $t_{EL}$	$\overline{\text{EC0}}$ , $\overline{\text{EC1}}$ $\overline{\text{EC2}}$ , $\overline{\text{EC3}}$	Fig. 3	$2t_{\text{sys}}^*$		ns
Event count clock input rising and falling times	$t_{ER}$ , $t_{EF}$	$\overline{\text{EC0}}$ , $\overline{\text{EC1}}$ $\overline{\text{EC2}}$ , $\overline{\text{EC3}}$	Fig. 3		20	ms

\*  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$$t_{\text{sys}} [\text{ns}] = 2000/f_c \text{ (Upper 2-bit = "00")}, 4000/f_c \text{ (Upper 2-bit = "01")}, 16000/f_c \text{ (Upper 2-bit = "11")}$$

Fig. 1. Clock timing

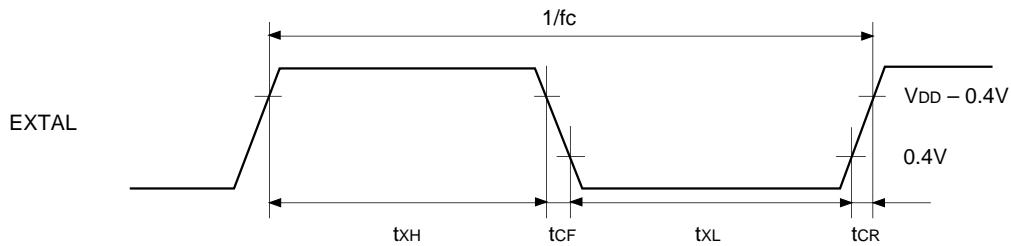


Fig. 2. Clock applying condition

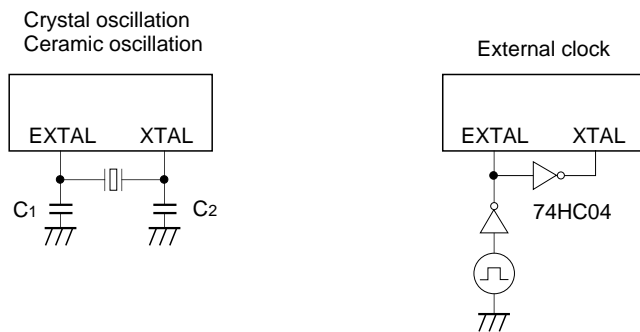
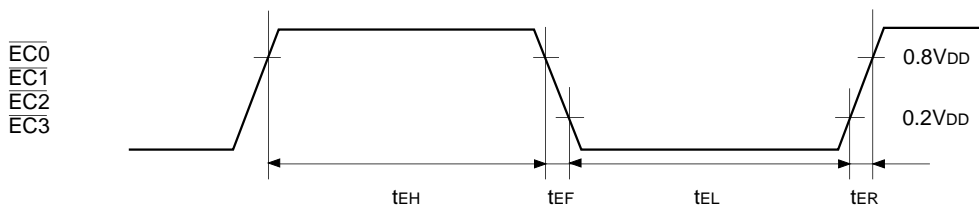


Fig. 3. Event count clock timing



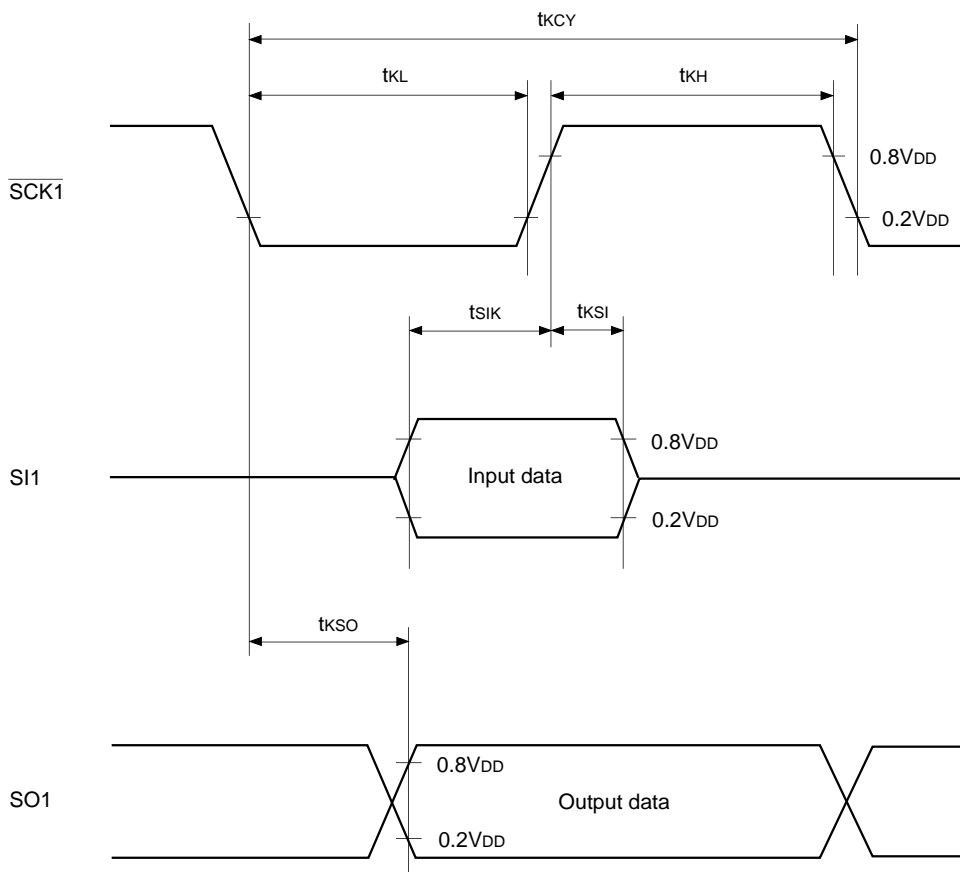
(2) Serial transfer

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK}}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK}}$ high and low level widths	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK}}$	Input mode	400		ns
			Output mode	8000/fc - 50		ns
SI input setup time (against $\overline{\text{SCK}} \uparrow$ )	$t_{\text{SIK}}$	SI	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI input hold time (against $\overline{\text{SCK}} \uparrow$ )	$t_{\text{KSI}}$	SI	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	$t_{\text{KSO}}$	SO	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

**Note)** The load of  $\overline{\text{SCK1}}$  output mode and SO1 output delay time is  $50\text{pF} + 1\text{TTL}$ .

Fig. 4. Serial transfer timing



**(3) A/D converter characteristics**(Ta = -10 to +75°C, V<sub>DD</sub> = AV<sub>DD</sub> = 4.5 to 5.5V, AV<sub>REF</sub> = 4.0 to AV<sub>DD</sub>, V<sub>SS</sub> = AV<sub>SS</sub> = 0V)

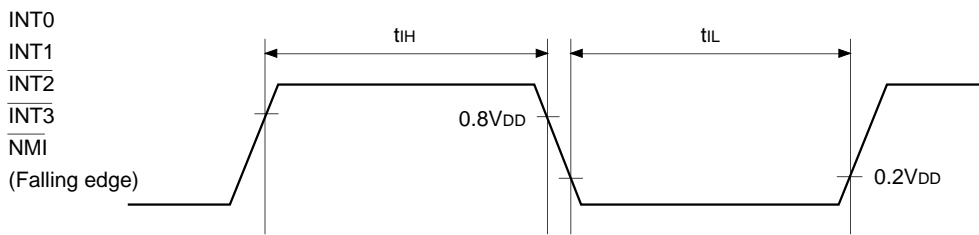
Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Absolute error			Ta = 25°C V <sub>DD</sub> = AV <sub>DD</sub> = 5.0V V <sub>SS</sub> = AV <sub>SS</sub> = 0V			±3	LSB
Conversion time	t <sub>CONV</sub>			160/f <sub>ADC</sub> *			μs
Sampling time	t <sub>SAMP</sub>			12/f <sub>ADC</sub> *			μs
Reference input voltage	V <sub>REF</sub>	AV <sub>REF</sub>		AV <sub>DD</sub> - 0.5		AV <sub>DD</sub>	V
Analog input voltage	V <sub>IAN</sub>	AN0 to AN7		0		AV <sub>REF</sub>	V
AV <sub>REF</sub> current	I <sub>REF</sub>	AV <sub>REF</sub>	Operating mode		0.6	1.0	mA
	I <sub>REFS</sub>		SLEEP mode STOP mode			10	μA

\* The value of f<sub>ADC</sub> is as follows by selecting ADC operation clock (MSC: Address 01FF<sub>H</sub> bit 0).When PS2 is selected, f<sub>ADC</sub> = fc/2When PS1 is selected, f<sub>ADC</sub> = fc

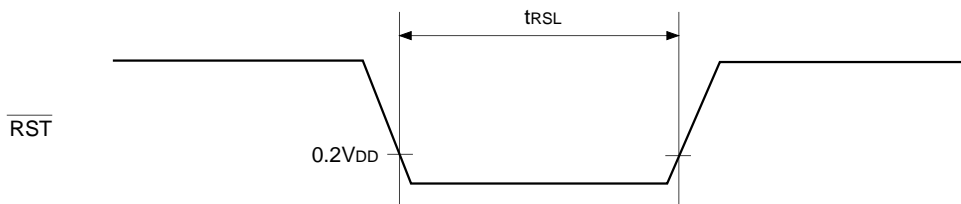
**(4) Interruption, reset input** (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Min.	Typ.	Max.	Unit
External interruption high and low level widths	t <sub>IH</sub>	INT0 INT1 INT2 INT3 NMI		1		μs
	t <sub>IL</sub>					
Reset input low level width	t <sub>RSL</sub>	RST		8/fc		μs

**Fig. 5. Interruption input timing**



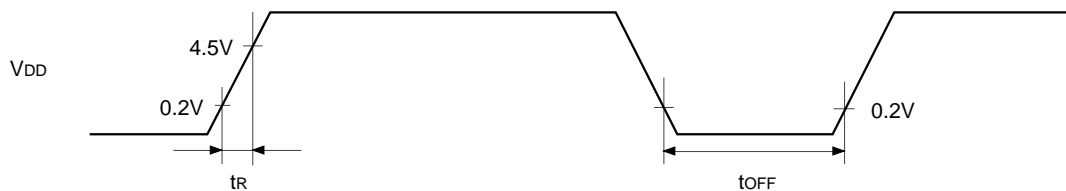
**Fig. 6. Reset input timing**



**(5) Power on reset** (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t <sub>R</sub>	VDD	Power on reset	0.05	50	ms
Power supply cut-off time	t <sub>OFF</sub>		Repetitive power on reset	1		ms

**Fig. 7. Power on reset**



The power supply should be rise smoothly.

Supplement

Fig. 8. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd ( $\Omega$ )	Circuit example
MURATA MFG CO., LTD.	CSA8.00MTZ	8.00	30	30	0	(i)
	CST8.00MTW*					(ii)
	CSA10.0MTZ	10.00	30	30	0	(i)
	CST10.0MTW*					(ii)
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	12	12	470	(i)
		10.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	22	22	0	(i)
		10.00				

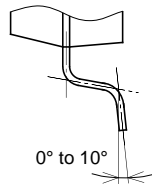
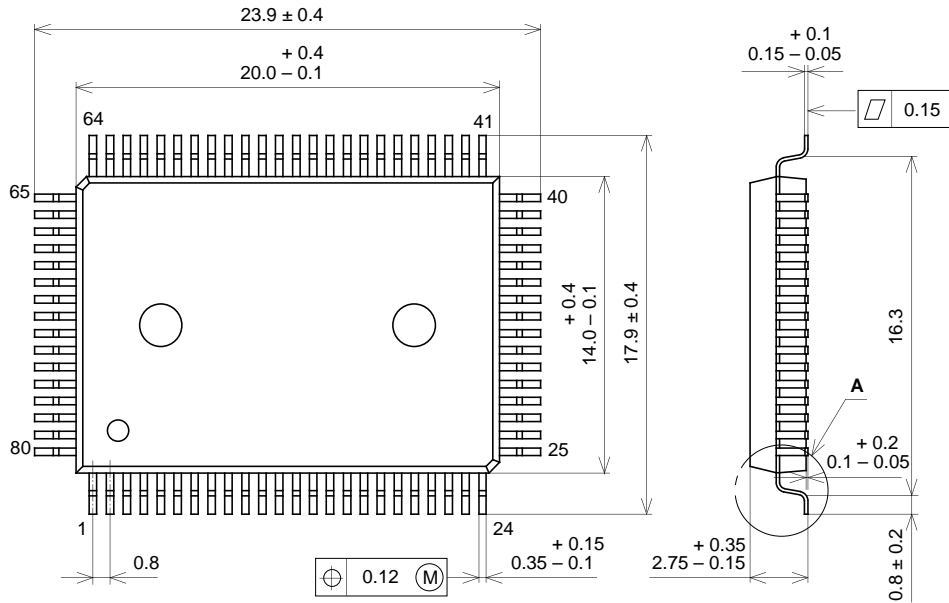
Those marked with an asterisk (\*) signify types with built-in ground capacitance. (C1, C2)

Mask option table

Item	Mask product	CXP861P16Q-1-□□□
Reset pin pull-up resistor	Non-existent/Existent	Existent
Power on reset circuit	Non-existent/Existent	Existent

Package Outline Unit: mm

80PIN QFP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	*QFP080-P-1420-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g



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