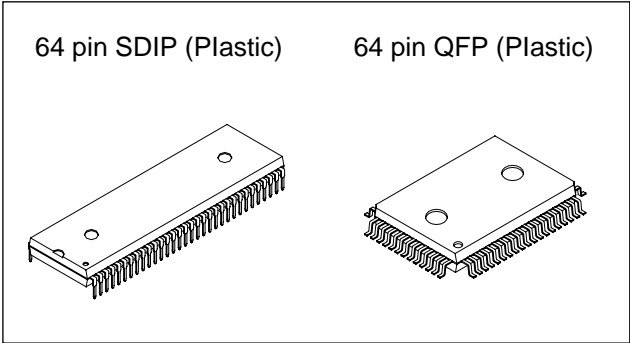


**CMOS 8-bit Single Chip Microcomputer**

**Description**

The CXP85452/85460 are a highly integrated micro-computers composed of a 8-bit CPU, ROM, RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, on-screen display function, I<sup>2</sup>C bus interface, PWM output, remote control reception circuit, HSYNC counter, and watchdog timer.

Futhermore, the CXP85452/85460 series provides power-on reset and sleep functions which enable to lower power consumption.



**Structure**

Silicon gate CMOS IC

**Features**

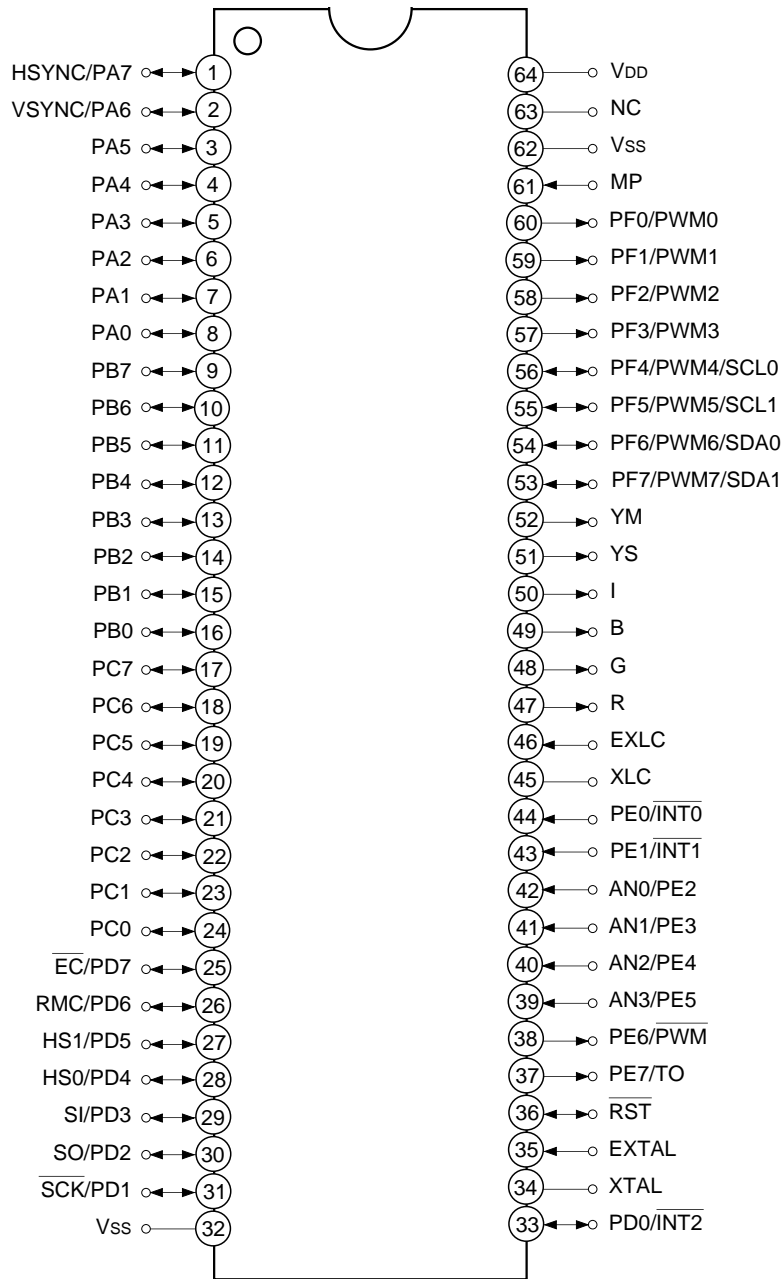
- A wide instruction set (213 instructions) which covers various types of data
  - 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle      0.5µs at 8MHz
- Incorporated ROM capacity      52K bytes (CXP85452)  
60K bytes (CXP85460)
- Incorporated RAM capacity      960 bytes
- Peripheral functions
  - A/D converter                      8-bit, 4-channel successive approximation method  
(Conversion time of 20µs at 8MHz)
  - Serial interface                    8-bit clock sync type, 1 channel
  - Timer                                 8-bit timer  
8-bit timer/counter  
19-bit time-base timer
  - On screen display (OSD) function   12 × 18 dots, 384 character types, 15 character colors,  
12lines of 32 characters,  
black frame output/half blanking, shadow, background  
color on full screen/half blanking,  
double scanning, jitter elimination circuit
  - I<sup>2</sup>C bus interface
  - PWM output                         14 bits, 1 channel  
8 bits, 8 channels
  - Remote control reception circuit   8-bit pulse measurement circuit, 6-state FIFO
  - HSYNC counter                      2 channels
  - Watchdog timer
- Interruption                         13 factors, 13 vectors, multi-interruption possible
- Standby mode                        SLEEP
- Package                              64-pin plastic SDIP/QFP
- Piggyback/evaluator                CXP85400 64-pin ceramic PSDIP/PQFP  
CXP85490 64-pin ceramic PSDIP (accommodates custom font)

Purchase of Sony's I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specifications as defined by Philips.

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

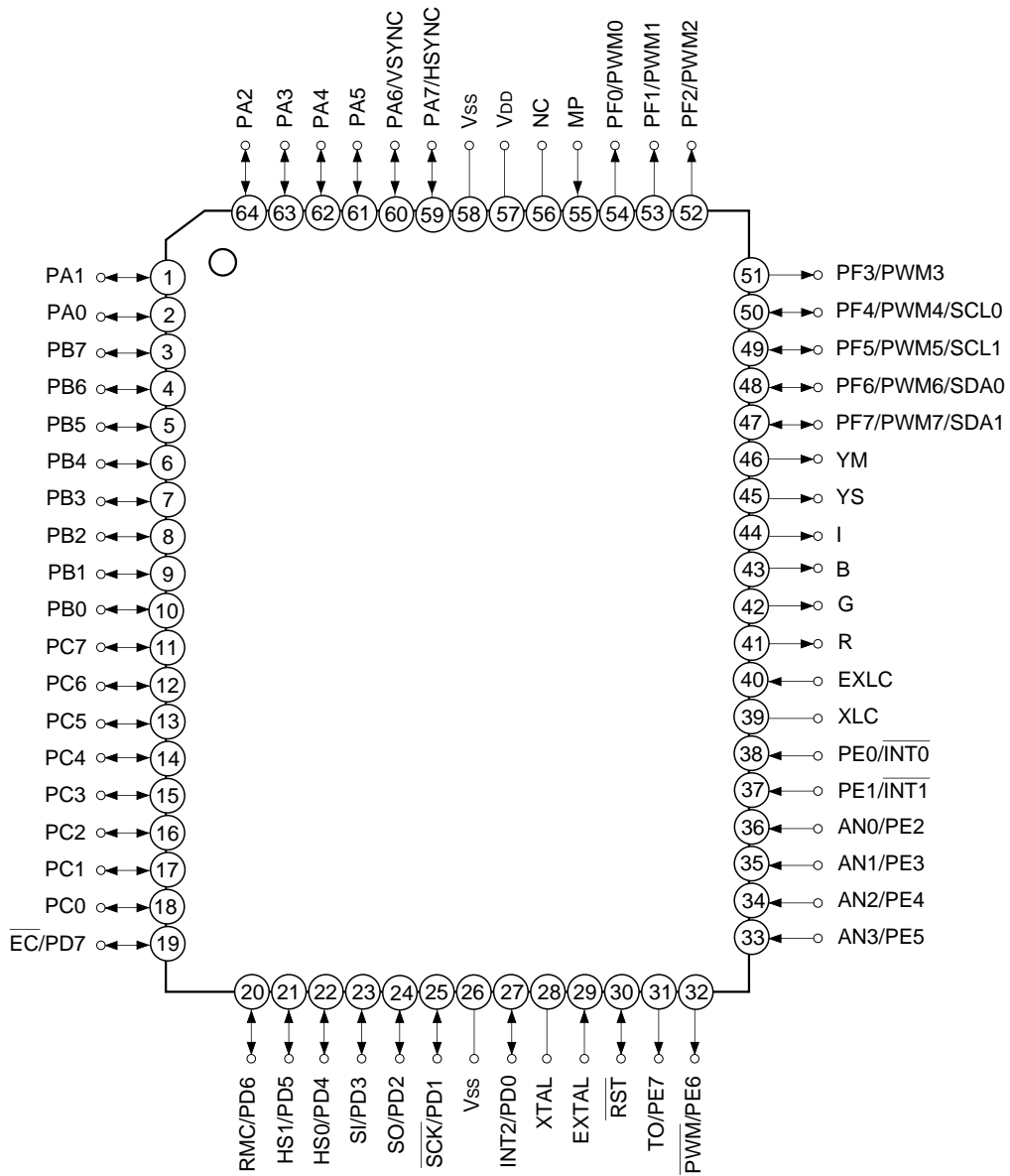


Pin Assignment (Top View) 64-pin SDIP



- Note)**
1. NC (Pin 63) is always connected to V<sub>DD</sub>.
  2. V<sub>ss</sub> (Pins 32 and 62) are both connected to GND.
  3. MP (Pin 61) is always connected to GND.

Pin Assignment (Top View) 64-pin QFP



- Note**
1. NC (Pin 56) is always connected to V<sub>DD</sub>.
  2. V<sub>SS</sub> (Pins 26 and 58) are both connected to GND.
  3. MP (Pin 55) is always connected to GND.

**Pin Description**

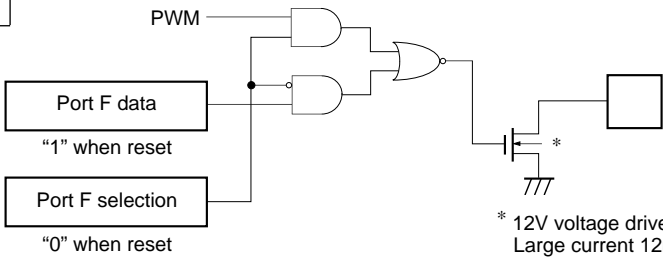
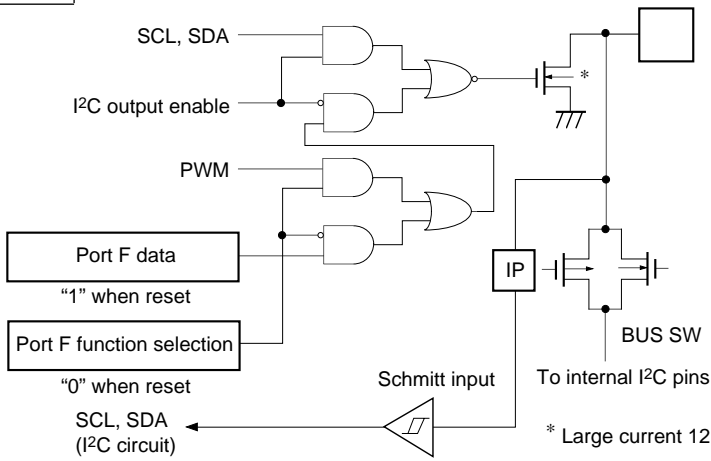
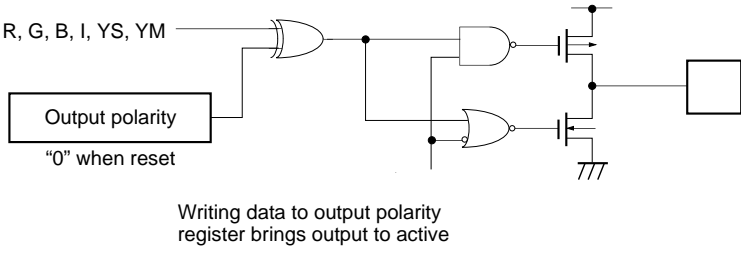
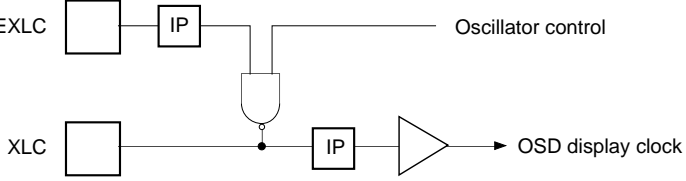
Symbol	I/O	Description		
PA0 to PA5	I/O	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)		
PA6/VS $\overline{\text{SYNC}}$	I/O/Input			OSD display vertical synchronization signal input pin.
PA7/HS $\overline{\text{SYNC}}$	I/O/Input			OSD display horizontal synchronization signal input pin.
PB0 to PB7	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)		
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)		
PD0/ $\overline{\text{INT2}}$	I/O/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. 12mA sink current drive possible. (8 pins)	Input pin for external interruption request. Active when falling edge.	
PD1/ $\overline{\text{SCK}}$	I/O/I/O		Serial clock I/O pin.	
PD2/ $\overline{\text{SO}}$	I/O/Output		Serial data output pin.	
PD3/ $\overline{\text{SI}}$	I/O/Input		Serial data input pin.	
PD4/HS0	I/O/Input		HSYNC counter (CH0) input pin.	
PD5/HS1	I/O/Input		HSYNC counter (CH1) input pin.	
PD6/ $\overline{\text{RMC}}$	I/O/Input		Remote control reception circuit input pin.	
PD7/ $\overline{\text{EC}}$	I/O/Input		External event input pin for timer/counter.	
PE0/ $\overline{\text{INT0}}$ PE1/ $\overline{\text{INT1}}$	Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	Input pin for external interruption request. Active when falling edge. (2 pins)	
PE2/ $\overline{\text{AN0}}$ to PE5/ $\overline{\text{AN3}}$	Input/Input		Analog input pin for A/D converter. (4 pins)	
PE6/ $\overline{\text{PWM}}$	Output/Output		14-bit PWM output pin. (CMOS output)	
PE7/ $\overline{\text{TO}}$	Output/Output		Timer/counter rectangular wave output pin.	
PF0/ $\overline{\text{PWM0}}$ to PF3/ $\overline{\text{PWM3}}$	Output/Output	(Port F) 8-bit output port. Large current (12mA) N-ch open drain output. Lower 4 bits are mid-voltage drive (12V); upper 4 bits are 5V drive. (8 pins)	8-bit PWM output pin. (8 pins)	
PF4/ $\overline{\text{PWM4/SCL0}}$ PF5/ $\overline{\text{PWM5/SCL1}}$	Output/Output/ I/O		I <sup>2</sup> C bus interface transfer clock I/O pin. (2 pins)	
PF6/ $\overline{\text{PWM6/SDA0}}$ PF7/ $\overline{\text{PWM7/SDA1}}$	Output/Output/ I/O		I <sup>2</sup> C bus interface transfer data I/O pin. (2 pins)	
R, G, B, I, YS, YM	Output	OSD display 6-bit output pin. (6 pins)		

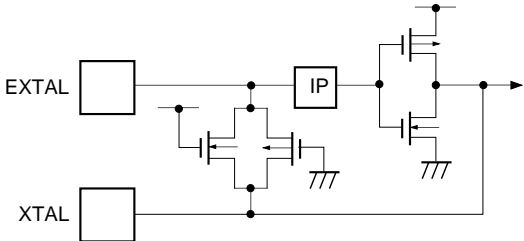
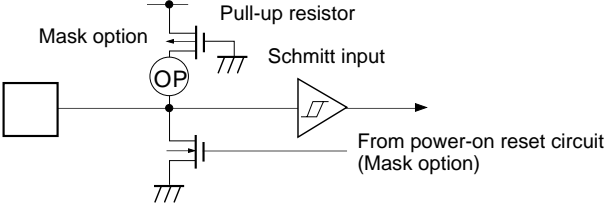
Symbol	I/O	Description
EXLC	Input	OSD display clock oscillation I/O pin. Oscillation frequency is determined by the external L and C.
XLC	Output	
EXTAL	Input	Crystal connection pin for system clock oscillation. When using an external clock, input to EXTAL pin and leave XTAL pin open.
XTAL	Output	
$\overline{\text{RST}}$	I/O	System reset pin for active at low level. This pin becomes I/O pin, and outputs low level at the power on with power-on reset function executed. (Mask option)
MP	Input	Test mode input pin. Always connect to GND.
NC		NC. Under normal operation, connect to V <sub>DD</sub> .
V <sub>DD</sub>		Positive supply voltage pin.
V <sub>SS</sub>		GND. Both V <sub>SS</sub> pins should be connected to common GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0 to PA5 PB0 to PB7 PC0 to PC7  22 pins	<p>Ports A, B, C data</p> <p>Ports A, B, C direction "0" when reset</p> <p>Data bus</p> <p>RD (Ports A, B, C)</p> <p>IP Input protection circuit</p>	Hi-Z
PA6/VSYNC PA7/HSYNC  2 pins	<p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Schmitt input</p> <p>VSYNC HSYNC</p> <p>Input multiplexer "0" when reset</p> <p>IP</p>	Hi-Z
PD0/ $\overline{\text{INT2}}$ PD3/SI PD4/HS0 PD5/HS1  PD6/RMC PD7/ $\overline{\text{EC}}$  6 pins	<p>Port D data</p> <p>Port D direction "0" when reset</p> <p>Data bus</p> <p>RD (Port D)</p> <p>Schmitt input</p> <p><math>\overline{\text{INT2}}</math>, SI, HS0, HS1, RMC, <math>\overline{\text{EC}}</math></p> <p>IP</p> <p>* Large current 12mA</p>	Hi-Z

Pin	Circuit format	When reset
<p>PD1/<math>\overline{\text{SCK}}</math> PD2/<math>\overline{\text{SO}}</math></p> <p>2 pins</p>	<p>Port D</p> <p>SCK or SO</p> <p>Output enable</p> <p>Port D data</p> <p>Port D direction</p> <p>"0" when reset</p> <p>Data bus</p> <p>RD (Port D)</p> <p>SCK only</p> <p>Schmitt input</p> <p>* Large current 12mA</p>	<p>Hi-Z</p>
<p>PE0/<math>\overline{\text{INT0}}</math> PE1/<math>\overline{\text{INT1}}</math></p> <p>2 pins</p>	<p>Port E</p> <p>Schmitt input</p> <p>(Interrupt circuit)</p> <p>Data bus</p> <p>RD (Port E)</p>	<p>Hi-Z</p>
<p>PE2/<math>\overline{\text{AN0}}</math> to PE5/<math>\overline{\text{AN3}}</math></p> <p>4 pins</p>	<p>Port E</p> <p>Input multiplexer</p> <p>To A/D converter</p> <p>Port E function selection</p> <p>"0" when reset</p> <p>Data bus</p> <p>RD (Port E)</p>	<p>Hi-Z</p>
<p>PE6/<math>\overline{\text{PWM}}</math> PE7/<math>\overline{\text{TO}}</math></p> <p>2 pins</p>	<p>Port E</p> <p>TO, PWM</p> <p>Port E data</p> <p>"1" when reset</p> <p>Port E function selection</p> <p>"1" when reset</p>	<p>High level</p>

Pin	Circuit format	When reset
<p>PF0/PWM0 to PF3/PWM3</p> <p>4 pins</p>	<p>Port F</p>  <p>* 12V voltage drive Large current 12mA</p>	<p>Hi-Z</p>
<p>PF4/PWM4/ SCL0 PF5/PWM5/ SCL1 PF6/PWM6/ SDA0 PF7/PWM7/ SDA1</p> <p>4 pins</p>	<p>Port F</p>  <p>* Large current 12mA</p>	<p>Hi-Z</p>
<p>R G B I YS YM</p> <p>6 pins</p>	 <p>Writing data to output polarity register brings output to active</p>	<p>Hi-Z</p>
<p>EXLC XLC</p> <p>2 pins</p>	 <p>Oscillator control</p> <p>OSD display clock</p>	<p>Oscillation halted</p>

Pin	Circuit format	When reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during STOP. (This device does not enter the STOP mode.)</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>	 <p>Mask option</p> <p>Pull-up resistor</p> <p>Schmitt input</p> <p>From power-on reset circuit (Mask option)</p>	<p>Low level</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Mid-voltage drive output voltage	V <sub>OUTP</sub>	-0.3 to +15.0	V	PF0 to PF3 pins
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	∑I <sub>OH</sub>	-50	mA	Total of all output pins
Low level output current	I <sub>OL</sub>	15	mA	Ports excluding large current output (value per pin)
	I <sub>OLC</sub>	20	mA	Large current output port (value per pin)* <sup>2</sup>
Low level total output current	∑I <sub>OL</sub>	130	mA	Total of all output pins
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	1000	mW	SDIP
		600	mW	QFP

\*<sup>1</sup> V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.\*<sup>2</sup> The large current output port is Port D (PD) and Port F (PF).

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing modes.
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing mode or SLEEP mode.
		2.5	5.5	V	Guaranteed data hold range for STOP mode.* <sup>1</sup>
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	* <sup>2</sup>
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	* <sup>3</sup>
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin* <sup>4</sup>
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	* <sup>2</sup>
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	* <sup>3</sup>
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin* <sup>4</sup>
Operating temperature	T <sub>opr</sub>	-20	+75	°C	

\*<sup>1</sup> This device does not enter the STOP mode.\*<sup>2</sup> PA, PB, PC, PE2 to PE5, SCL0, SCL1, SDA0, SDA1 pins\*<sup>3</sup> INT2, SCK, SI, HS0, HS1, RMC, EC, INT0, INT1, HSYNC, VSYNC, RST pins\*<sup>4</sup> Specifies only during external clock input.

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V <sub>OH</sub>	PA to PD, PE6, PE7, R, G, B, I, YS, YM	V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -0.5mA	4.0			V
			V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -1.2mA	3.5			V
Low level output voltage	V <sub>OL</sub>	PA to PD, PE6, PE7, R, G, B, I, YS, YM, PF0 to PF3, $\overline{\text{RST}}^{*1}$	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.8mA			0.4	V
			V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.6mA			0.6	V
		PD, PF	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.0mA			0.4	V
			V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 4.0mA			0.6	V
Input current	I <sub>IHE</sub>	EXTAL	V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V	0.5		40	μA
	I <sub>IHL</sub>		V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V	-0.5		-40	μA
	I <sub>ILR</sub>	$\overline{\text{RST}}^{*2}$	V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V	-1.5		-400	μA
I/O leakage current	I <sub>Iz</sub>	PA to PE, HSYNC, VSYNC, R, G, B, I, YS, YM, $\overline{\text{RST}}^{*2}$	V <sub>DD</sub> = 5.5V, V <sub>I</sub> = 0, 5.5V			±10	μA
Open drain output leakage current (N-ch Tr off)	I <sub>LOH</sub>	PF0 to PF3	V <sub>DD</sub> = 5.5V, V <sub>OH</sub> = 12.0V			50	μA
		PF4 to PF7	V <sub>DD</sub> = 5.5V, V <sub>OH</sub> = 5.5V			10	μA
I <sup>2</sup> C bus switch connection impedance (Output Tr off)	R <sub>BS</sub>	SCL0: SCL1 SDA0: SDA1	V <sub>DD</sub> = 4.5V V <sub>SCL0</sub> = V <sub>SCL1</sub> = 2.25V V <sub>SDA0</sub> = V <sub>SDA1</sub> = 2.25V			120	Ω
Supply current	I <sub>DD</sub>	V <sub>DD</sub> <sup>*3</sup>	1/2 frequency dividing operation mode V <sub>DD</sub> = 5.5V, 8MHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 22pF)		18	30	mA
	I <sub>DDSL</sub>		SLEEP mode V <sub>DD</sub> = 5.5V, 8MHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 22pF)		0.9	3	mA
	I <sub>DDST</sub>		STOP mode <sup>*4</sup> V <sub>DD</sub> = 5.5V, termination of 8MHz oscillation	—	—	—	μA
Input capacitance	C <sub>IN</sub>	PA to PD, PE0 to PE5, SCL, SDA, EXLC, EXTAL, $\overline{\text{RST}}$	1MHz clock 0V for non-measurement pins		10	20	pF

\*1 Specifies  $\overline{\text{RST}}$  pin only when the power-on reset circuit is selected with mask option.

\*2 For  $\overline{\text{RST}}$  pin, specifies the input current when pull-up resistor is selected, and specifies the leakage current when non-resistor is selected.

\*3 When all output pins open. Specifies only when the OSD oscillation is halted.

\*4 This device does not enter the stop mode.

**AC Characteristics**

(1) Clock timing

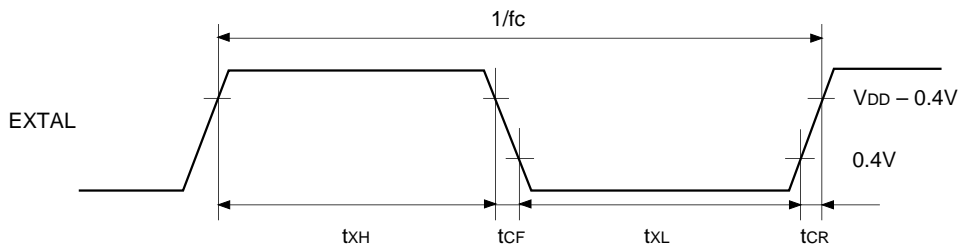
( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	$f_c$	XTAL EXTAL	Fig. 1, Fig. 2	3.5	9	MHz
System clock input pulse width	$t_{xL}$ , $t_{xH}$	EXTAL	Fig. 1, Fig. 2 External clock drive	50		ns
System clock rise and fall times	$t_{cR}$ , $t_{cF}$	EXTAL	Fig 1, Fig 2 External clock drive		200	ns
Event count input clock pulse width	$t_{eH}$ , $t_{eL}$	$\overline{EC}$	Fig. 3	$t_{sys} + 50^{*1}$		ns
Event count input clock rise and fall times	$t_{eR}$ , $t_{eF}$	$\overline{EC}$	Fig. 3		20	ms

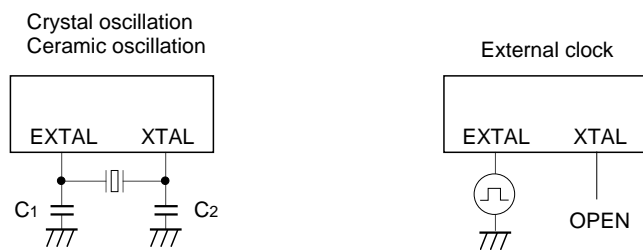
\*1  $t_{sys}$  indicates three values according to the contents of the clock control register (CLC: 00FE<sub>H</sub>) upper 2 bits (CPU clock selection).

$t_{sys}$  (ns) =  $2000/f_c$  (Upper 2 bits = "00"),  $4000/f_c$  (Upper 2 bits = "01"),  $16000/f_c$  (Upper 2 bits = "11")

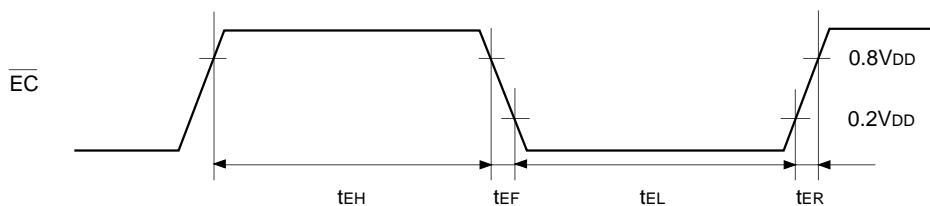
**Fig. 1. Clock timing**



**Fig. 2. Clock applied condition**



**Fig. 3. Event count clock timing**



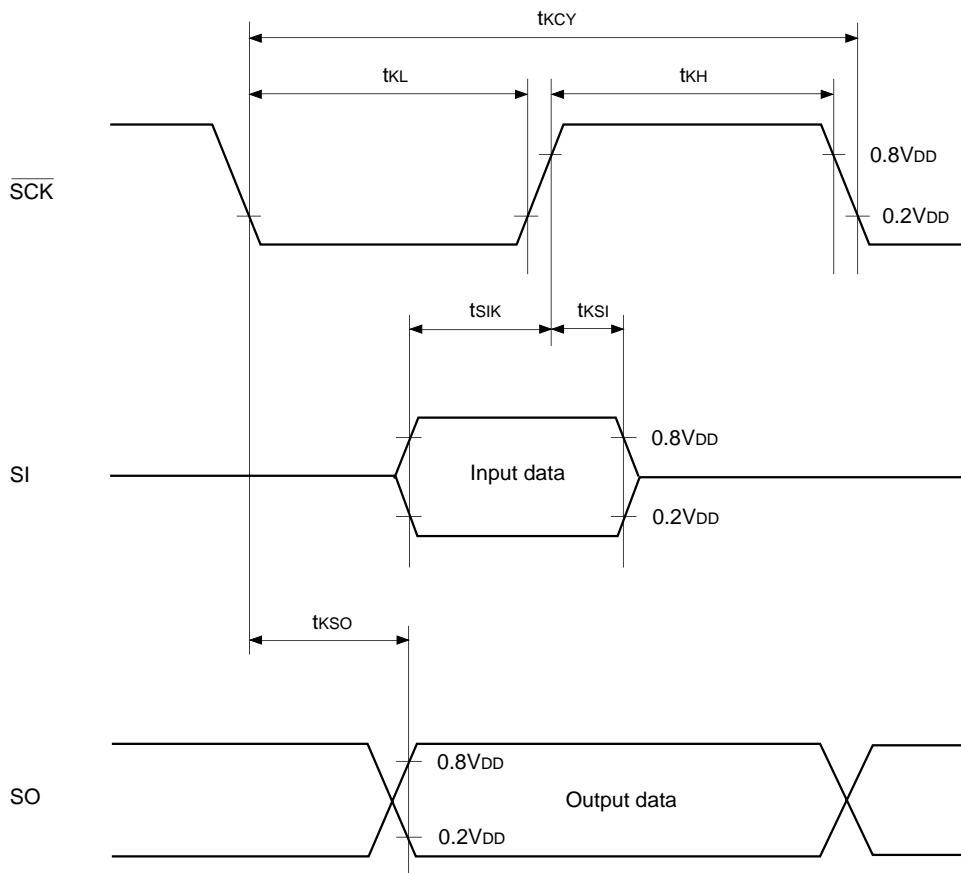
(2) Serial transfer

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK}}$	Input mode	1000		ns
			Output mode	$8000/f_c$		ns
$\overline{\text{SCK}}$ high and low level widths	$t_{\text{KH}}$	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$ input mode	400		ns
	$t_{\text{KL}}$		$\overline{\text{SCK}}$ output mode	$4000/f_c - 50$		ns
SI input set-up time (for $\overline{\text{SCK}} \uparrow$ )	$t_{\text{SIK}}$	SI	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI hold time (for $\overline{\text{SCK}} \uparrow$ )	$t_{\text{KSI}}$	SI	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	$t_{\text{KSO}}$	SO	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

**Note)** The load of  $\overline{\text{SCK}}$  output mode and SO output delay time is  $50\text{pF} + 1\text{TTL}$ .

Fig. 4. Serial transfer timing

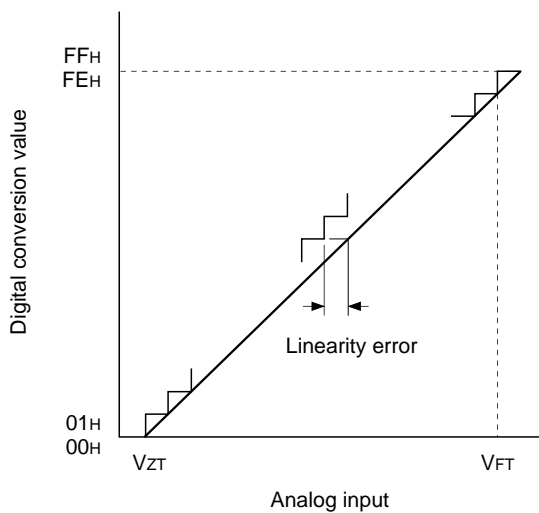


(3) A/D converter characteristics

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						$\pm 3$	LSB
Zero transition voltage	$V_{ZT}^{*1}$		$T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = 0\text{V}$	-50	10	70	mV
Full-scale transition voltage	$V_{FT}^{*2}$			4910	4970	5030	mV
Conversion time	$t_{CONV}$			$160/f_{ADC}^{*3}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$12/f_{ADC}^{*3}$			$\mu\text{s}$
Analog input voltage	$V_{IAN}$	AN0 to AN3		0		$V_{DD}$	V

Fig. 5. Definitions for A/D converter terms



- \*1  $V_{ZT}$ : Digital conversion values change between  $00_H \leftrightarrow 01_H$ .
- \*2  $V_{FT}$ : Digital conversion values change between  $0E_H \leftrightarrow 0F_H$ .
- \*3  $f_{ADC}$  indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC:  $00F6_H$ ) and the bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC:  $00FE_H$ )

PCK1, 0	CKS	
	0 ( $\phi/2$ selection)	1 ( $\phi$ selection)
00 ( $\phi = f_{EX}/2$ )	$f_{ADC} = f_c/2$	$f_{ADC} = f_c$
01 ( $\phi = f_{EX}/4$ )	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ( $\phi = f_{EX}/16$ )	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

(4) Interruption, reset input (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t <sub>IH</sub> t <sub>IL</sub>	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$		1		μs
Reset input low level width	t <sub>RSL</sub>	$\overline{\text{RST}}$		8/fc		μs

Fig. 6. Interruption input timing

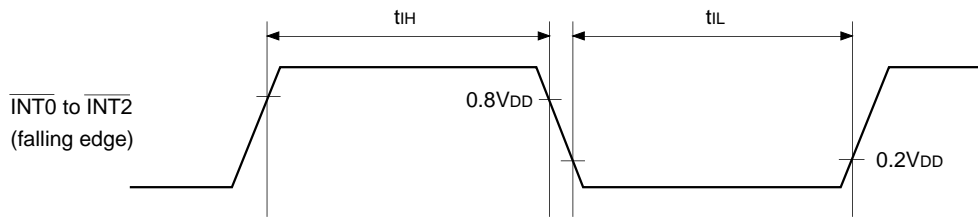
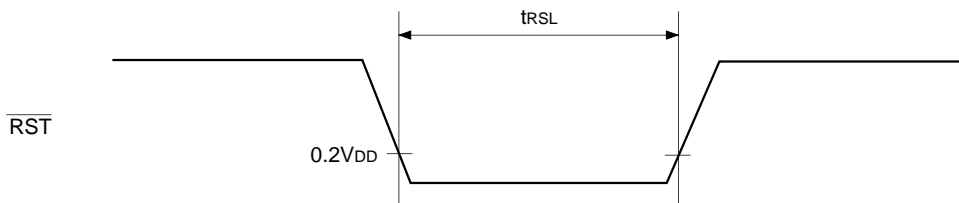


Fig. 7.  $\overline{\text{RST}}$  input timing



(5) Power-on reset

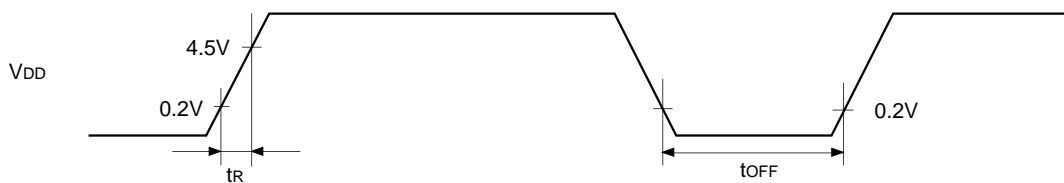
Power-on reset\*1

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rise time	t <sub>R</sub>	VDD	Power-on reset	0.05	50	ms
Power supply cutt-off time	t <sub>OFF</sub>		Repeated power-on reset	1		ms

\*1 Specifies only when power-on reset function is selected.

Fig. 8. Power-on reset



Take care when turning on power.

(6) I<sup>2</sup>C bus timing

(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f <sub>SCL</sub>	SCL		0	100	kHz
Bus-free time before starting transfer	t <sub>BUF</sub>	SDA, SCL		4.7		μs
Hold time for starting transfer	t <sub>HD; STA</sub>	SDA, SCL		4.0		μs
Clock low level width	t <sub>LOW</sub>	SCL		4.7		μs
Clock high level width	t <sub>HIGH</sub>	SCL		4.0		μs
Set-up time for repeated transfers	t <sub>SU; STA</sub>	SDA, SCL		4.7		μs
Data hold time	t <sub>HD; DAT</sub>	SDA, SCL		0*1		μs
Data set-up time	t <sub>SU; DAT</sub>	SDA, SCL		250		ns
SDA, SCL rise time	t <sub>R</sub>	SDA, SCL			1	μs
SDA, SCL fall time	t <sub>F</sub>	SDA, SCL			300	ns
Set-up time for transfer completion	t <sub>SU; STO</sub>	SDA, SCL		4.7		μs

\*1 For the data hold time, the SCL rise time (300ns Max.) is not considered so that 300ns should be exceeded.

Fig. 9. I<sup>2</sup>C bus transfer data timing

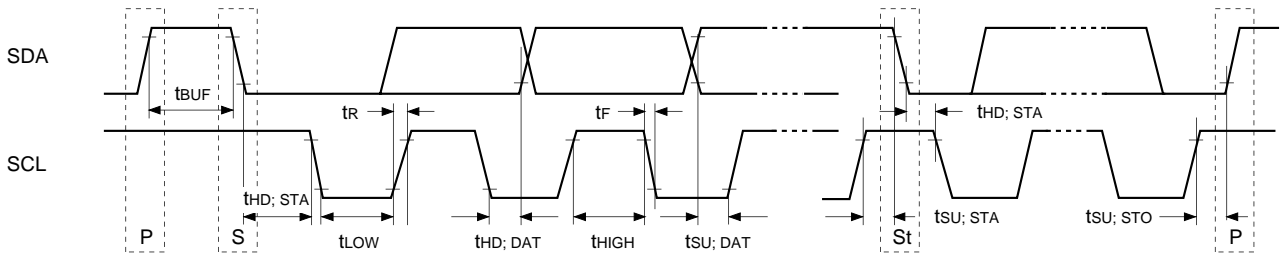
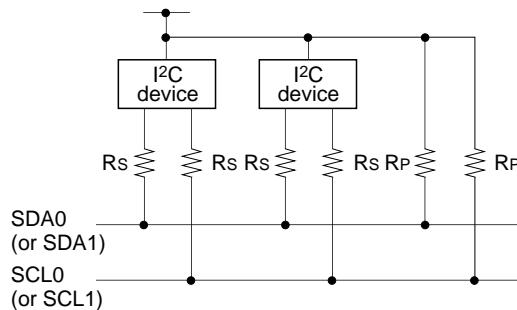


Fig. 10. I<sup>2</sup>C device recommended circuit



- A pull-up resistor (Rp) must be connected to SDA0 (or SDA1), and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce spike noise caused by CRT flashover.

(7) OSD timing (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condiiton	Min.	Max.	Unit
OSD clock frequency	fosc	EXLC XLC	Fig. 12	4	7*1	MHz
					14*2	
HSYNC pulse width	tHWD	HSYNC	Fig. 11	1.2		μs
VSYNC pulse width	tVWD	HSYNC	Fig. 11	1		H*3
HSYNC afterwrite rise and fall times	tHCG	HSYNC	Fig. 11		200	ns
VSYNC beforewrite rise and fall times	tVCG	VSYNC	Fig. 11		1.0	μs

- \*1 Oscillation clock at 4MHz operation
- \*2 Oscillation clock at 8MHz operation
- \*3 H indicates 1HSYNC period.

Fig. 11. OSD timing

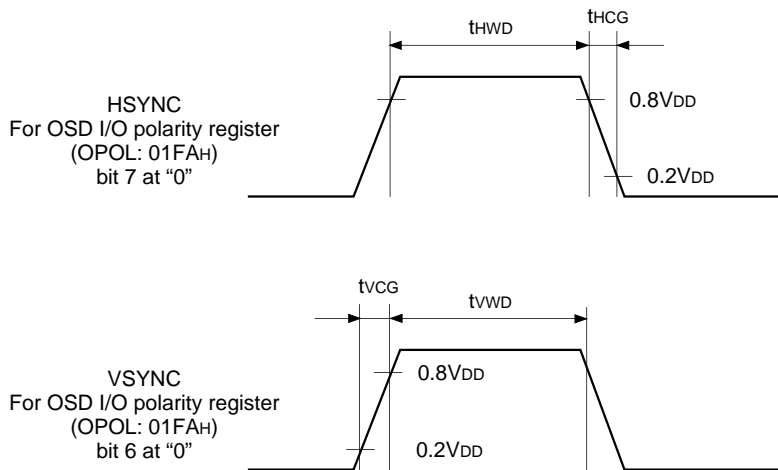
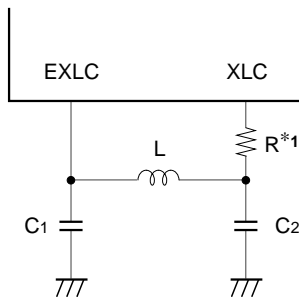


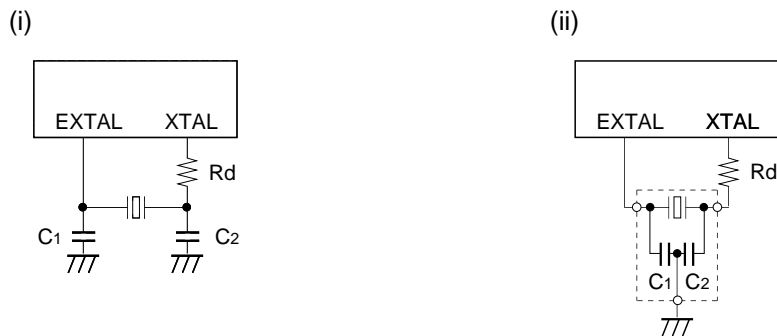
Fig. 12. LC oscillation circuit connection



\*1 The series resistor for XLC is used to reduce the frequency of occurrence of the undesired radiation.

Appendix

Fig. 13. SPC700 Series recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit Example
MURATA MFG CO., LTD.	CSA4.00MG	4.00	30	30	0*2	(i)
	CSA4.19MG	4.19				
	CSA8.00MTZ	8.00				
	CST4.00MGW*1	4.00				(ii)
	CST4.19MGW*1	4.19				
	CST8.00MTW*1	8.00				
RIVER ELETEC CO., LTD.	HC-49/U03	4.00	12	12	0*2	(i)
		4.19				
		8.00				
KINSEKI LTD.	HC-49/U(-S)	4.00	27	27	0*2	(i)
		4.19				
		8.00				

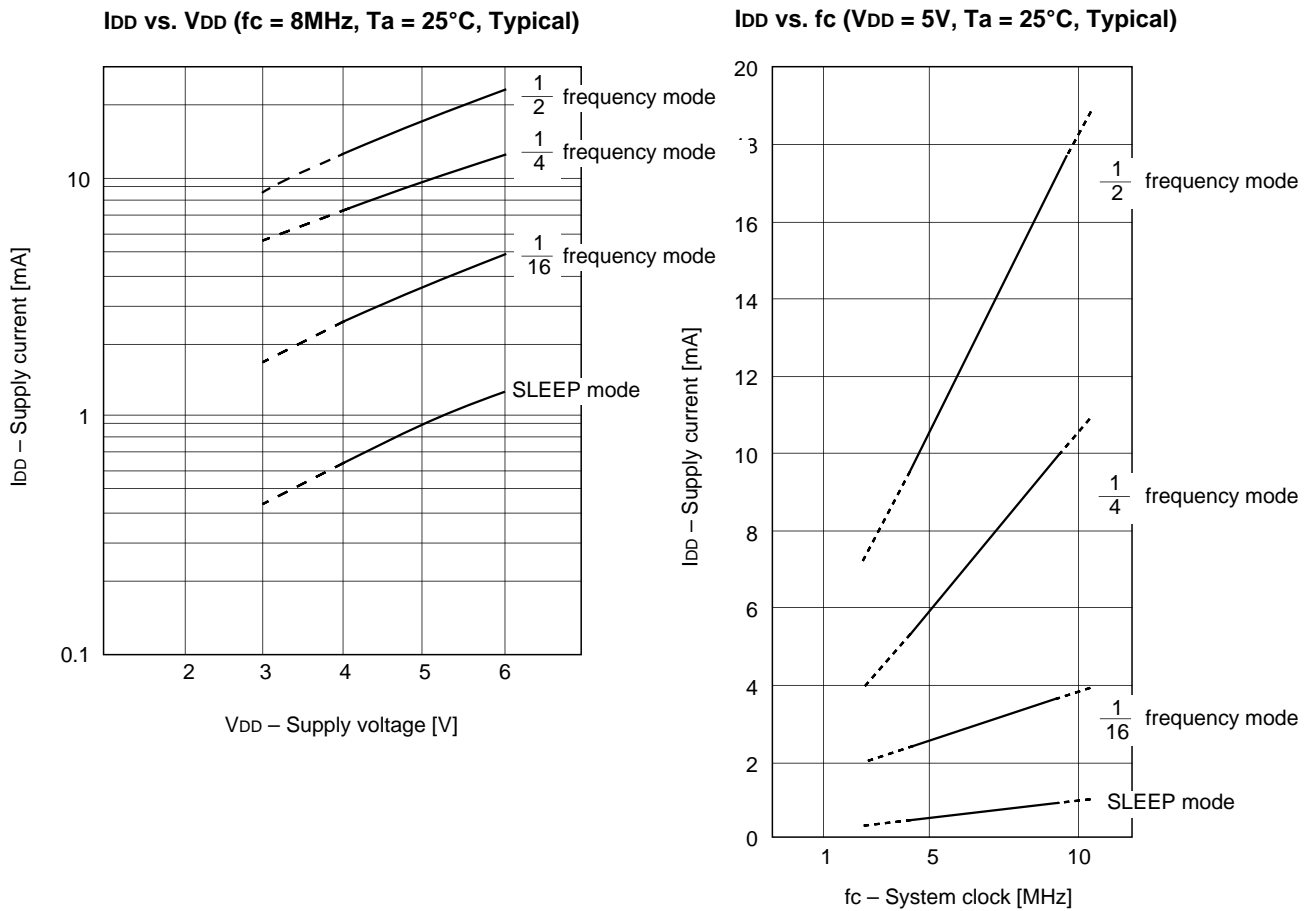
\*1 These models have the on-chip grounding capacitors (C1 and C2).

\*2 The series resistor for XTAL can reduce the effect of the noise caused by the electrostatic discharge.

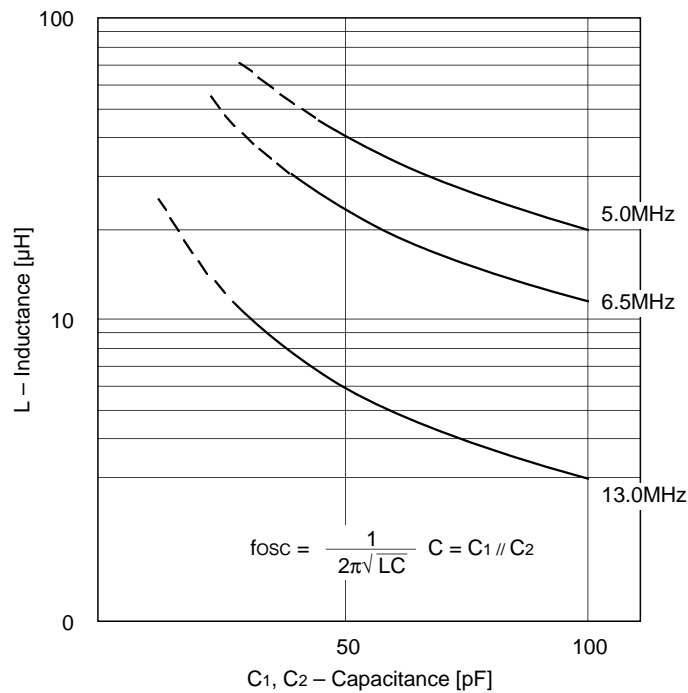
Mask Option Table

Item	Inclusion	
	Non-existent	Existent
Reset pin pull-up resistor	Non-existent	Existent
Power-on reset circuit	Non-existent	Existent

Fig. 14. Characteristics curves



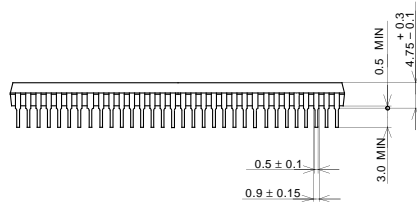
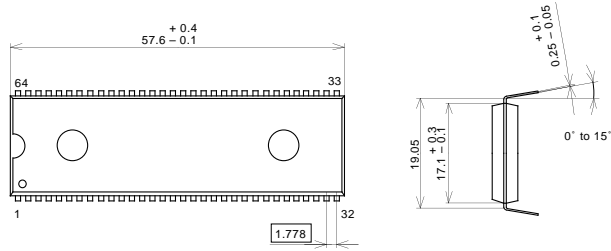
Parameter Curve for OSD Oscillator L vs. C (Analytically calculated value)



Package Outline

Unit: mm

64PIN SDIP (PLASTIC)

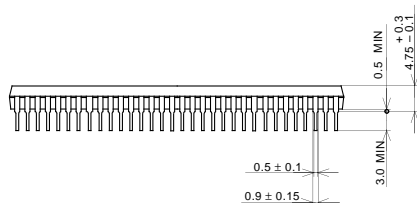
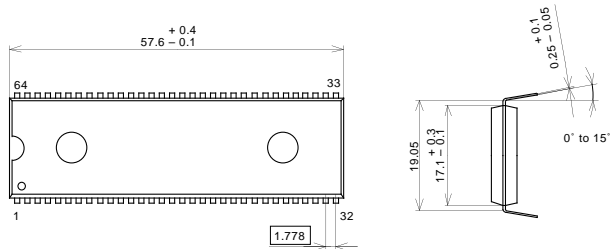


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

64PIN SDIP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

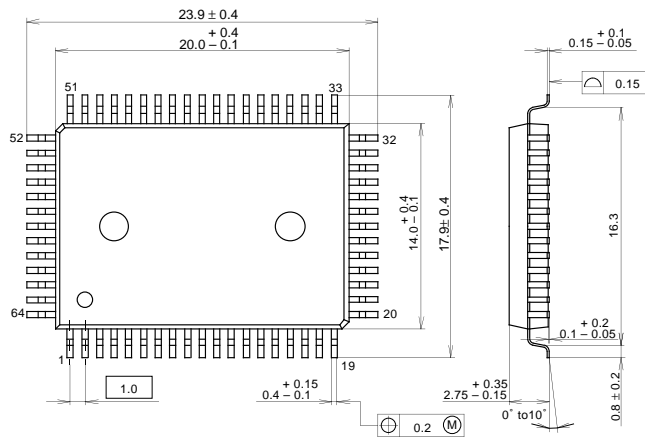
LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm

Package Outline

Unit: mm

64PIN QFP (PLASTIC)

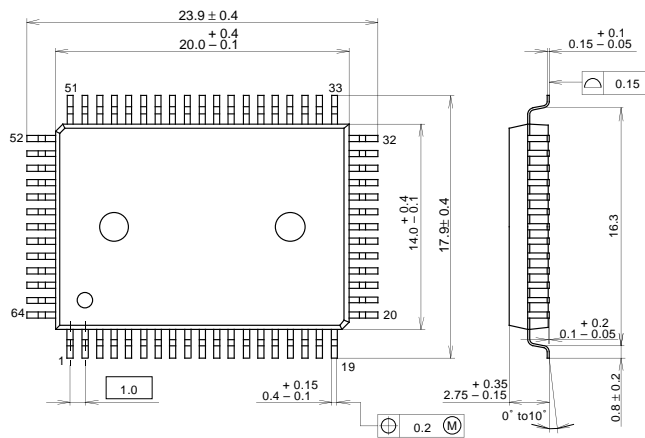


PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

64PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18 $\mu$ m



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